Analysis of a PLL-Based Down Converter and Phase Detection Circuit for Self-Tracking Arrays

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***Abstract*—In this paper we analyze a down conversion and phase detection circuit for a self-tracking receiving antenna array which uses a nested phase-locked loop (PLL) architecture. Analytic expressions for the system model are derived and stability is checked using the Hurwitz criterion. The results lead to design constraints for the employed loop filters, ensuring stability of the proposed circuit. The general influence of parameter choice on system bandwidth and adaption speed is evaluated.**

I. Introduction

Phase-locked loops (PLLs) are essential building blocks of radio receivers. They have been successfully used for self-tracking arrays [1] and for phase conjugation in retro-directive antenna systems [2].

In this paper the PLL-based down converter and phase detection circuit shown in Fig. 1 is analyzed. It shall be used for each element in a receiving antenna array and simultaneously performs the following tasks:

1) Down convert the received signal x_{RF} to an intermediate frequency (IF).
2) Provide a phase-aligned version of the down converted signal y_{Rx} with respect to a reference signal x_{ref}. This achieves automatic self-tracking of incoming signals whereby the radiation pattern is that of a phased array.
3) Extract the radio frequency (RF) signal phase which is observed in the output signal y_{V1}.

The obtained phase information can be used to decode a phase modulated signal directly. Moreover, phase differences between several array elements can be employed for signal analysis like direction-of-arrival (DOA) estimation or to create retro-directive response signals without the need to sample and process each received signal.

II. Circuit Operation Principle

The circuit in Fig. 1 consists of two PLLs. Both have a forward path made from a phase-frequency detector (PFD) d_i, loop filter h_i, and voltage-controlled oscillator (VCO) V_i, $i \in 1, 2$. Using Laplace transform and regarding phase transfer functions, the loop forward gains are given by [3]

$$G_i(s) = K_{\mathsf{d}i} h_i(s) K_{\mathsf{V}i} \frac{1}{s} = K_i h_i(s) \frac{1}{s}, \tag{1}$$

where $K_{\mathsf{d}i}$ is the gain of the PFD and $K_{\mathsf{V}i}$ denotes the VCO sensitivity. $h_i(s)$ is the loop filter transfer function. $\frac{1}{s}$ means

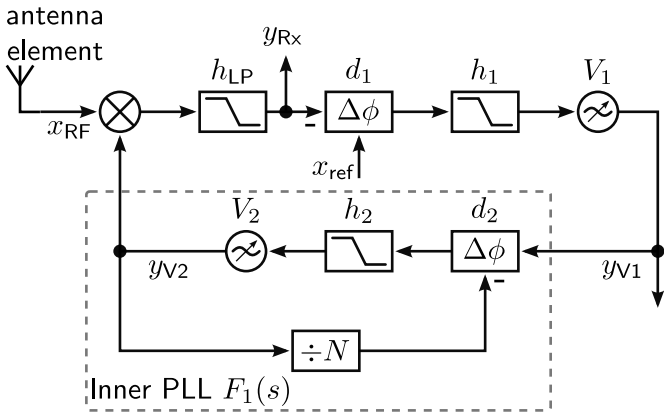

Fig. 1: Block diagram of the PLL-based down converter and phase detection circuit consisting of two nested feedback systems.

that the VCO's output frequency is the integral over a varying phase term. The inner PLL marked in Fig. 1 has a feedback path consisting of a frequency divider. This PLL uses the input y_{V1} from VCO V_1 to synthesize the signal y_{V2} such that its frequency is N-times that of y_{V1}. When in lock, the phase transfer function of the inner loop is

$$F_1(s) = \frac{\tilde{\Psi}_{\mathsf{V2}}(s)}{\tilde{\Psi}_{\mathsf{V1}}(s)} = \frac{G_2(s)}{1 + G_2(s)\frac{1}{N}}. \tag{2}$$

$\tilde{\Psi}_{\mathsf{V1}}$ and $\tilde{\Psi}_{\mathsf{V2}}$ denote the phase variations of the loop input and output signals.

Regarding the outer loop, the feedback path encompasses the whole inner PLL $F_1(s)$, as well as the down mixer and lowpass filter h_{LP}. The filter's purpose is to reject the upper side band of the mixing operation. For the analysis of phase transfer functions, the mixing and filtering operations reduce to a subtraction of the signal phase terms.

Using control theory analysis techniques, the phase transfer function of the whole circuit is found to be

$$G_{\mathsf{sys}}(s) = \frac{\tilde{\Psi}_{\mathsf{V1}}(s)}{\tilde{\Psi}_{\mathsf{RF}}(s)} = \frac{G_1(s)}{1 + G_1(s)F_1(s)}. \tag{3}$$

A phase variation of the RF signal translates to a phase change of the VCO 1 output signal. For the steady state, i.e. $s \to 0$ the output phase becomes $\tilde{\Psi}_{\mathsf{V1}} = \frac{1}{N}\tilde{\Psi}_{\mathsf{RF}}$. This shows the

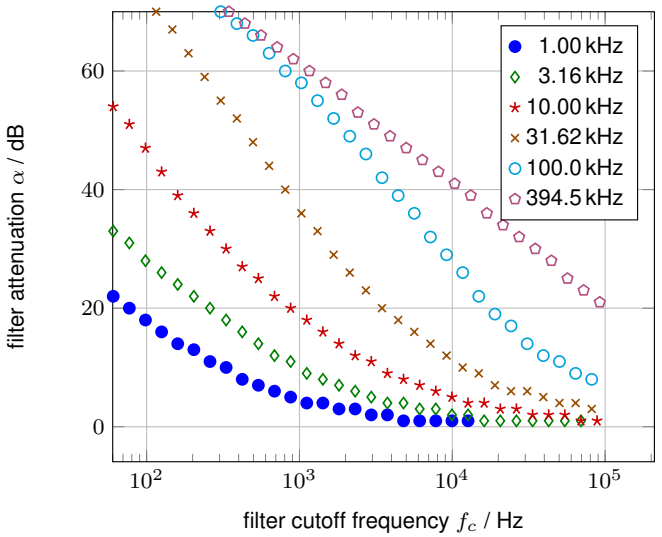

Fig. 2: Stability limits for different f_n plotted over filter characteristics of h_1. The system is stable for parameters below the plotted lines.

phase detection capabilities of the circuit. The nested feedback structure may cause the system to become unstable. In the following, we will show how stability can be guaranteed by appropriate loop filter design.

III. Stability Analysis

Since parameters like PFD gain, VCO sensitivity, and division factor N are usually predefined, our analysis focuses on the loop filters parameters. We assume that both h_1 and h_2 are lowpasses with one zero and one pole. The inner PLL is then characterized by a damping factor ζ and a natural frequency f_n, both defined by $h_2(s)$. h_1 shall be described by its 3 dB-cutoff frequency f_c and its maximum stop-band attenuation α.

As an example, the circuit is used to receive a signal of $f_{\mathsf{RF}} = 5.8\,\mathrm{GHz}$. Assuming a reference frequency of 100 MHz, the division factor must be $N = 57$. The sensitivities of the PLLs are $K_1 = 40.0\,\mathrm{kHz}$ and $K_2 = 100.0\,\mathrm{MHz}$. To attain optimum acquisition time, the damping factor of the inner loop is set to $\zeta = 1/\sqrt{2}$ [3]. The maximum attainable natural frequency of the inner PLL is given by

$$f_n < \frac{1}{2\pi} \cdot 2\frac{K_2}{N}\zeta = 394.8\,\mathrm{kHz}. \tag{4}$$

System stability depends on h_1 and is checked by the Hurwitz criterion. Fig. 2 shows the borders of the stable region, given different values of f_n, over the parameter space of h_1. f_c and α must be chosen such that they are below the plotted borders. It can be seen, that the valid parameter space generally widens for larger f_n. This is to be expected as it means that a more agile frequency synthesis in the inner loop allows for faster changes, i.e. larger bandwidth, in the outer loop.

The valid parameter space of $h_1(s)$ can be used to optimize the circuit for a desired application. In the following, we show the influence of the outer loop filter on system performance.

Set	f_c (kHz)	α (dB)	f_{max} (kHz)	ϕ_{marg} (°)	G_{marg} (dB)
1	1.0	10	102.9	64.9	13.7
2	1.0	20	4.9	69.0	23.5
3	1.0	30	4.3	31.8	32.7
4	0.1	10	91.4	65.8	13.8
5	10.0	10	17.5	55.5	13.1
6	10.0	20	13.8	28.4	20.3

TABLE I: Maximum frequency for $\epsilon = 5\,\%$, phase, and gain margins for six filter parameter sets using $f_n = 394.5\,\mathrm{kHz}$.

IV. Outer Loop Filter Parameter Choice

Before we can optimize, we need to define system performance metrics. Feedback systems are generally characterized by their phase margin ϕ_{marg} and gain margin G_{marg} which are measures for settling time and stability reserve. For the proposed circuit, it is important to know the maximum frequency at which phase changes can be detected without distortions. The system output should therefore be within a $\pm\epsilon$ region around its steady state $1/N$ over a large bandwidth. Such a condition can be formulated as

$$(N|G_{\mathsf{sys}}(j2\pi f)| - 1)^2 < \epsilon^2. \tag{5}$$

f_{max} is the maximum frequency for which this is fulfilled and reflects the system bandwidth. Faster phase changes will not be detected correctly.

We select the inner loop bandwidth $f_n = 394.5\,\mathrm{kHz}$, define $\epsilon = 0.05$, and regard different sets of filter parameters listed in Table I. Phase margin is decreased the closer we get to the stability boundaries. This can be achieved by an increase in both f_c and/or α. Increasing the filter attenuation increases gain margin G_{marg} but reduces system bandwidth and phase margin. Comparing the sets, no. 1 is optimum in terms of f_{max}. ϕ_{marg} is also very high, ensuring that the system will not oscillate. The gain margin G_{marg} is rather low in comparison but margins in excess of 10 dB are usually sufficient. Using parameter set 1, the system can directly receive a 5.8 GHz signal with 100 kHz bandwidth. Larger bandwidths can be achieved by decreasing N or increasing K_2.

V. Conclusion and Outlook

In this work we have presented stability conditions and performance indicators of a PLL-based down converter and phase detection circuit to be used for self-tracking receiving antenna arrays. We have analyzed the influence of the PLL loop filter parameters on system behavior. Further steps will include the optimization of filter parameters for application specific requirements and the use of higher order loop filters.

References

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