System Concept of a Compact Multi-Antenna GNSS Receiver

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***Abstract*—This paper presents the conceptual design of a compact 2x2 array receiver for GNSS applications. Besides mere miniaturization, the goal of this work is also investigation on novel techniques for coping with the strong mutual coupling imposed in electrically small antenna arrays and RF front ends, by means of eigenmode reception and digital beamforming in the beam space.**

***Index Terms*—Antenna array, digital beamforming, mutual coupling, decoupling, orthogonal modes.**

I. Introduction

Many applications of GNSS, like transport of people or goods, in particular defence and law enforcement, demand ever more robust positioning solutions. Within the single antenna receivers, digital signal processing techniques allowed for certain enhancements in terms of multipath and jamming suppression, which contributes to robustness. However, with advancement of the integrated circuits (ASIC and FPGA), powerful multi-antenna solutions arose, which comprise digital beamforming (DBF) algorithms for suppressing the unwanted signals (noise and interference) and enhancing the gain in the directions of the desired satellites. These techniques have been known for many years and have already been successfully implemented in GNSS receivers [2].

The purpose of this study is to provide benefits of array processing on a smaller scale, where compactness is achieved by reducing not only the size of the single antenna elements and front-ends, but also distances between them. Here, mutual coupling plays a significant role. To overcome its effect, a combination of hardware and software techniques is proposed. Firstly, the highly coupled reception patterns are decomposed by means of a decoupling and matching network (DMN) to an orthogonal subspace of beams so that every output of the network represents a different orthogonal beam. After RF processing by means of CMOS-integrated RF front ends and A/D converters, the proposed DBF algorithms must operate in the beam space, rather than in the usual element space. The challenges are set upon the fact that the beams differ in their shape, radiation efficiency and gain (SNR).

In Fig. 1, the new hardware architecture is illustrated. Compared to previous approaches [2], a DMN is inserted between the antenna array and the calibration network, which is composed of power divider (PD) and directional couplers (DC). The grey-shaded blocks in Fig. 1 represent sections II-IV, where we explain the new concept as well as the new challenges coming along with it. Simulated performances are presented in section V.

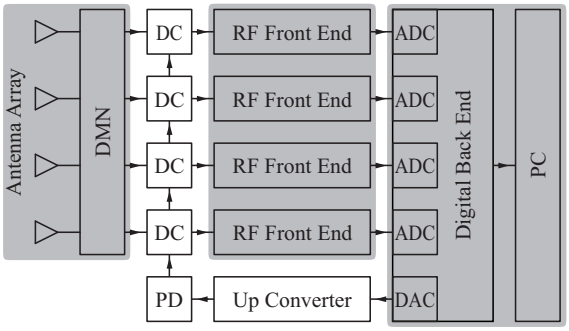

Fig. 1. Proposed architectural modification for the hardware side of the receiver. For acronyms see main text.

II. Antenna Array and DMN

The antenna array is one of the elements which affect most the miniaturization capability of the overall system: the challenge is to miniaturize the array elements and, additionally, to use minimal inter-antenna distances while keeping the radiation properties of the overall array within the performance requirements.

Microstrip radiators have numerous advantages over other kind of GNSS antennas, among them relatively easy manufacturability (thanks to their layered-structure) and the possibility to integrate antennas, feeding layers and other

circuitry in a multi-level solid structure, as well as the existence of different types of miniaturization techniques.

In order to accomplish this goal for the single radiator, the use of a substrate with high permittivity (ROGERS RT 6010, $\varepsilon_r = 10.2$, $\tan\delta = 0.0023$) [1] with a relatively high thickness ($h = 5.08$ mm) has been chosen, to provide good performance both in terms of bandwidth and miniaturization (achieved miniaturization factor of 3.3).

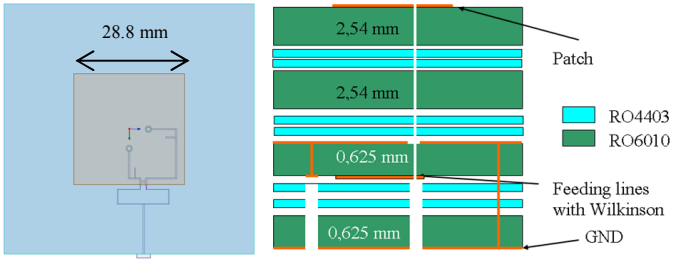

Fig. 2. Top view (left) and stack-up of the radiator (right).

The antenna element is essentially a square patch fed by two vias, with power division for RHCP operation realized by a Wilkinson power divider, as shown in Fig. 2. The antenna manages to reach very good performances both in terms of radiation patterns and polarization purity. Fig. 3 depicts the axial ratio vs. frequency and the radiation pattern in a vertical plane cut at the central frequency of the Galileo E1-band, 1575 MHz. The achieved AR 3-dB bandwidth is over 25 MHz, which is significantly more than the necessary 4 MHz bandwidth for coping with the fabrication inaccuracies.

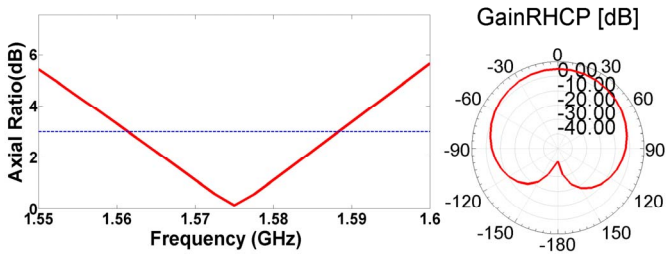

Fig. 3. Axial ratio versus frequency (left) and RHCP gain radiation pattern at central frequency of E1 band - 1575 MHz.

The antenna array consists of 2x2 squarely arranged elements placed at inter-element distances $d = \lambda/4$ (47.5 mm). This chosen geometry is optimal for maximum radiation efficiency as discussed in [1]. In a receiver scenario, strong mutual coupling at reduced element separations of $d < \lambda/2$, results in embedded elements' impedances that are different from their self-impedances. Therefore, compact arrays are inherited with poor input matching and insufficient degrees of freedom. Several approaches using DMNs involving eigenmode excitations for mitigating coupling have been reported in the literature. Eigenmode excitations can be realized using an impedance transformation network or a combination of microstrip components (hybrids, couplers and stubs) [3]. The former method requires a priori accurate estimation of the antenna impedance matrix which might not be possible. Thus a decoupling network consisting of four 180°-hybrid couplers for producing the orthogonal modes (usually close to eigenmodes in symmetrical antennas) is proposed (Fig. 4). Furthermore, a simplified single port matching is applied. In mathematical terms, the resulting scattering matrix has zero off-diagonal elements, meaning no coupling between the output ports, and zero diagonal elements meaning perfect matching.

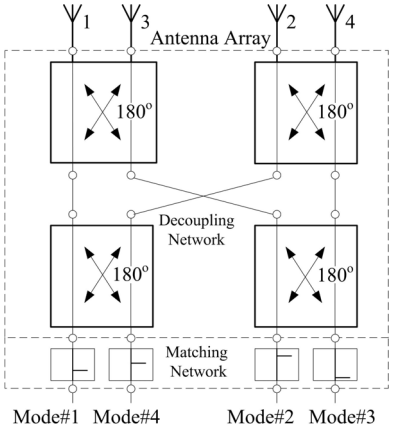

Fig. 4. Block diagram of complete decoupling and matching network for 4-element array in square arrangement, using four 180°-hybrids, and single stub matching networks.

The eigen-decomposition of simulated antenna array radiation patterns results in eigenvectors and respective eigen-efficiencies or modal radiation efficiencies. In Fig. 5, simulated modal realized-gain RHCP patterns are shown, when the antenna array elements are excited with exact decomposed eigenvectors, which might not be exactly true in practical implementations. The simulated modal radiation efficiencies without the matching network are 93%, 63%, 45%, and 24% respectively. Mode#4 or π-mode gives the minimum eigenefficiency, but has the most and deepest nulls, which is significant for interference cancellation.

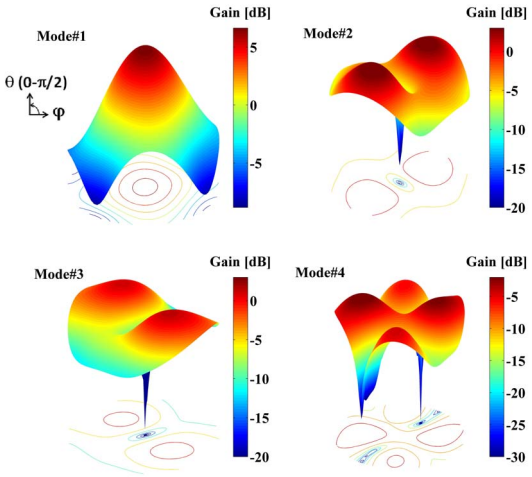

Fig. 5. Simulated exact eigenmode realized-gain RHCP patterns for a 4-element planar lossy array in a square arrangement, where mode#1 has in-phase (++++) excitation for elements, mode#2 has (++--) excitation with one null, mode#3 has (+--+) excitation with two nulls,

mode#4 has (+-+-) excitation with three nulls. mode#1 has the maximum gain, and mode#4 has the minimum gain but the deepest nulls.

III. RF Receiver Front End

The RF front end (Fig. 6) comprises all circuitry needed for conditioning of the output signal of the antenna structure (including DMN and calibration network) for analogue-to-digital conversion. In order to comply with the miniaturization requirement, we aim for implementation of all four receiver paths into one application-specific integrated circuit (ASIC) in a 0.18-µm CMOS technology. The main blocks and their interconnections are shown.

The first two stages of the signal paths are a low-noise amplifier (LNA) and an external surface acoustic wave (SAW) filter. The SAW filter is used for suppression of unwanted signals from the following mixer stage (MIX), especially within the image and half-IF band, as well as out-of-band interferers, e.g., GSM-1800. Since DMN, DC, and several connectors precede the front-end module, an LNA is needed as the first stage in order to fulfil the noise requirements for the whole chain. Therefore, we employ the SAW filter behind the LNA. However, it also implies that the LNA must be capable of operating out-of-band interferers without going into saturation. Another issue is the necessity of 50-Ω terminations at the output of the LNA and the input of the mixer stage, which require additional matching circuits. After the mixer, an active intermediate-frequency filter (IFF) and a coarsely tuned variable-gain amplifier (VGA) are employed to filter out unwanted aliases and provide sufficient gain, respectively.

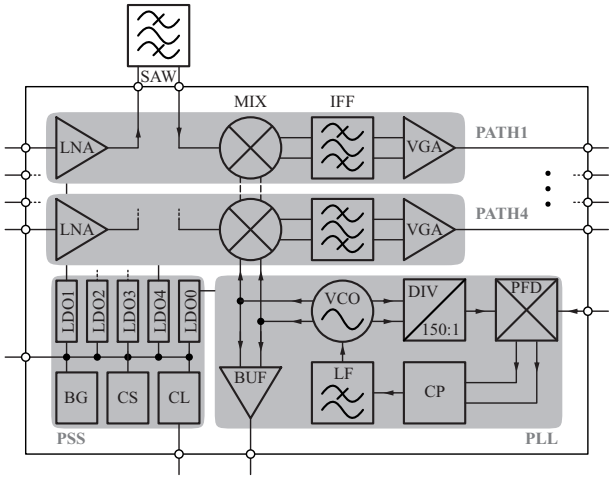

Fig. 6. Block diagram of the receiver frond end. For acronyms see text.

The mixers' local-oscillator signal (LO) is synthesized with a fixed-frequency phase-locked loop (PLL) which is fed with an external reference-oscillation signal (RO), which is generated at the digital back end via direct digital synthesis (DDS). Since all oscillation signals are derived from the same clock, the receiver is capable of carrier-phase tracking applications. The PLL consists of a phase-frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO), and an integer divider (DIV). The LO is additionally buffered (BUF) to drive the external up converter. Another important section of the front end is the power-supply system (PSS). It possesses five low-dropout regulators, one for each signal path and one for the PLL in order to reduce coupling between the paths due to common power supply nodes. A bandgap voltage reference (BG) is needed to generate a temperature-stabilized voltage source. Furthermore, current sources (CS) are employed for biasing, and a control logic block (CL) is used to tune gain of the VGA and centre frequency of the VCO in a static manner (no feedback).

IV. Digital Receiver Back End

The digital part of the receiver is based on the platform described in [2]. The system employs several ADCs and DACs connected to an FPGA where high-rate baseband processing modules are instantiated. In the present case four ADCs and one DAC are required. The FPGA interacts with a Personal Computer (PC) which controls the baseband processing modules and computes the final position, velocity, and time (PVT).

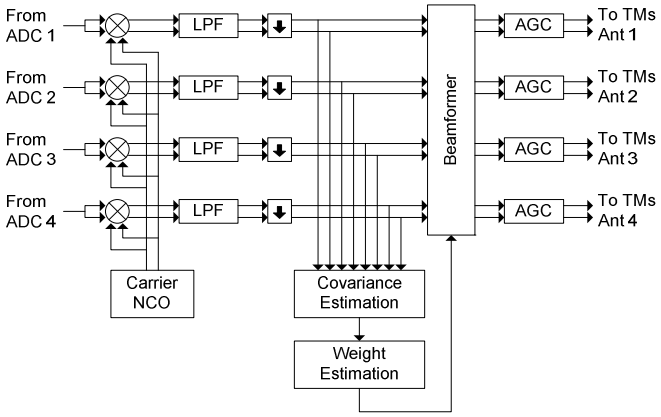

Fig. 7: Signal pre-processing and beamforming.

Different baseband processing blocks are briefly described following the signal path. After digitization, the signal is pre-processed in a digital filter which is detailed in Fig. 7. First, the real input data is multiplied by a digital carrier signal to generate a complex signal on lower IF. Afterwards, the signal is down-sampled after filtering (LPF).

Interference mitigation is achieved by passing the filter output to the beamformer (pre-correlation). The latter applies a projector matrix which is computed in the block "weight estimation" to the filtered input signals. Most of the proposed beamforming algorithms rely on the signal covariance matrix. Thus, only two high-level blocks "Covariance-Estimation" and "Weight-Estimation" are shown in the schematic. The objective is to find adequate implementations which yield a trade-off between beamforming performance and costs in terms of logic-cell requirements on the FPGA.

In order to reduce the word length for the correlation process, a digital automatic gain control (AGC) is applied after beamforming. The correlation process is computed by

several tracking modules detailed in Fig. 8. Compared to most single antenna architectures, the modules correlate a locally generated carrier- and code-signal with each complex signal generated by the beamformer. Up to twelve modules with at least 5 x 4 = 20 complex integrators are used in this case.

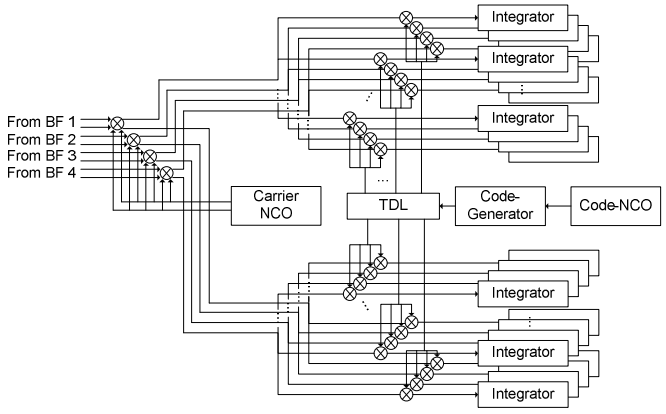

Fig. 8: Tracking module implemented in the FPGA.

Control of the tracking modules, i.e. acquisition, tracking, beamforming (post-correlation) is computed on the PC. Therefore, the integrator outputs are periodically transferred to the PC via a cPCI interface and control values computed by the control algorithms are returned. Typical tracking loops are applied, but in contrast to single antenna GNSS receivers, the correlator outputs are weighted based on beamforming results before they are summed and committed to standard loop algorithms. In contrast to the pre-correlation beamforming, algorithms for amplifying the line-of-sight signal and mitigating multipath effects are computed in software. Applied algorithms have to be evaluated in order to find a reasonable trade-off between computing requirements and beamforming performance. A baseband calibration signal is also generated on the FPGA. A reserved PRN sequence is fed back into the front ends and tracked by a dedicated tracking module. Phase variations occurring in the analogue signal path can be corrected based on tracking results.

In addition to baseband processing, PVT, direction-of-arrival (DoA) and direction-of-interference (DoI) estimation are computed on the PC. The latter tasks have lower priority in contrast to the baseband processing since update rates are much lower (1 Hz). Thus, a multithreaded receiver has to be implemented. Concerning DoA estimation algorithms, different approaches are implemented and compared in terms of estimation accuracy and computing requirements.

V. Simulated Performance

In order to assess the system performance, software simulations have been carried out. A scenario (Table I) with three band-limited interfering signals (BLI) was tested for a null-constraint deterministic (a priori known DoA and DoIs) and an LMS adaptive beamformer. It can be seen in Fig. 9 that even though the estimated CN0 drops once the interference starts, the receiver can still track the satellite signal.

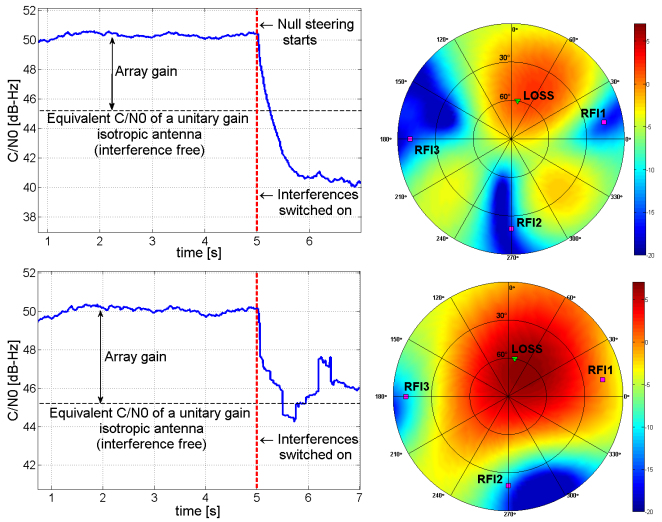

Fig. 9. CN0 vs. time (left) and resulting beamforming (right) of the deterministic (up) and adaptive (down) DBF algorithms.

TABLE I
Parameters of the Simulated Scenario

Signal type	DoA/ DoI azimuth	DoA /DoI elevation	Carrier frequency	Received power [dBW]
L1-CA PRN1	80°	60°	L1	-160
0.5 MHz BLI	10°	15°	L1+0.7 MHz	-125
0.1 MHz BLI	270°	20°	L1+0.5 MHz	-120
0.2 MHz BLI	180°	10°	L1+1.5 MHz	-115

VI. Conclusion

We have proposed a conceptual design for a compact 2x2 GNSS array receiver by combining hardware miniaturization techniques and corresponding DBF algorithms. The preliminary simulated results of the system and its components are encouraging further investigation of this concept. Future work will focus on hardware manufacturing and validation by measurement.

Acknowledgment

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References

[1] S. Irteza, N. Murtaza, S. Caizzone, R. Stephan, M. A. Hein, “Compact planar L-band antenna arrays with optimal diversity performance” to be published in IEEE-APWC Turin 2011

[2] M. Cuntz, L. Greda, M. Heckler, A. Konovaltsev, M. Meurer, L. Kurz, G. Kappen, T.G. Noll, "GALANT - Architecture of a Real-Time Safety of Life Receiver", *Proc. ION GNSS 2009,* in Savannah, Georgia, Sept. 22-25, 2009.

[3] J. Weber, Ch. Volmer, K. Blau, R. Stephan, and M. A. Hein. Miniaturised antenna arrays using decoupling networks with realistic elements. In *IEEE Trans. Microwave Theory Tech.*, volume 54, pages 2733–2740, June 2006.