Block Distributed Schur Complement Preconditioners for CFD Computations on Many-Core Systems

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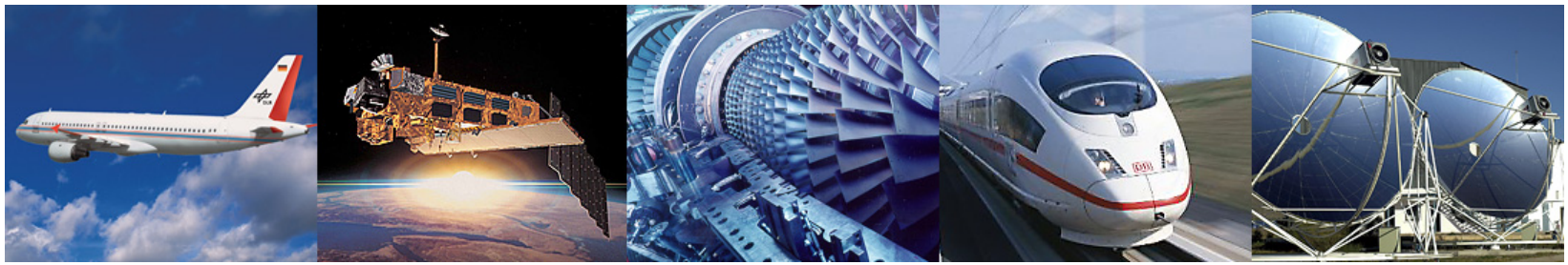
DLR
German Aerospace Center



- Research Institution
- Space Agency
- Project Management Agency

Locations and employees

Germany: 6,900 employees across 33 research institutes and facilities at

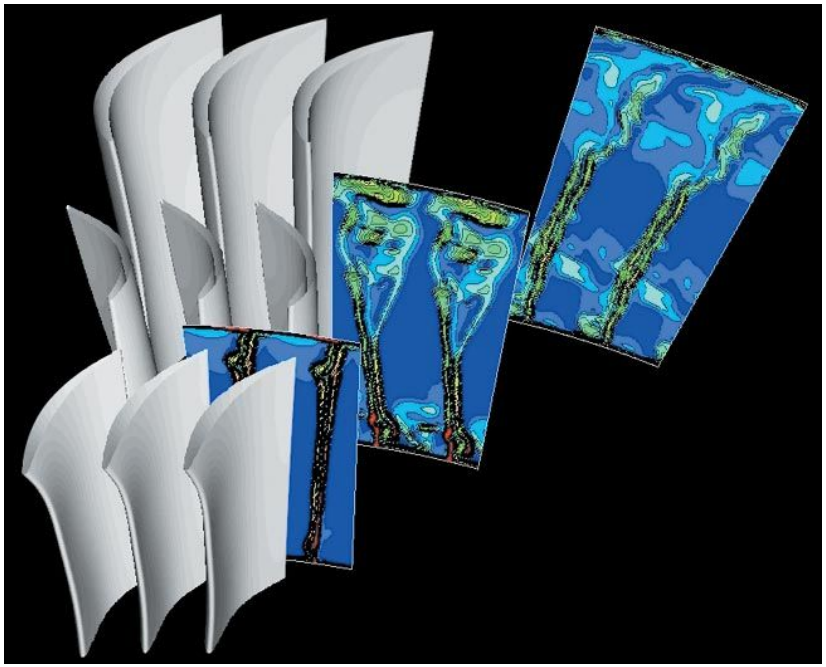
- 15 sites.

Offices in **Brussels**, **Paris** and **Washington**.

Survey

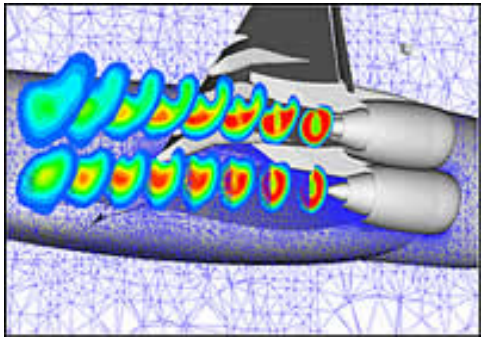
- CFD computations at DLR
- Storage schemes for sparse matrices
- The *Distributed Schur Complement* method (DSC)
- Experiments with TRACE and TAU matrices
- Conclusions and future work

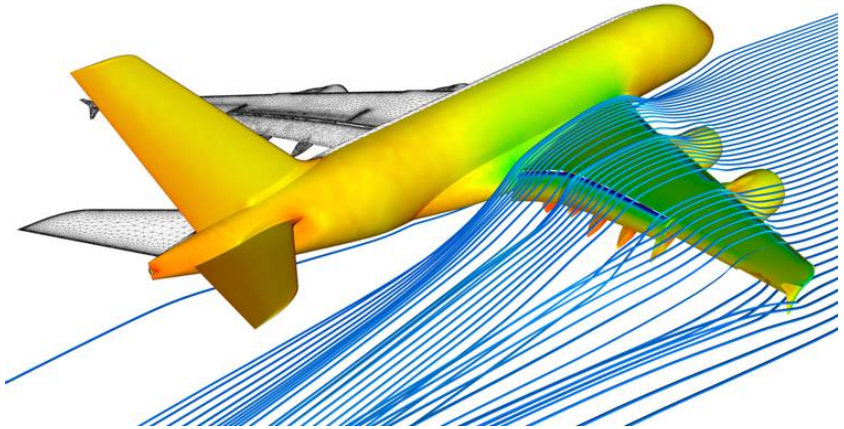
Parallel Simulation System TRACE



- TRACE: Turbo-machinery Research Aerodynamic Computational Environment
- Developed by the Institute for Propulsion Technology of the German Aerospace Center (DLR-AT)
- Calculates internal turbo-machinery flows
- Finite volume method with block-structured grids
- The linearized TRACE modules require the parallel, iterative solution with preconditioning of large, sparse, non-symmetric real or complex systems of linear equations

Preconditioners for TAU: Background





- TAU: developed for the aerodynamic design of aircrafts by the DLR Institute of Aerodynamics and Flow Technology
- Unstructured RANS solver (Reynolds-averaged Navier-Stokes), exploits finite volumes
- Requires the parallel, iterative solution with preconditioning of large, sparse, real, non-symmetric systems of linear equations
- Solvers used: geometric Multigrid, AMG preconditoned GMRes
- Here: experiments with DSC methods

Storage Schemes for Sparse Matrices

Compressed Row Storage (CSR) and Block Compressed Row Storage (BCSR)

Matrix:

1	0	0	2	0	0
0	3	4	5	0	0
0	0	0	0	6	7
0	0	0	0	8	9

Non-zero values, row-wise:

1	2	3	4	5	6	7	8	9

Column indices, row-wise:

1	4	2	3	4	5	6	5	6

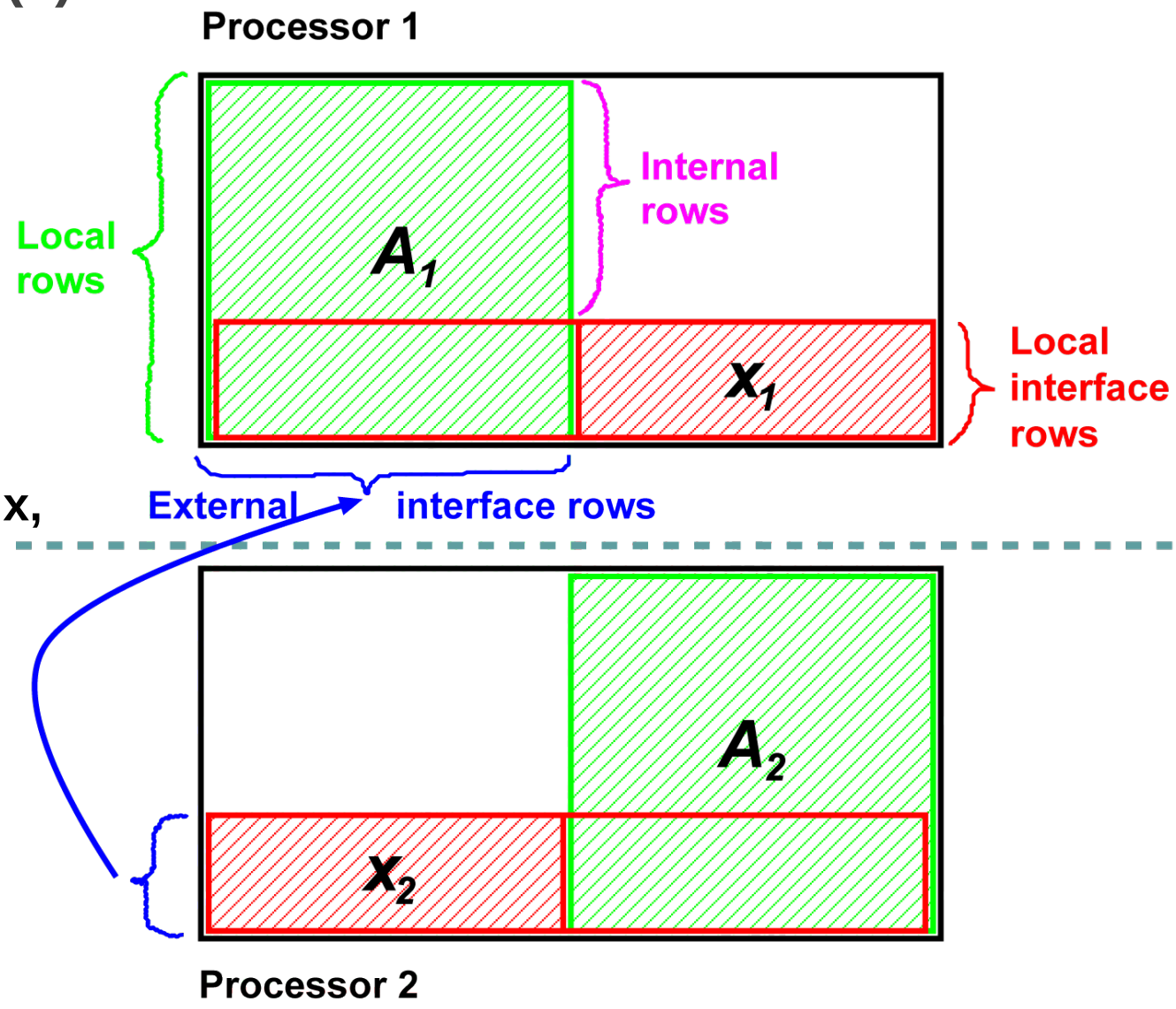
Row pointers:

1	3	6	8	10

1	0	0	2	0	0
0	3	4	5	0	0
0	0	0	0	6	7
0	0	0	0	8	9

- TRACE and TAU apply BCSR with 5x5 blocks.
- Avantage: less indirect addressing
- Disadvantage: A few zeros are stored.

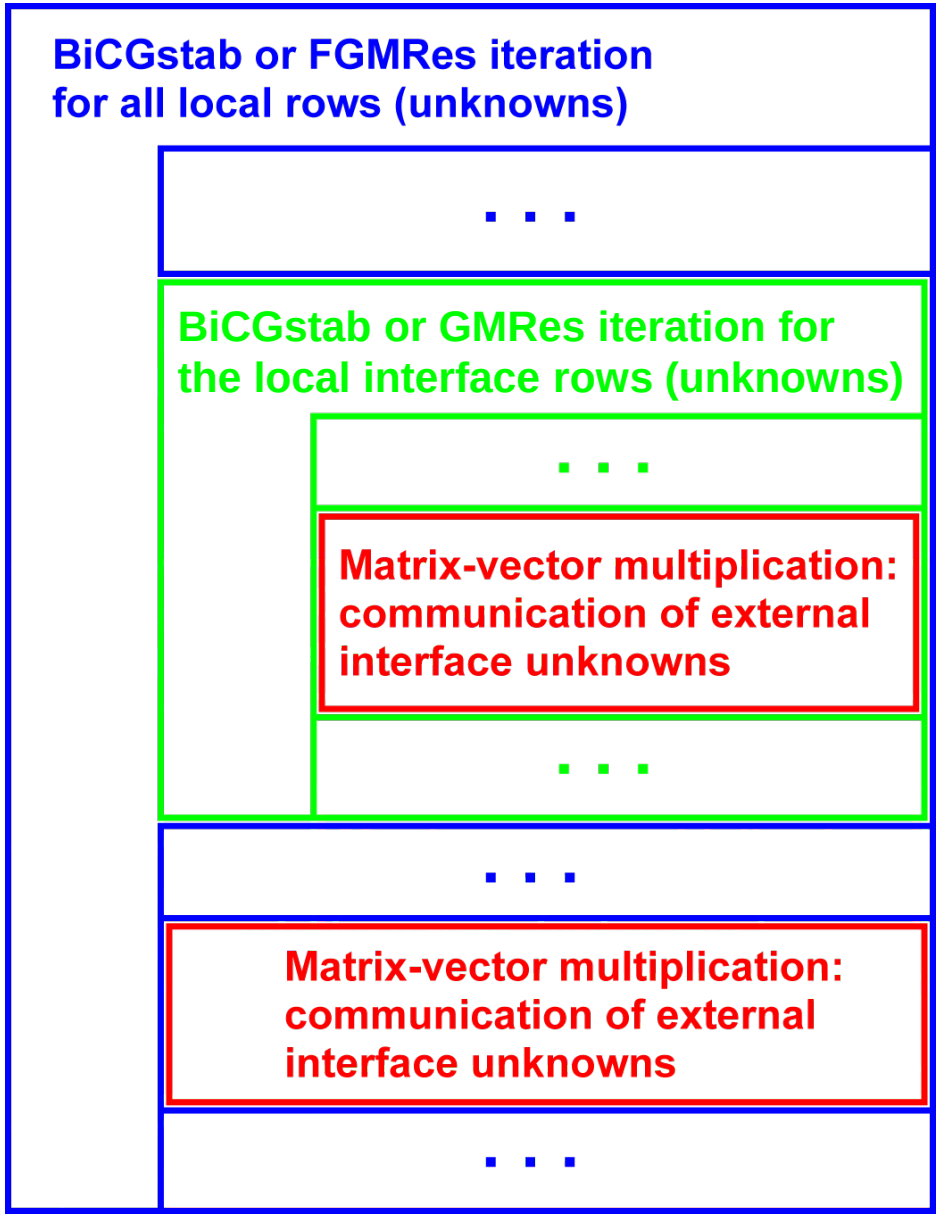
DSC Method (1)


Processor 1
Local rows
Internal rows
A_1
x_1
Local interface rows
External interface rows
Distributed matrix, 2 processors
A_2
x_2
Processor 2

DSC Method (2)

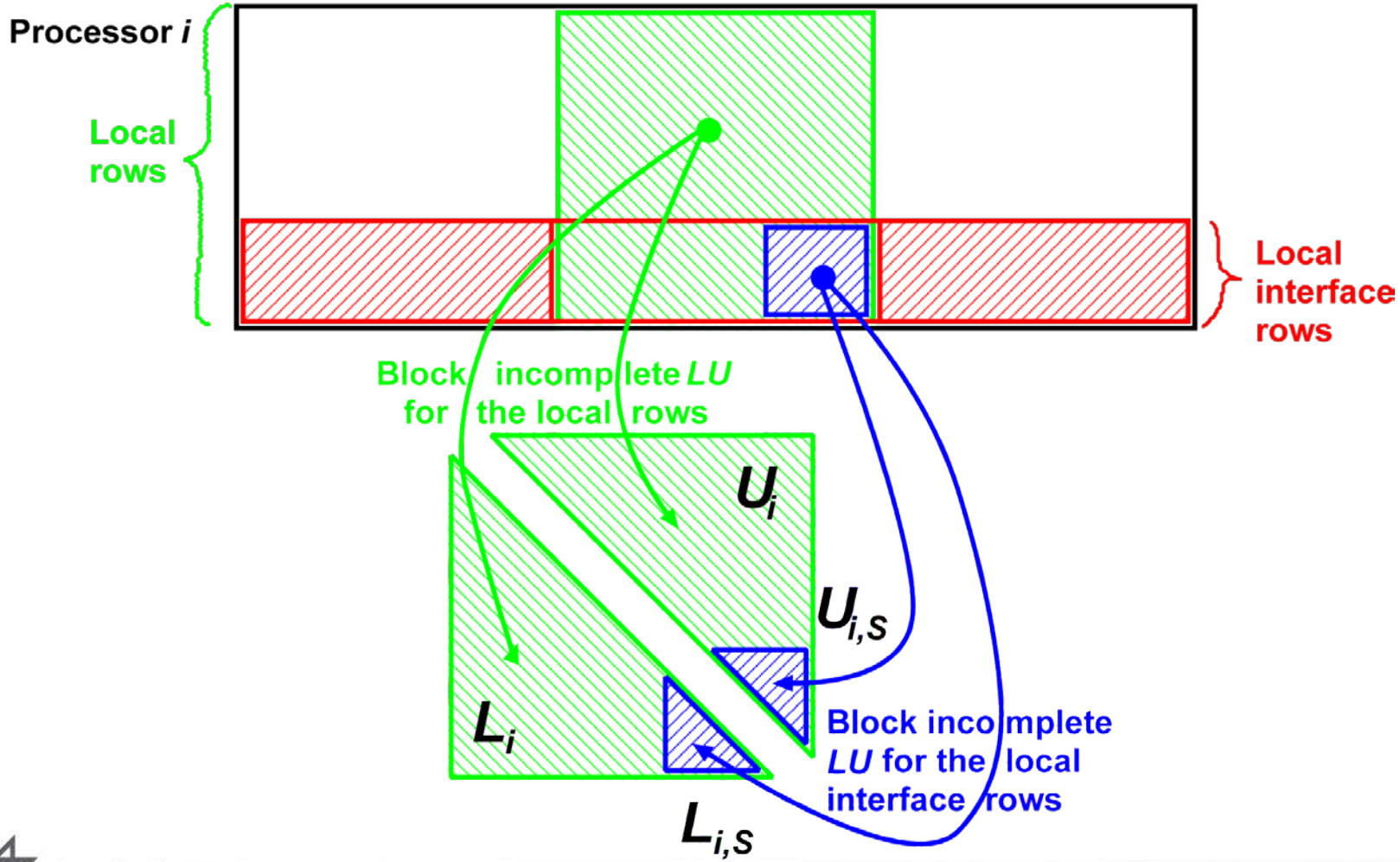
DSC Algorithm

Schematic view on each processor



DSC Method (3)

Preconditioning within the DSC algorithm



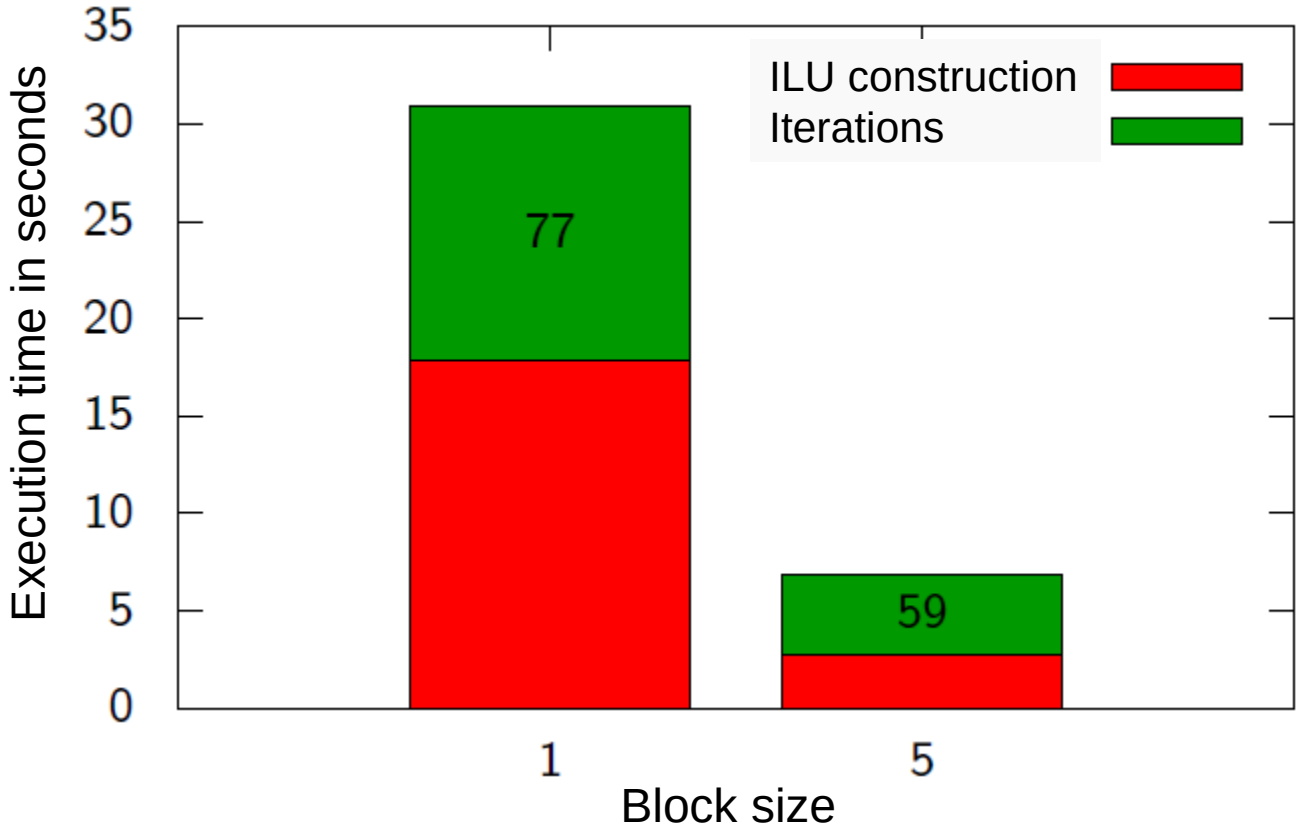
Hardware System

- **RWTH Bull HPC cluster**
  - Intel Westmere X5675 CPUs
  - 6 cores per CPU with 3.06 GHz
  - 12 cores (2 CPUs) per node
- Computations with 1 MPI process per core

Experiments: CSR versus BCSR Format

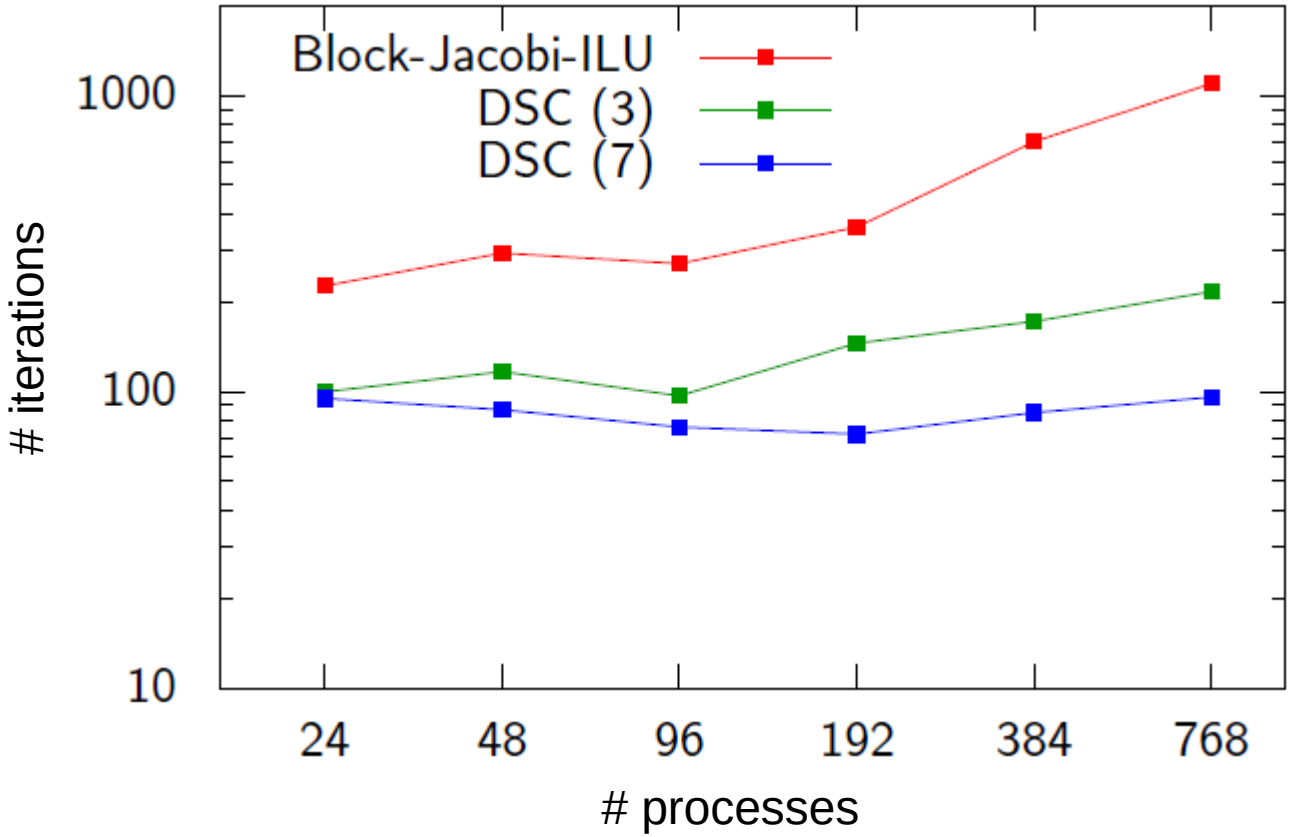
Block-Jacobi-ILU preconditioning with 12 processes

TAU matrix: n=541,980; nz=170,610,950; ILU fill-in ratio≈0.8; |rel. res.| < 10^{-5}



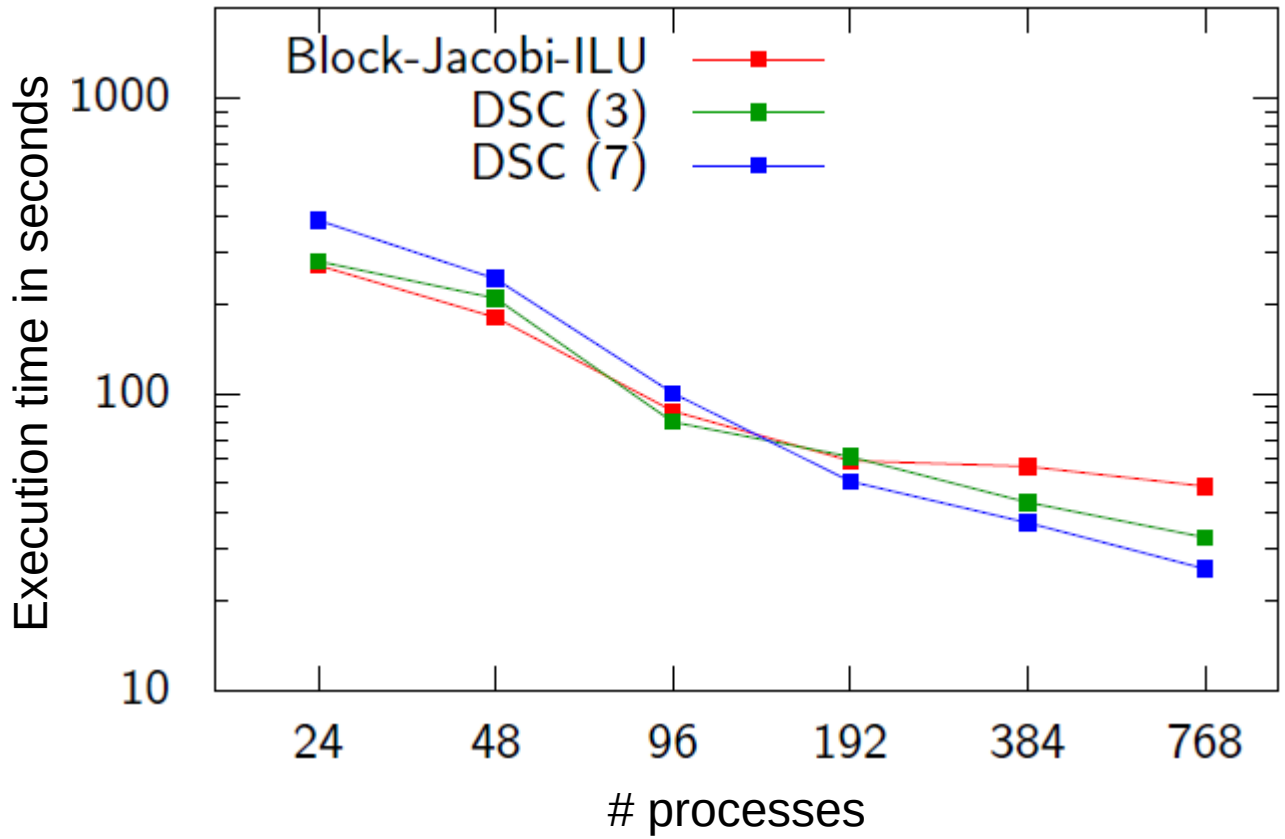
Experiments: Strong Scaling, Iterations

TRACE mat. UHBR: n=4,497,520; nz=552,324,700; threshold=$5 \cdot 10^{-4}$; |rel. res.|<10^{-5}



Experiments: Strong Scaling, Time

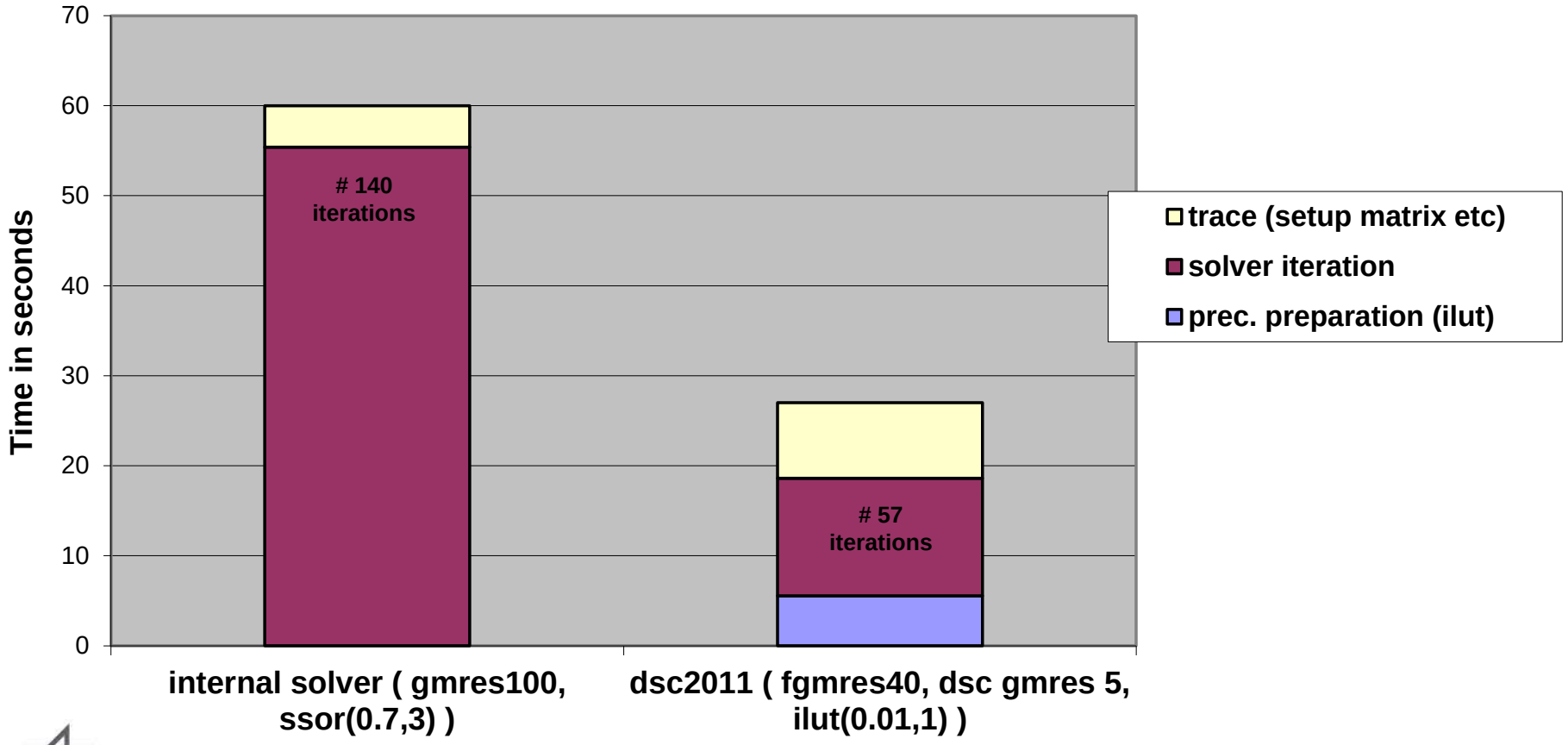
TRACE mat. UHBR: n=4,497,520; nz=552,324,700; threshold=$5 \cdot 10^{-4}$; |rel. res.|<10^{-5}



linearTRACE Performance: Internal versus DSC Solver

(2x Intel XEON E5520 with 4 cores each, 2.26 GHz)

dsc2011 solver for linearTRACE
(8 processes, test case "THD stator": dim = 0.8 Mio, nnz = 90 Mio)



Conclusions

- **BCSR format application significantly outperforms CSR format application for real TRACE and TAU problems.**
- **DSC method achieves higher scalability and faster iteration than block-local methods.**
- **DSC method very suitable for TRACE and TAU problems**

Future work

- **Hybrid parallelization is appropriate to further improve scalability.**

Questions?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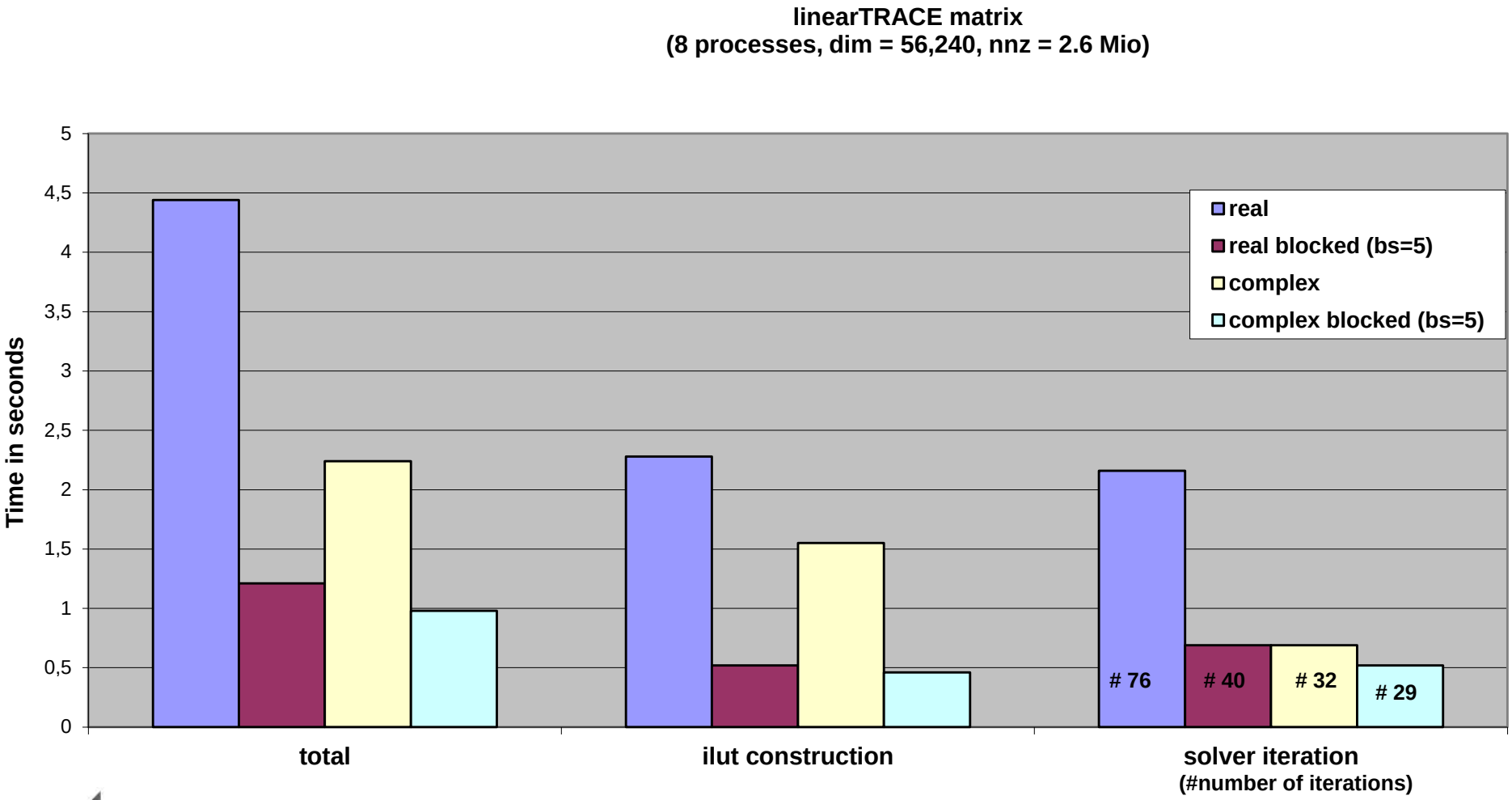
DLR
N747NA

DSC Solver: CSR versus BCSR Format

(2x Intel XEON E5520 with 4 cores each, 2.26 GHz)



DSC Method: Effect of the Interface Iteration (real)
(2x Intel XEON E5520 with 4 cores each, 2.26 GHz)

Results on 8 cores

TAU matrix:
n=541,980;
nz=170,610,950;
threshold = 10^{-3};
|rel. residual| < 10^{-7}