

## **A GNSS Prototyping Platform with Digital Beamforming Capabilities for SoL Applications**

M. Cuntz, H. Denks, A. Konovaltsev, A. Hornbostel, E. Schittler-Neves, A. Dreher  
*German Aerospace Center (DLR),  
Institute of Communications and Navigation,  
Oberpfaffenhofen, Germany, email: [manuel.cuntz@dlr.de](mailto:manuel.cuntz@dlr.de)*

Future navigation services provided by upcoming global navigation satellite systems like Galileo will require corresponding improvements on the navigation receiving systems. Therefore, the Institute of Communications and Navigation of the German Aerospace Center originated the development of a GNSS prototyping platform for development and research on navigation receivers with improved capabilities for interference and multipath mitigation by utilization of array antenna processing techniques. Interference and multipath signals can cause serious performance degradations, which cannot be tolerated for SoL applications. New digital beam-forming and signal-processing algorithms will contribute to overcome this problem by suppressing interference and multipath signals and improving the reception of useful line-of-sight satellite signals and thus enable a more accurate and reliable navigation solution. The aim is to develop a complete Safety-of-Life (SoL) receiver demonstration system which includes the whole chain including array antenna, RF front-end, digital signal processing, navigation solution and integrity assessment.

The paper presents an overview of the whole platform architecture. In its first realization the platform consists of a two times two array antenna and a subsequent four channel RF front-end for GPS/Galileo L1 signal reception. The received signals are down-converted, digitized and recorded for off-line processing. In the first part of the paper the two by two antenna array and the L1 front-end concept are discussed. Basic design issues of the front-end concerning interference robustness and low noise are pointed out. The second part of the paper introduces the architecture of the FPGA implementation, which is used to record 250 MByte of data with a data rate of 1 GByte/s. In the following, the basic digital receiver design and its implementation in an offline SW-receiver are described. Also, a possible future FPGA-implementation for real-time processing will be discussed. The next chapter provides an overview of the digital beam-forming and direction finding techniques that are used. Finally, first results are presented and an outline for the future platform development is given.