Architecture and design considerations of a mass memory module for small satellite platforms

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Abstract

The increasing number of satellites, particularly for Earth observation such as Synthetic Aperture Radar (SAR), requires efficient on-board data processing solutions due to limited downlink capacity. Addressing this, the EU Horizon Europe project SOPHOS aims to develop high-performance processing technologies focused on SAR applications in small satellites. This paper presents the SOPHOS system as a whole and details the design of a high-performance Mass Memory Module for this application. Based on a Microchip RT-PolarFire FPGA, the proposed design reaches a storage capacity of 50 Tbit and data rates up to 10 Gbit/s.
Keywords: Mass Memory, SAR, small satellite

1. Introduction

The number of satellites launched into space is growing each year [1], along with their capabilities and complexity. Earth observation satellites already provide nearly full coverage with optical sensors, and the use of Synthetic Aperture Radar (SAR) is increasing also in civilian, non-military earth observation spacecraft. As the volume of space-borne data grows, one bottleneck remains in the persistent downlink limitations. To tackle this issue, advanced on-board data processing and storage systems are needed, which must also be applicable to smaller satellites. This enables the processing and compression of SAR data on-board the satellite.

This paper presents the developments made within the EU Horizon Europe project SOPHOS, which focuses on developing technologies for high-performance on-board processing, specifically tailored for SAR applications on small satellite (SmallSat) platforms. The focus of this paper is on the design of the Mass Memory Module (MMM) developed for the SOPHOS system.

Current mass memory technologies face challenges when deployed in small satellites, mainly due to the limited storage capacity of standard SDRAMs and the lower data rates and complex handling of NAND flash devices. Scalability is further hindered by rigid internal data routing and outdated EEE component designs. Traditional MMMs for space applications can achieve high data rates and capacities, but their dependence on older components and the constraints imposed by ECSS rules applicable for traditional space PCB layout limit their adaptability for small satellite designs. Current high performance MMMs for the traditional space market such as [2] are large with a mass of over 20kg and a power consumption of over 100W, and are thus incompatible with small satellite platforms.

The SOPHOS MMM seeks to address these limitations by leveraging the increased capacity and speed of next-generation NAND Flash devices, utilizing new FPGA technology combined with high-speed interfaces, and implementing high-density placement and routing in the PCB layout.

2. The SOPHOS demonstrator

The SOPHOS demonstrator comprises a Payload Processing Module (PPM), a Mass Memory Module (MMM), and Electronic Ground Support Equipment (EGSE) that includes a SAR instrument emulator and ground segment. Fig. 1 provides an overview of the demonstrator. High data rates for payload data are achieved using 10G Ethernet interfaces, while command and control functions are managed via SpaceWire interfaces. Advanced algorithms for SAR image formation and compression are developed and optimized for the PPM to demonstrate the system's capabilities and performance.

The payload data can be selectively stored in the MMM, processed in the PPM, or transmitted to the Ground Control segment, facilitated by a routing function implemented within the MMM. This provides a flexible data path, which is required to demonstrate the defined use cases. The PPM utilizes the SpaceCloud solution designed and manufactured by Unibap [3], offering a

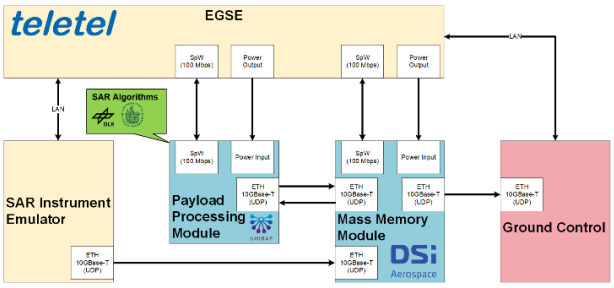

Fig. 1 Overview of SOPHOS demonstrator

cutting-edge processing architecture for on-orbit processing of large data volumes. SpaceCloud primarily relies on COTS components to meet the high computational demands, while the MMM predominantly uses qualified, space-proven, radiation-tolerant devices for reliable long-term data storage. This results in a mixed-criticality approach for the overall design.

To provide a comprehensive overview of the SOPHOS system, the following paragraphs briefly describe the applied SAR algorithms, as well as the PPM and EGSE components. The MMM is then discussed in detail in the upcoming sections.

2.1 SAR Algorithms & Optimisations

In SOPHOS, two possible algorithms are considered on the emulated instrument data: data compression and SAR image formation.

For data compression, we implement a PO-BAQ (Performance-Optimized Block-Adaptive Quantization) [4], which extends state-of-the-art BAQ by optimizing resource allocation and SAR image degradation. By exploiting a priori knowledge of SAR backscatter statistics, PO-BAQ adapts the quantization rate in the scene in order to meet a specific performance requirement (e.g., Signal-to-Quantization Noise Ratio, SQNR) in the final focused product.

The processing for on-board raw data compression involves the uplink of a bitrate allocation map (BRM, previously derived on ground); quantization of radar echoes with variable bit-rate according to the pre-defined BRM; Storing compressed data on-board and downlinking to ground for further processing.

The PO-BAQ approach enables more efficient use of downlink capacity, optimizing global performance within a given budget and increasing the system's acquisition capability for continuous observation.

An example is shown in Fig. 2(a): the bitrate map (BRM) on the left-hand side is designed to achieve a constant SQNR of 10 dB, the acquired raw data are quantized according to the given BRM, and afterwards SAR processing is carried out on ground. The resulting SAR image degradation shows a homogeneous distribution (SQNR map on the right and histogram in Fig. 2(b)), which is effectively concentrated around the target value. If, on the other hand, a constant bitrate is applied, this

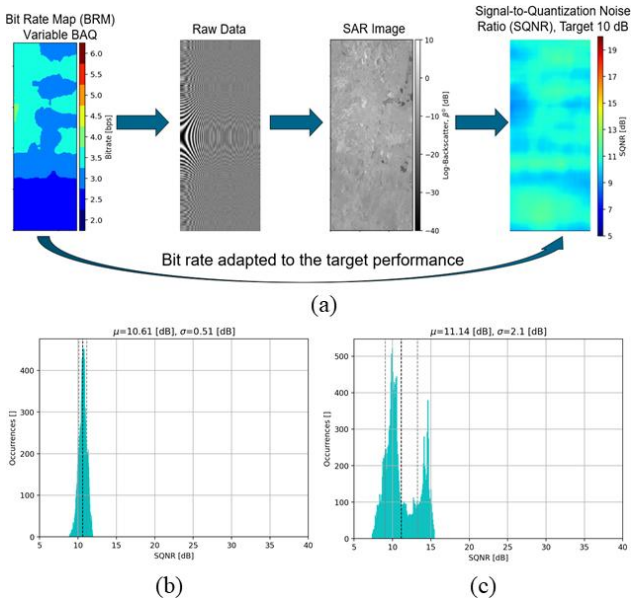

Fig. 2 (a) On the left, example of BRM applied to SAR raw data for the area shown in the middle to achieve a target SQNR of 10 dB, on the right the resulting SQNR map is depicted; (b) Distribution of the SQNR values using the BRM in (a), and (c) distribution of the SQNR values in case a constant 3-bit BAQ is used for raw data compression.

results in an inhomogeneous image degradation, as depicted in the SQNR histogram in Fig. 2(c), resulting from a compression using 3-bit BAQ.

Given the severe constraints imposed by the downlink capacity, the approach and analyses adopted in SOPHOS will help to optimize the overall global performance for a given downlink budget and, in this way, to increase the acquisition capability of the system allowing for more continuous observation.

For onboard SAR image formation, an extended wavenumber domain algorithm is selected for implementing the processing of monostatic SAR data, as shown in Fig. 3. In particular, an adaptation to the spaceborne case of the extended omega-K algorithm is selected [5], [6].

In case of oversampled data, an azimuth low-pass filter in frequency domain is used to reduce the data volume as a first stage of data reduction prior to processing, as a function of desired azimuth resolution.

The SOPHOS demonstrator is designed around 2 uses cases, “Light” and “High-End”. Table 1 shows the typical data set dimensions (Light and High-End) and the execution time for the developed Python prototype, which includes I/O, deformatting, SAR image formation in a monochromatic algorithm setup, multi-looking and storage, all performed on a single CPU core.

The SOPHOS Light case can be processed within one block on the SpaceCloud system, as sufficient RAM is

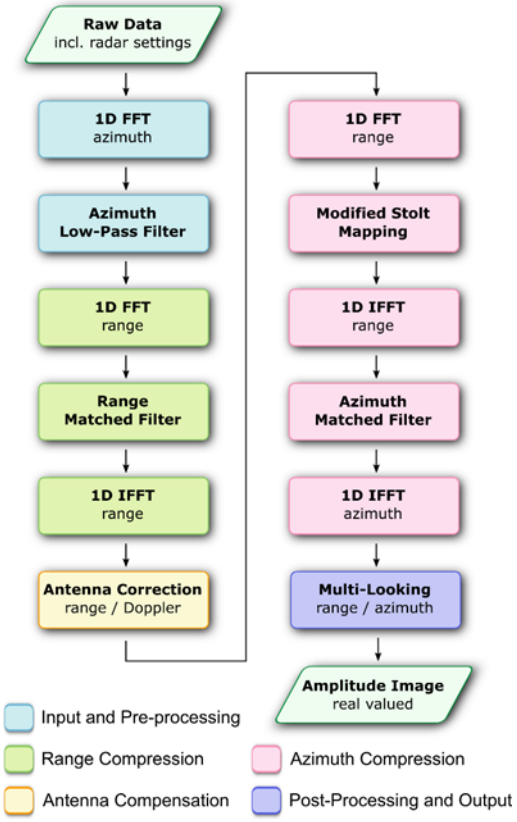

Fig. 3 Flowchart illustrating the processing for on-board SAR image formation.

available. However, the High-End case requires block-processing in azimuth. This is applicable also for larger azimuth scene dimensions, like for the Sentinel-1 (S-1) reference. In the scope of this project, only the basic algorithm for the conventional stripmap SAR mode will be optimized and benchmarked on the target SpaceCloud platform.

In SOPHOS, we focus on developing optimized data compression and image formation algorithms for both CPU and GPU architectures, aiming for portability across various spaceborne platforms. GPU work will prioritize vendor-independent frameworks like OpenCL or JAX. Both CPU and GPU performance will be enhanced through vectorization to enable near real-time operation, suitable for persistent observation scenarios. The development emphasizes robustness and avoids low-level code optimization by using self-optimizing techniques.
The accuracy of the optimized algorithms will be validated against reference results from existing Python/C prototypes. Performance improvements via vectorization will be demonstrated through runtime comparisons with these baseline implementations.

Table 1 Data dimensions for the different use cases in the SOPHOS project. For reference the numbers for a Sentinel-1 stripmap dataset are listed as well.

	SOPHOS High End	SOPHOS Light	Sentinel-1
Rows (range)	98946	31590	21838
Columns (azimuth)	38906	38880	48125
Low-Pass Dec. Factor	2	4	1
No of blocks	3	1	2
Acq. Time	7.5 sec	7.5 sec	25 sec
Proc. Time (Prototype)	410 sec	100 sec	207 sec

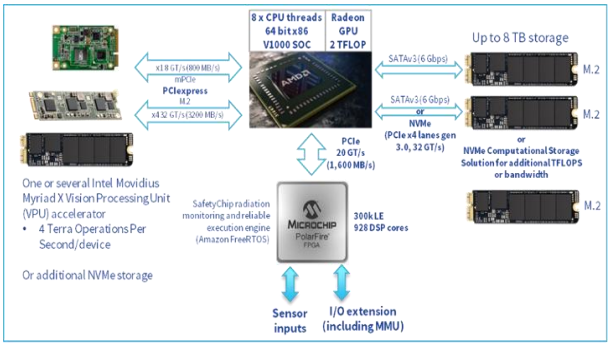

Fig. 4 Block diagram with SpaceCloud processing architectures available on iX10-101.

2.2 Payload Processing Module

The SOPHOS PPM consists of Unibap's SpaceCloud solution iX10-101. The solution is a space-qualified heterogeneous compute solution that carries the needed processing architectures to perform on-orbit processing of high data volumes by carrying a combination of different computing architectures as shown in Fig. 2. It's comprised of 6 PCB's put together in a ~1U form factor, the complete unit contains e.g.,

- AMD GPU V1000 SoC compute node,
- SpaceWire connected via PolarFire FPGA,
- 10 Gb-Ethernet connected to AMD,
- Intel Movidius MyriadX for AI applications, and
- Standard Linux for use of modern cloud enabled development tools.

The unit resides in an aluminium enclosure. The enclosure provides mechanical robustness (vibration and shock), thermal management (one sided), ease of integration (all interfaces on one side) and radiation protection. See Fig. 3 for a photo of the PPM in its enclosure.

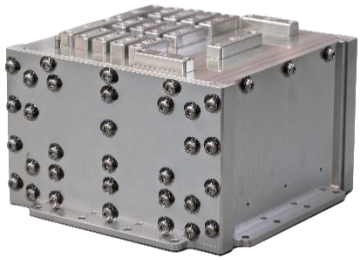

Fig. 5 The SOPHOS PPM (iX10-101)

2.3 EGSE

The SOPHOS EGSE provides the following primary functions and capabilities:

- Command and control the Mass Memory Module and the Payload Processing Module, simulating the S/C platform (e.g. On-board Computer) in terms of telemetry (TM) and telecommands (TC) communication with the payload sub-systems using SpaceWire links.
- Simulate a SAR instrument by transmitting synthetic science data (i.e. SAR raw data) from input files to the payload sub-systems using high-speed 10 Gbp/s fibre optic interfaces
- Simulate a downlink receiver by receiving and archiving high-speed telemetry downlink packets from the Mass Memory Module using high-speed 10 Gbp/s fibre optic interfaces for later offline analysis and visualisation.
- Control the different elements of the test bench to support SOPHOS test and demonstrating activities. The Ground Control System will simulate the ground segment transmitting telecommands and receiving telemetry to/from the EGSE to command and control the Payload Processing Module, the Mass Memory Module and the instrument emulator.

The Ground Control System will also include the appropriate control and data software (Central Checkout System or CCS), that will provide the required control and monitoring during end-to-end tests and measurements.

3. MMM architecture design

This section describes the architecture of the MMM for SOPHOS, including the requirements, PCB design and description of the functionality.

4.1 MMM Requirements

The high level requirements of the SOPHOS MMM are based on the specified overall system performance and the identifies use cases. The key requirements are shown in table 1.

Table 2 Excerpt from the high level requirements for the SOPHOS system targeting the MMM.

Req-ID	***Name***	***Description***
HL-REQ1	*Data Rate*	*at least **7.2 Gbit/s**.*
HL-REQ5	*Mass Memory*	*total data volume: **6 TB (48 Tbits)**.*
HL-REQ6	*Power*	*Average **power consumption** < **20W***
HL-REQ7	*Size*	*compatible with **SmallSats***
HL-REQ9	*Memory Reliability*	***mass memory** shall include EDAC mechanisms for error correction and detection*

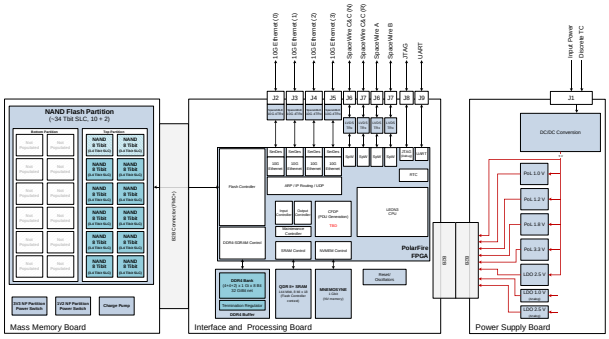

Fig. 6 Overview of the MMM architecture.

4.2 MMM HW architecture

The MMM is a non-redundant module consisting of 3 PCBs that are connected by board-to-board connectors: a Mass Memory Board (MMB), an Interface and Processing Board (IPB) and a Power Supply Board (PSB). Each of these boards is presented in more detail below. An overview of the architecture is shown in Fig. 6.

The MMB comprises the Flash memory partition for non-volatile data storage as well as the flash power switch circuitry. The data is stored on up to 24x 8 Tbit synchronous NAND Flash devices operated in SLC mode. The user capacity is scalable to up to 50 Tbit BOL by adapting the number of Flash devices. Initial performance evaluations of the MMM will be carried out using a PCB equipped with 12 x 8 Tbit NAND Flash devices.

The flash devices in use on the MMM are also part of a concurrent program at DSI to up-screen modern TLC flash devices [7].

The Interface and Processing Board (IPB) is centred around the radiation-tolerant Microchip RT-PolarFire FPGA and is equipped with DDR4-SDRAM for buffering both incoming and outgoing data. It features four high-speed 10GBase-R Ethernet interfaces utilizing

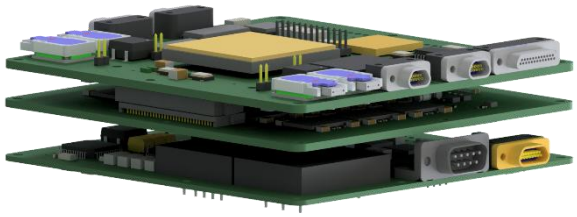

Fig. 7 PCB stack-up of the MMM.

optical transceivers, along with two SpaceWire interfaces dedicated to Command and Control. The IPB's external interfaces are designed for flexibility, allowing adaptation to customer-specific requirements for various payloads and other units. This adaptability supports a wide range of interfaces, including Ethernet, SpaceFibre, SpaceWire, proprietary SerDes protocols like WizardLink, and more.
The Power Supply Board (PSB) provides the primary and secondary power conversion for the IPB and MMB as well as overvoltage protection.

The stack-up of the three PCBs is shown in Fig. 7. The dimensions of the stack are 132 mm x 127 mm. This form factor is achieved by a high-density placement and routing, e.g. the MMB features a dual-sided design of the flash components if populated for full user capacity. To enable a unit design compliant with the requirements in small satellites, it is necessary to deviate from traditional space programs and ECSS routing and placement rules. This allows components to be placed in a much higher density layout when compared to legacy space products in Europe.
The MMM will be enclosed in a housing to provide robustness against mechanical stress as well as thermal management of the unit.

4.3 MMM functionalities
The MMM is responsible for major functionalities in the SOPHOS system: data storage, data replay and data routing.
While most data handling functionalities are implemented on the FPGA, the required boot loader and application software to control the data-chain of the MMM run on a CPU. Therefore, a soft-core LEON3FT CPU implemented in the RT-PolarFire FPGA [8].
The SpaceWire C&C interface is implemented using heritage SpaceWire IP, integrated with both nominal and redundant interfaces. The MMM's data storage functionality incorporates Error Detection and Correction (EDAC) capabilities to identify and correct bit errors, following established heritage EDAC approaches. This will include protection of buffer memory and storage memory [9].

5. MMM Design considerations
Given the constraints of current technology and design capabilities, the design of the MMM involved several key considerations to ensure the system meets its performance and functional requirements.
One such design consideration is the choice of the NAND Flash devices. SLC Raw NAND Flash has traditionally been the standard for modern spaceborne MMMs due to its high density and non-volatility. However, SLC NAND Flash devices are not evolving any more in terms of technology nodes, capacity and performance and thus cannot satisfy the storage demands of the SOPHOS MMM. To achieve the required storage capacity and throughput, the MMM uses up-screened commercial TLC 3D-NAND Flash, known for its high density and low power consumption.
While TLC NAND Flash offers very high density, its application in space has been limited due to its relatively low endurance. To address this, the NAND Flash controller operates the TLC NAND Flash in SLC mode, significantly enhancing the Flash devices' lifetime at the cost of some storage capacity. However, since the raw capacity of TLC 3D-NAND Flash devices is much greater than that of the highest-capacity planar SLC devices, even when operated in SLC mode, they still provide a significantly higher user capacity compared to traditional SLC NAND Flash solutions. In fact, SLC capacity of modern 3D-NAND is more than one order of magnitude above planar SLC NAND.
The MMM requires high-speed board-to-board interconnects that can accommodate a large number of pins in a minimal footprint in order to meet the requirement for small sized system. Traditional space-qualified connectors do not offer sufficient density for the required pin count. To address this, a VITA 57.4 FMC+ connector is used for the connection between the MMM and the IPB. This industrial connector, widely used in other markets, supports high-speed data interfaces and high-density connections, such as the wide NAND Flash bus needed for the MMM.
Another major design challenge is managing the power consumption and dissipation of the MMM. The average power is required to be under 20 W and thus at a level acceptable for SmallSat applications but one that restricts component selection. Combined with the required performance of the device, this limitation rules out the use of modern space grade SRAM-based FPGAs, which can exceed power requirements even at idle. Therefore, the Microchip RT-PolarFire FPGA was selected due to its lower power consumption, as well as its high-speed interfaces, and fabric capacity [10].
The use of high-speed interfaces requires careful attention to signal integrity. To ensure this, signal integrity simulations are carried out as the final step in the PCB routing process. These simulations have been

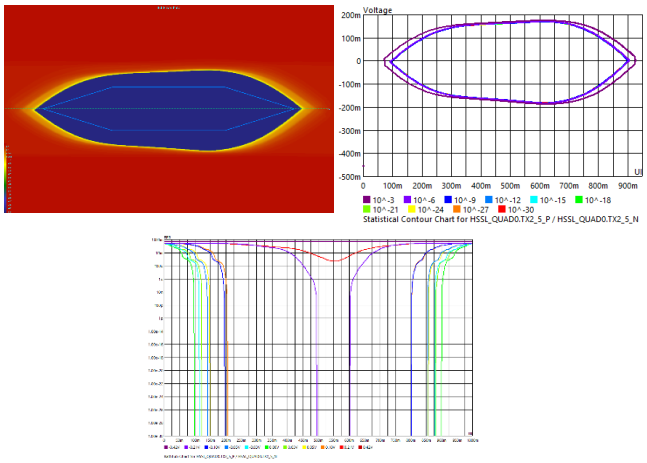

Fig. 8 Exemplary signal integrity simulation results of a SerDes TX path on the SOPHOS MMM

proven to be crucial for verifying the signal integrity of critical traces and nets on the PCB. Critical routes that undergo simulation include the DDR4 buffer memory bus, the NAND Flash bus and the SerDes interfaces to the optical transceivers. Exemplary results of these simulations are shown in Fig. 8.

6. Conclusions

This paper presents the development of a demonstrator for on-board processing of SAR data with a focus on the architecture of a novel high-performance Mass Memory Module. The demonstrator features as high-performance processing module, an EGSE including an instrument emulator, and the MMM. Data-intensive SAR algorithms are used in the test cases.

The MMM is designed to meet the requirements of high data volume satellite applications featuring up to 10 Gbit/s data throughput and up to 50 Tbit data storage capacity, while maintaining a footprint compatible with small satellites.

The key advancements of this development include the integration of a novel, high-performance radiation-tolerant FPGA, high-speed optical Ethernet interfaces, and a compact form factor achieved through high-density placement and routing. The resulting MMM represents a substantial improvement in performance compared to currently available products for small satellite platforms.

Acknowledgements

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