APPLICATION-AWARE BENCHMARKING OF NISQ HARDWARE

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DLR

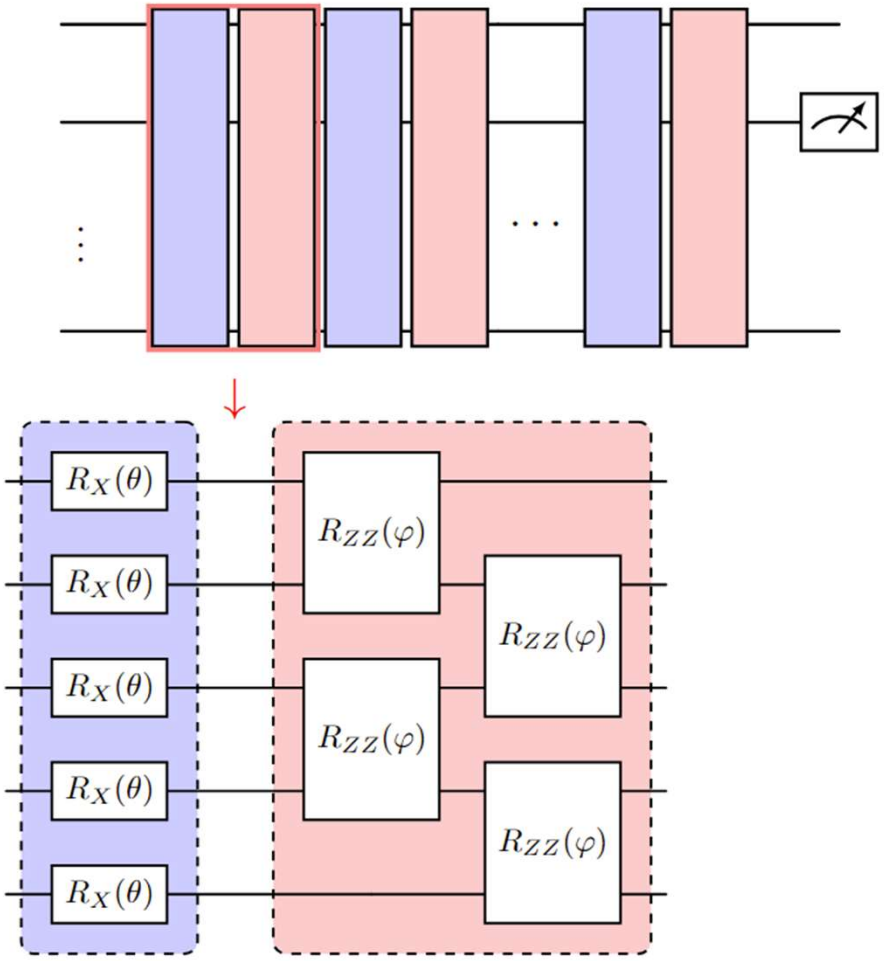
Abstract

- Inputs:
  - Quantum circuit U (application) consisting of single and two-qubit Pauli rotations
  - Pauli observable O to measure on that circuit
  - Target hardware
  - Optional: QEM method, etc.
- Aim: benchmark the fidelity $F = \langle O \rangle_{U,\text{noisy}} / \langle O \rangle_{U,\text{ideal}}$ on target hardware
- Issue: we don't know ideal value $\langle O \rangle_{U,\text{ideal}}$
- Output:
  - Family of Clifford benchmarking circuits V_i such that

$$\frac{\langle O \rangle_{V_i,\text{noisy}}}{\langle O \rangle_{V_i,\text{ideal}}} \approx F$$

arXiv: 2410.01505

Example application: quantum simulation of kicked-Ising model



$$H = -J \sum_{\langle i,j \rangle} Z_i Z_j + h \sum_i X_i$$

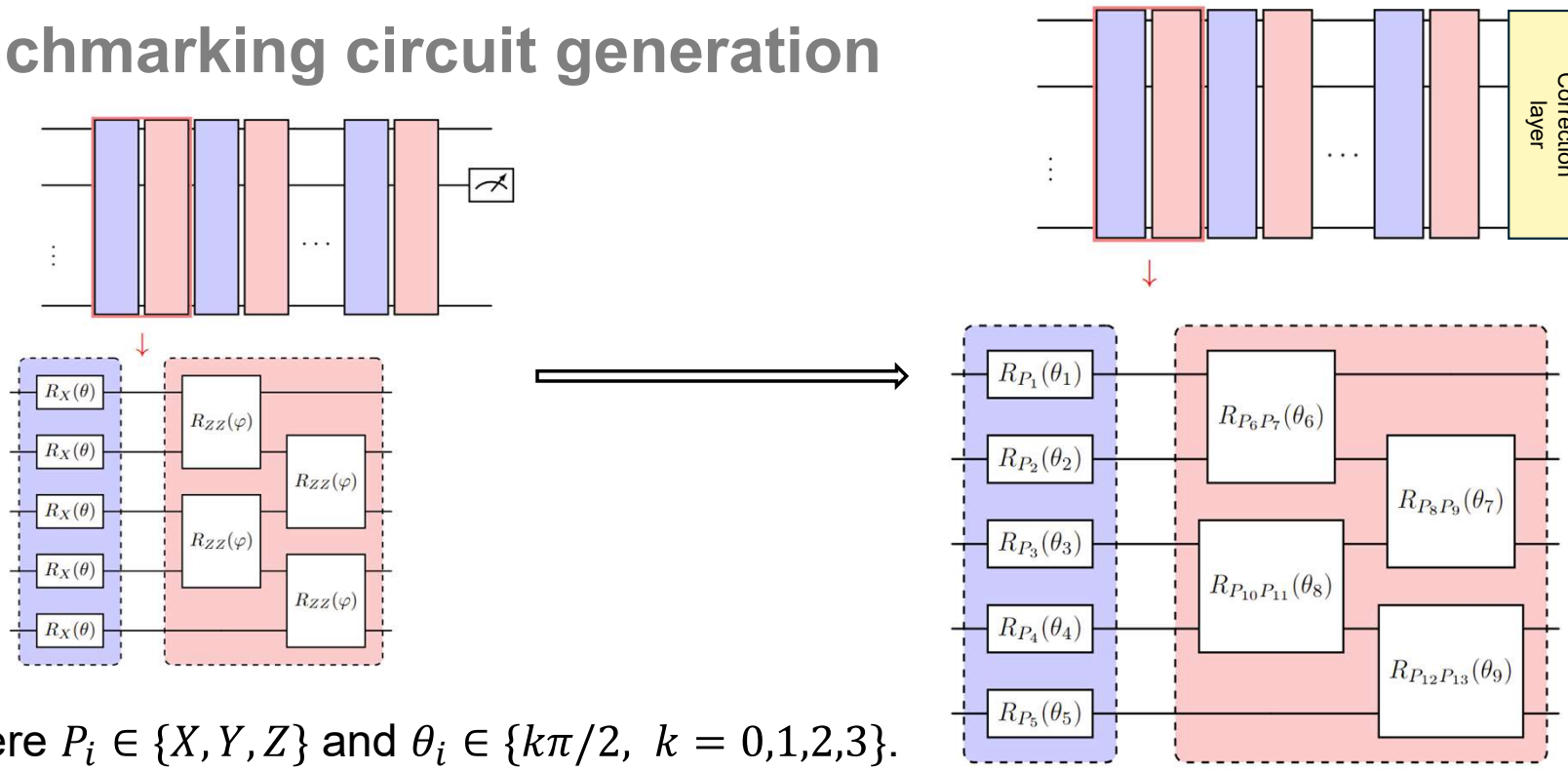
$$\Downarrow$$

$$e^{-iHt} = [L_2 L_1]^n + \mathcal{O}\left(\frac{t^2}{n}\right)$$

- Circuit consists of repeated Trotter layers
- Layers consist of single and two-qubit Pauli rotation gates
- Z measurement on single qubit

arXiv: 2410.01505

Benchmarking circuit generation



where $P_i \in \{X, Y, Z\}$ and $\theta_i \in \{k\pi/2,\ k = 0,1,2,3\}$.

- Pick Paulis P_i such that output state is a known product state of Pauli eigenstates
- Apply 'correction layer' of single qubit gates to move state to $+1$-eigenstate of O, then $\langle O \rangle_{V_i,\text{ideal}} = 1$ and $\langle O \rangle_{V_i,\text{noisy}} \approx F$
- Requirement: benchmarking circuit and application circuit have same error behaviour when running on hardware

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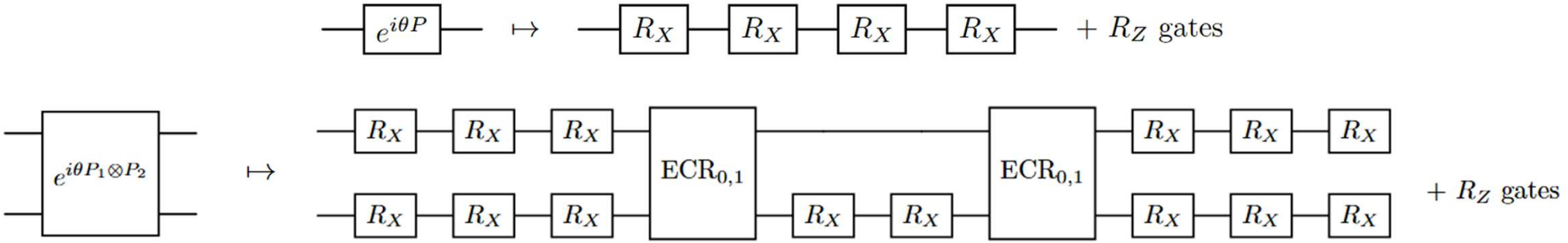
Rigid compilation rules for specific hardware

- We impose rigid compilation rules on Pauli rotations to keep circuit structure consistent
- E.g. IBM hardware has basis gates set $\{\sqrt{X}, X, R_Z(\theta), ECR\}$, where $R_Z(\theta)$ is error-free [1]



where each $R_X \in \{\sqrt{X}, X\}$

- Possible assumptions:
  - Similar error for all single-qubit gates
  - Two-qubit gate error $\gg$ single-qubit gate error

[1] Efficient Z-Gates for Quantum Computing, McKay et al., Phys. Rev. A 96, 022330

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[Cliffordise, compile] or [compile, Cliffordise]?

- Can benchmark generic circuits (not just Pauli rotations) by first compiling to hardware, then Cliffordising
- E.g. IBM hardware has basis gate set $\{ECR, X, \sqrt{X}, R_z(\theta)\}$, so can Cliffordise by setting each R_z rotation angle to nearest multiple of $\frac{\pi}{2}$
- Also useful but less control over $\langle O \rangle_{\text{ideal}}$
- IBM recently announced *Noisy Estimation Analyser Tool (NEAT)* which does this (`qiskit_ibm_runtime.debug_tools.Neat`)

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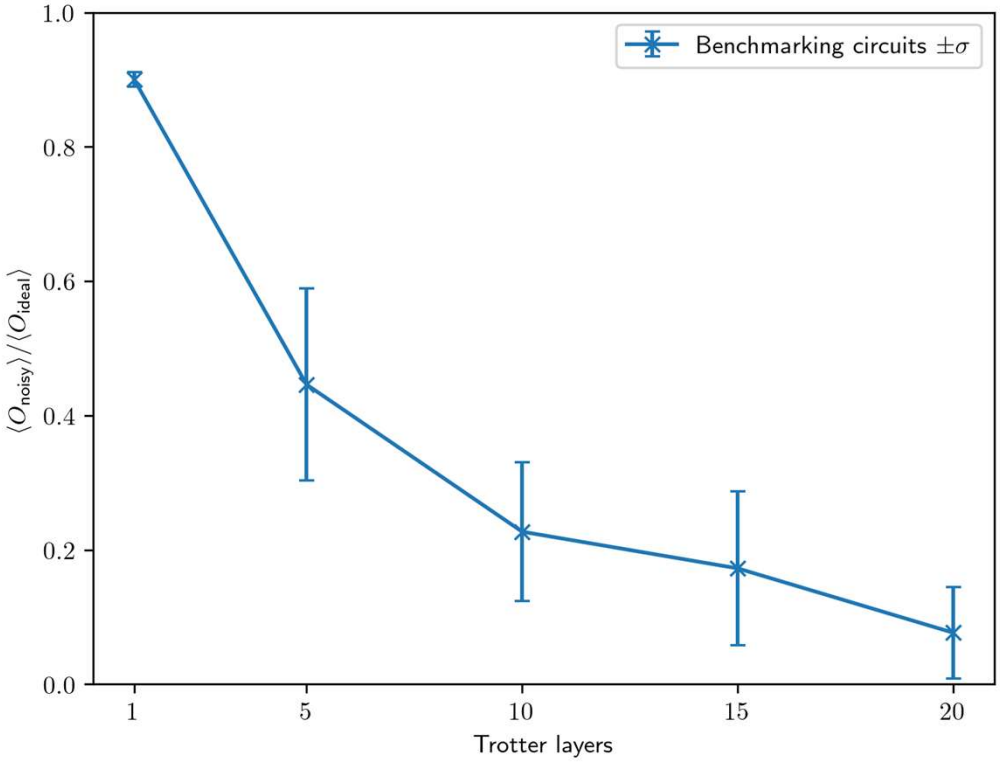
Demonstration on hardware (no QEM)



- Results from `ibm_brisbane` with 16 qubits
- 10 benchmarking circuits per datapoint

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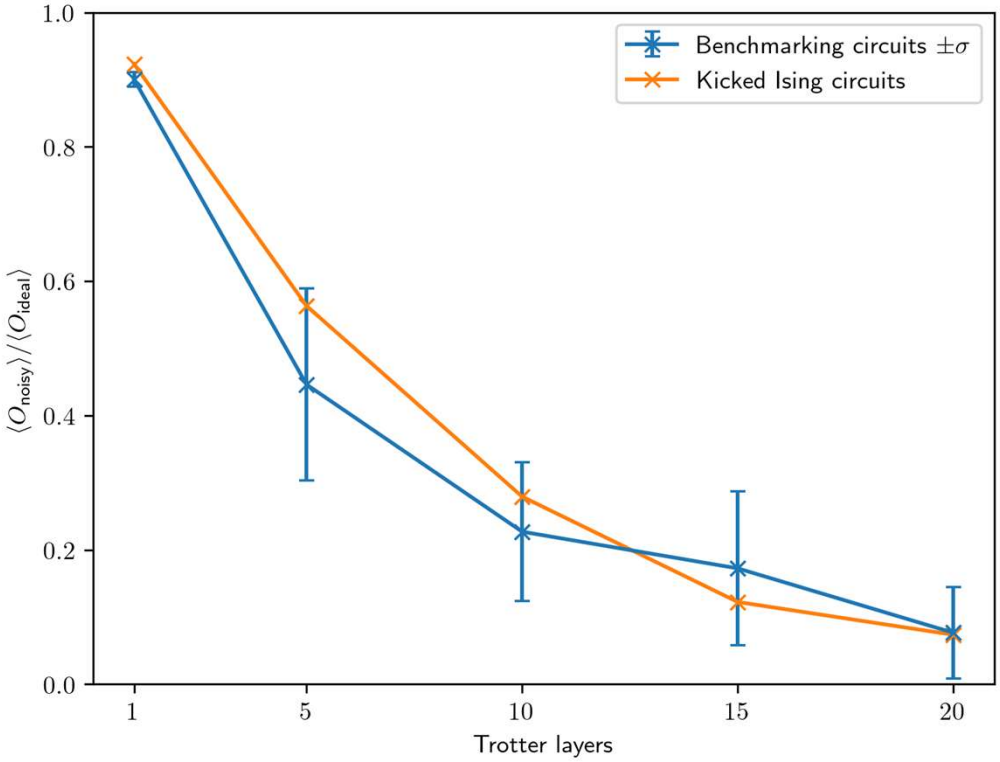
Demonstration on hardware (no QEM)



- Results from `ibm_brisbane` with 16 qubits
- 10 benchmarking circuits per datapoint
- 1 application circuit per datapoint

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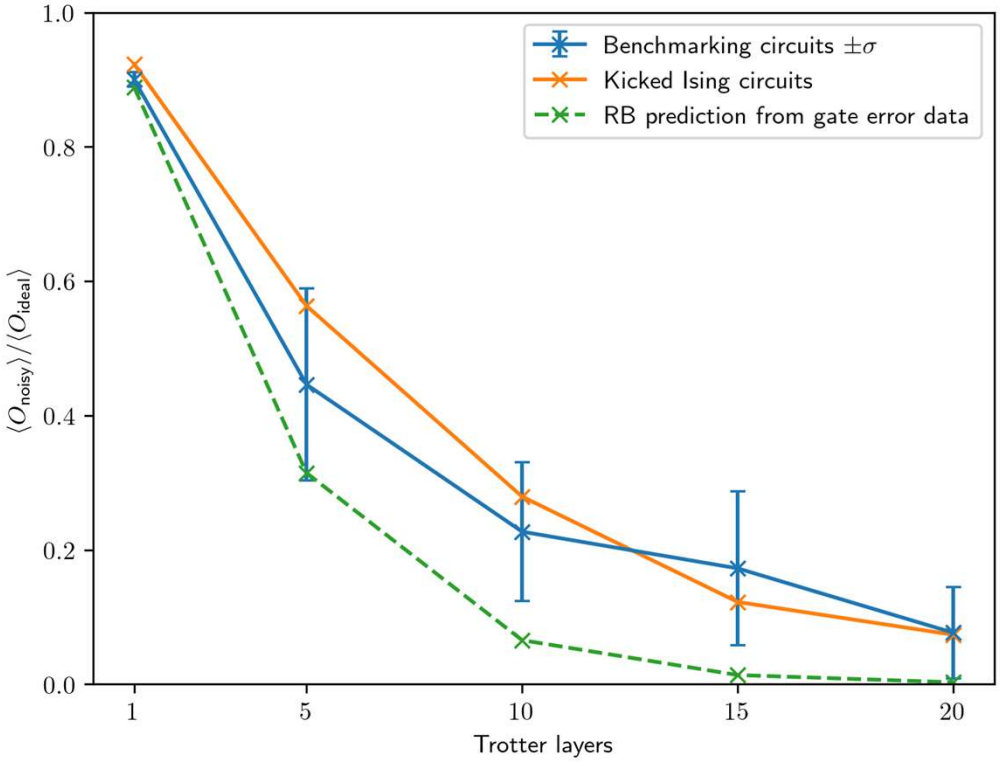
Demonstration on hardware (no QEM)



- Results from `ibm_brisbane` with 16 qubits
- 10 benchmarking circuits per datapoint
- 1 application circuit per datapoint
- RB prediction from live gate error rates

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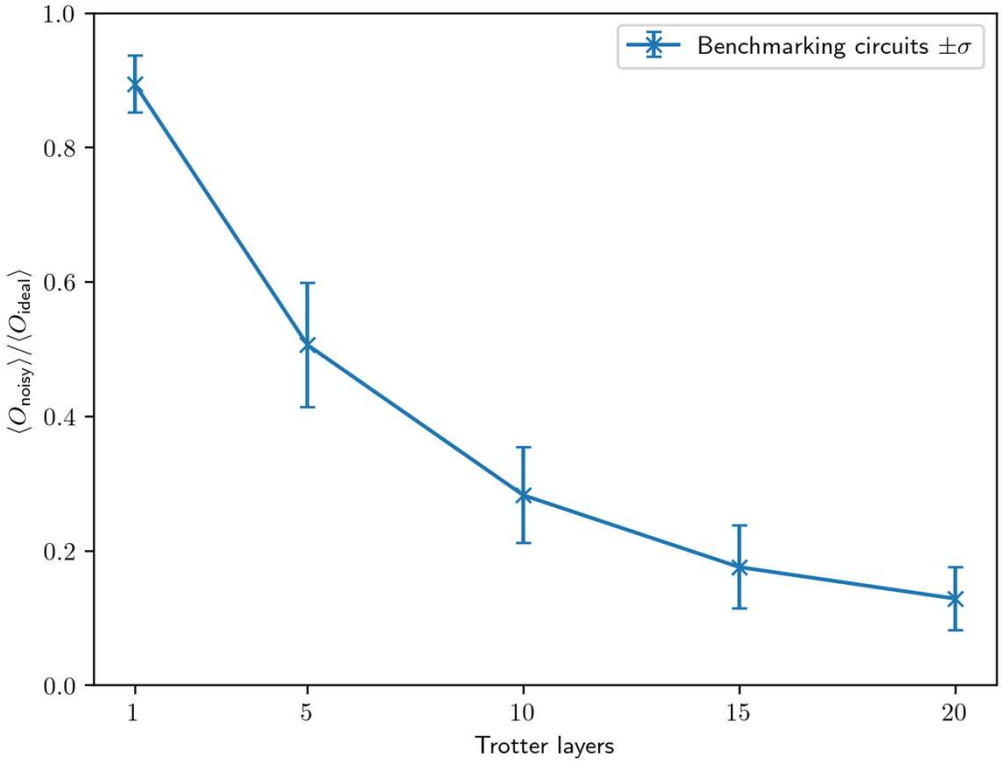
Demonstration on hardware (no QEM)



- Results from `ibm_brisbane` with 127 qubits
- 10 benchmarking circuits per datapoint

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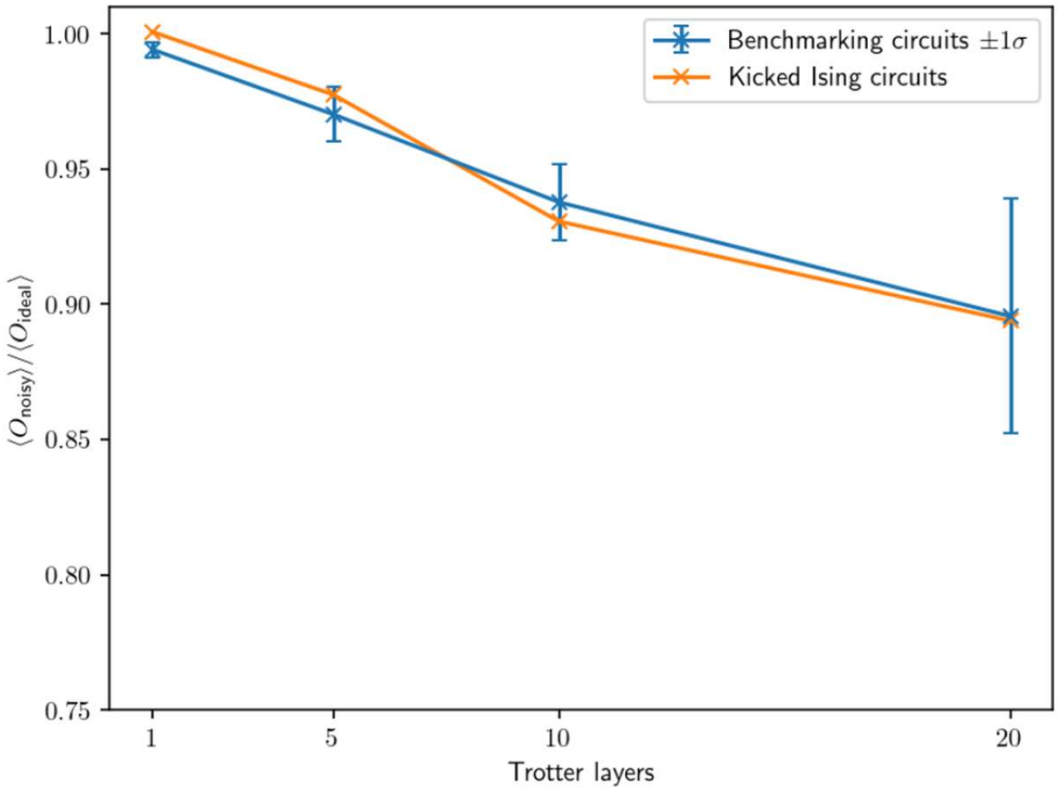
Benchmarking QEM methods



- 10-qubit noisy simulation using ZNE + Pauli twirling
- Gate-wise depolarising noise
- 10 benchmarking circuits, 1 kicked Ising circuit per datapoint
- 3 amplified noise levels (1,3,5) per circuit
- 25 Pauli twirling repetitions per noise level

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Thanks!

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