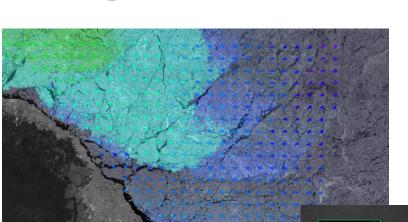
# Sea Ice Classification Using Edge Al for Synthetic Aperture Radar Satellite On-board Image Processing

**Dominik Günzel and Stefan Wiehle** 

Remote Sensing Technology Institute, German Aerospace Center (DLR)

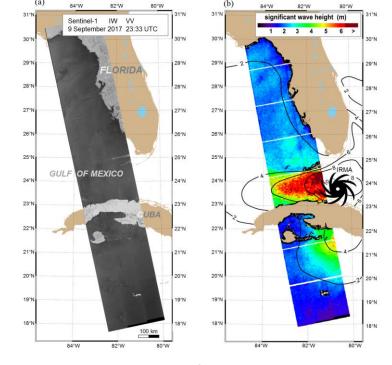


## Background

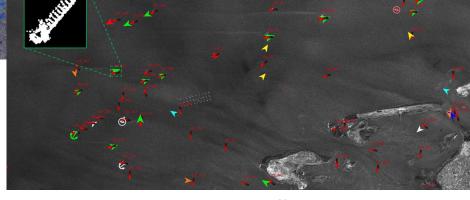


32'30'
33'15'
33'30'
33'45'
34'00'
Oil spill

DLR



Sea ice drift



Maritime traffic

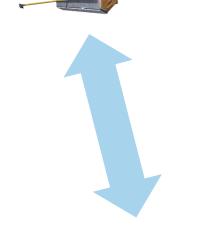
Wind speed & wave height

- State of the oceans changes constantly
- Satellite images record a point in time
- Derived information decays rapidly

### **Satellite Data Downlink**



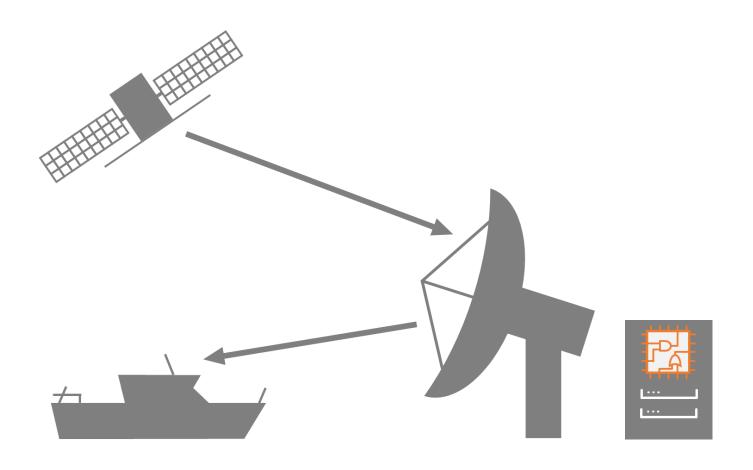
Data acquisition Continue flight Data transfer to ground station



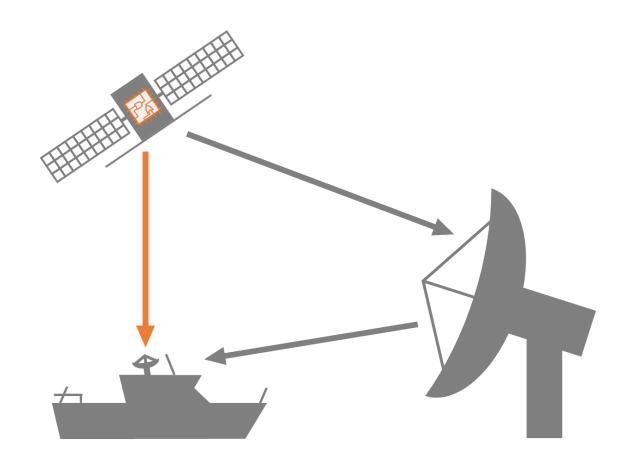


Significant delay between acquisition and product delivery





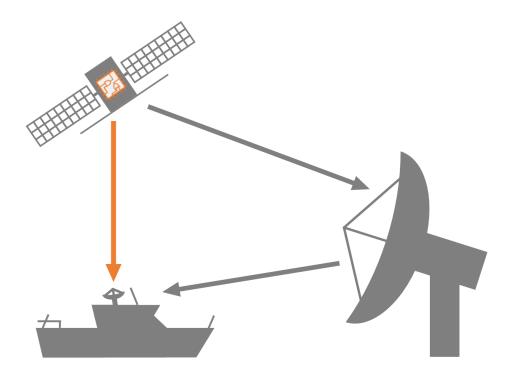






#### **On-board Data Processing**

- Processing can begin right after acquisition
- Data volume significantly reduced
- Enables direct down-link to user (lower data rate required)
- Conventional down-link of full data still possible



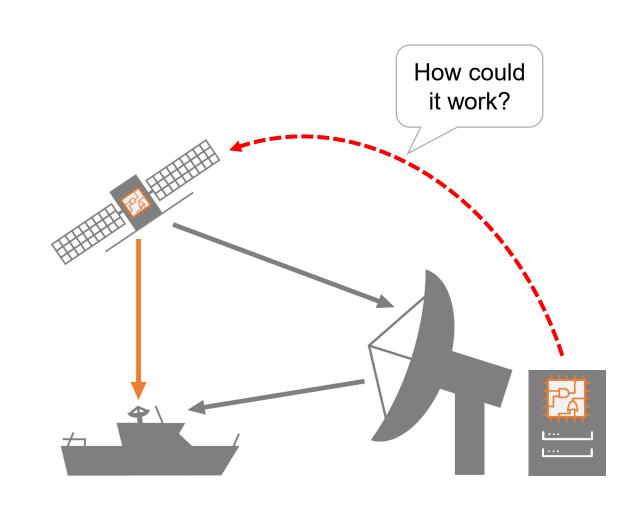


#### **Necessary Steps**

- SAR acquisition
- Raw data focusing
- Information extraction
- Down-link

#### **On-board Constraints**

- Size, weight and power (SWaP)
- Radiation
- Technological
- Security





## A network of excellence for distributed, efficient and scalable Al at the edge

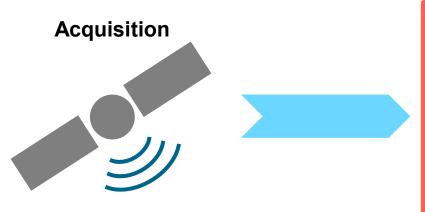


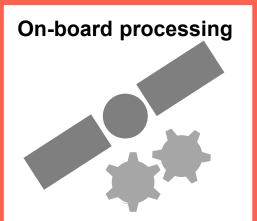
### **Edge Al for Satellite On-board Image Processing**

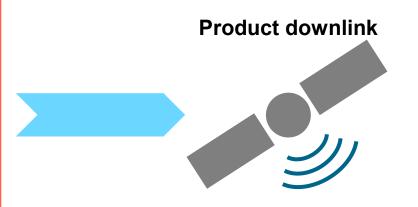
- Implementation of (ground-based) demonstrator
- Application: Sea ice classification on Synthetic Aperture Radar (SAR) data
- Hardware comparable to satellite on-board devices

This project has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement No. 101120726









## **Prototype Hardware**



Multi-Processor System-On-Chip (MPSoC)

AMD Zynq UltraScale+ ZU19EG

**Programmable Logic (PL)** 

FPGA 16nm FinFET+, 6.2M ASIC gates capacity; 5 GB DDR4

**Processing System (PS)** 

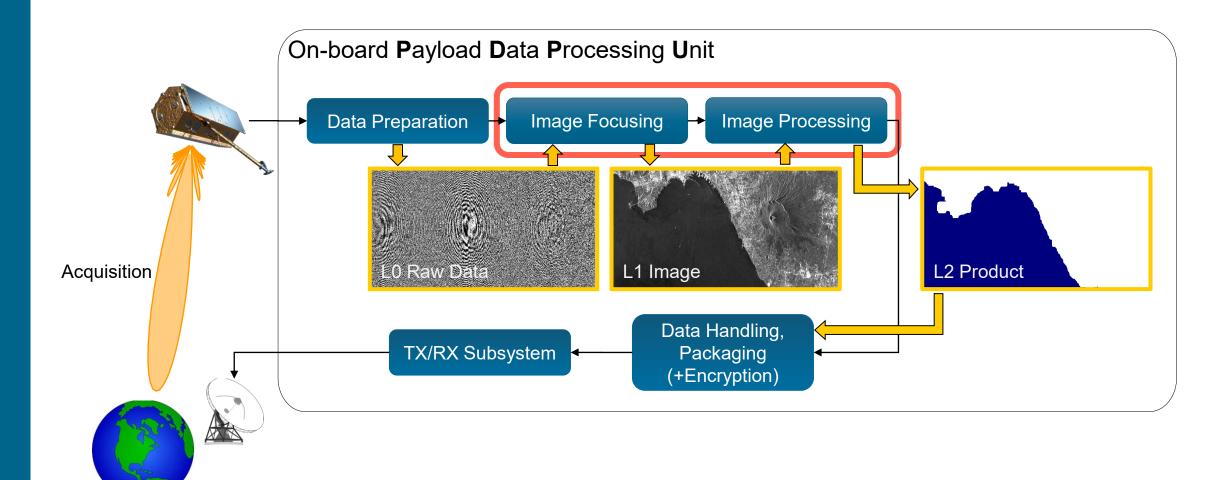
Quad-core ARM Cortex-A53 CPU @ 1.2 GHz; 4 GB DDR4



Siemens Veloce proFPGA modular board

## **SAR On-board Processing Chain**



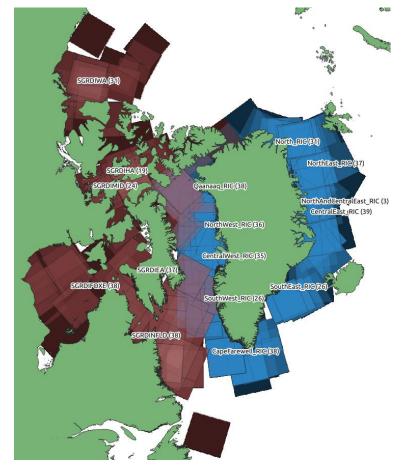


#### **Sea Ice Dataset**



#### **Al4Arctic Challenge Dataset**

- 533 manually labelled scenes
  - Canadian Ice Service
  - Danish Meteorological Institute
- Input data:
  - Sentinel-1 EW dual-pol (HH & HV)
  - SAR incidence angles grid
  - AMSR2 temperature data
  - ERA5 weather data
  - Distance to land
- Reference maps:
  - SIC: Total Sea Ice Concentration
  - SOD: Ice Stage of Development
  - FLOE: Floe size



Coverage of the Al4Arctic Dataset\*

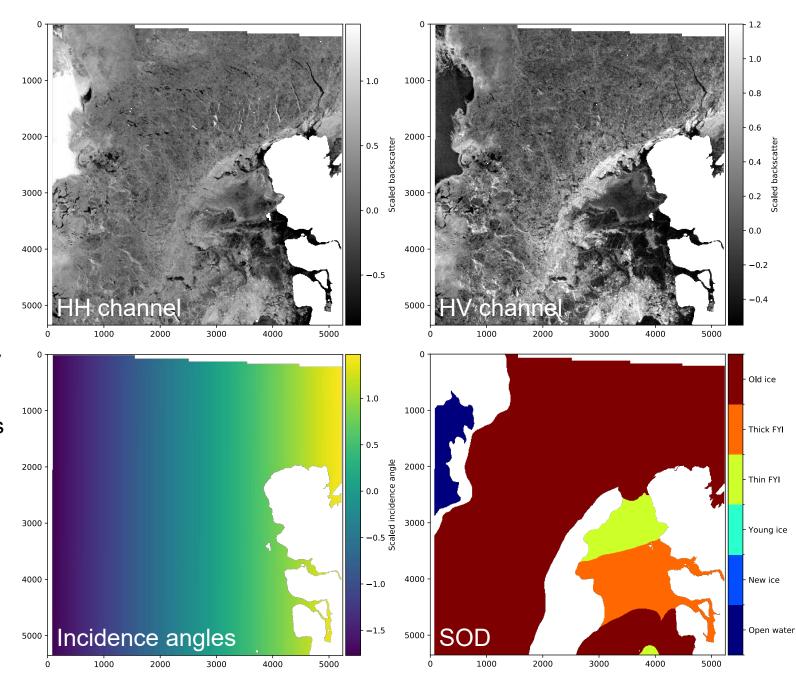
### Sea Ice Classifier

#### U-Net

- VGG13 encoder
- Input size 512 x 512 pixels
- 18.4 mil parameters
- PyTorch framework

#### Inputs

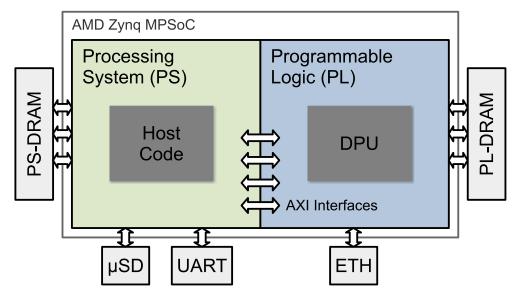
- Sentinel-1 EW dual-pol HH & HV
- Incidence angle of each pixel
- ➤ Sliced into 512 x 512 px. patches
- Output: Segmentation map
  - Stage of Development (SOD)
  - Proxy for ice thickness
  - 6 classes



## **CNN Implementation on MPSoC**



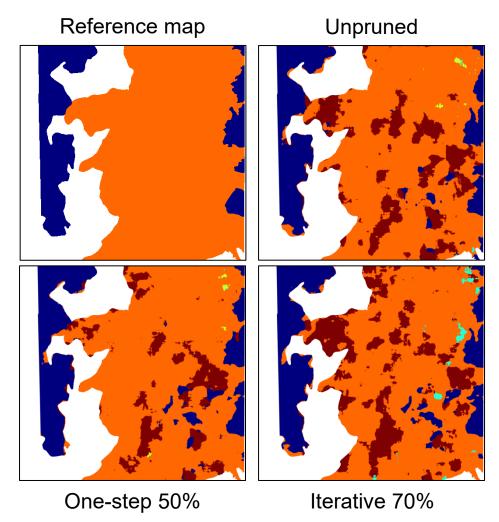
- AMD Deep Learning Processor Unit (DPU) for Zynq UltraScale+
  - Implemented in PL logic
  - Offers set of common operators
  - Programmed via Python/C++ API
- Vitis Al toolchain for model porting
  - Inspection
  - Pruning
  - Quantization
  - Compilation



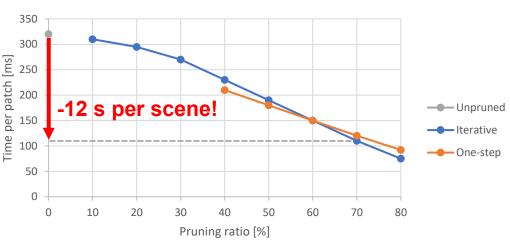
DPU integration on AMD Zynq MPSoC

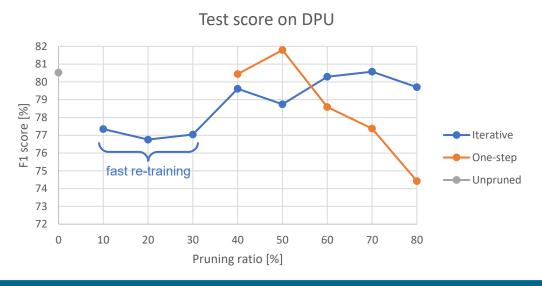
## **Model Pruning**

## Pruned Model Inference Time on DPU DLR





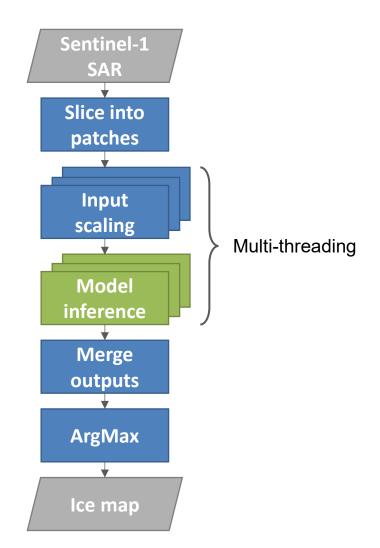




One-step pruning F1 score degraded rapidly at >50% sparsity, where iterative pruning maintained high score

## **On-board Integration**





- Model inference on PL (FPGA)
  - Multi-core DPU execution
- Pre- and post-processing on PS (ARM CPU)
  - Slicing into patches
  - Input scaling
  - Merging inference results
  - ArgMax to find dominant class

MPSoC inference steps

## Results (1)



Old ice

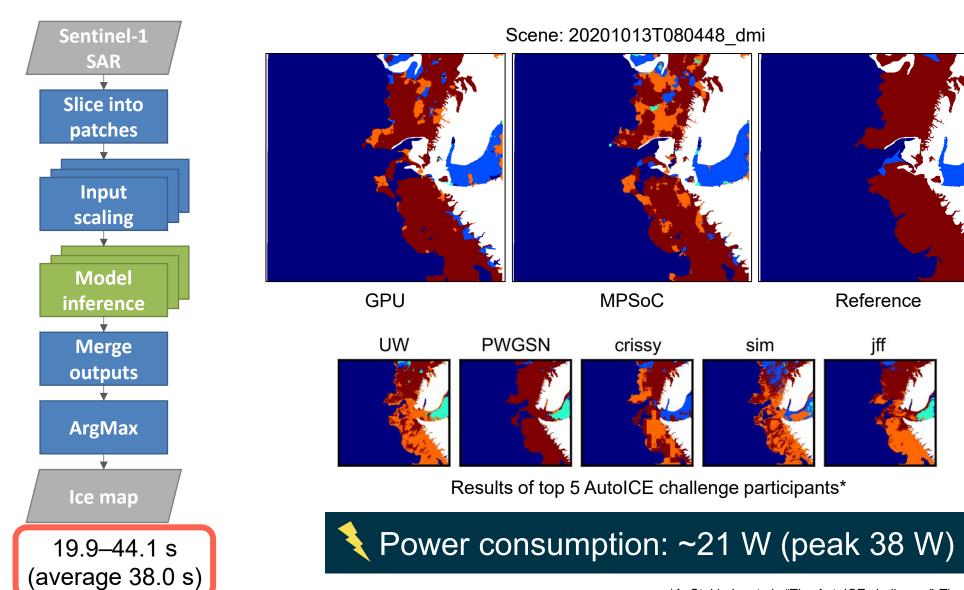
Thick FYI

Thin FYI

Young ice

New Ice

Open water



## Results (2)



Old ice

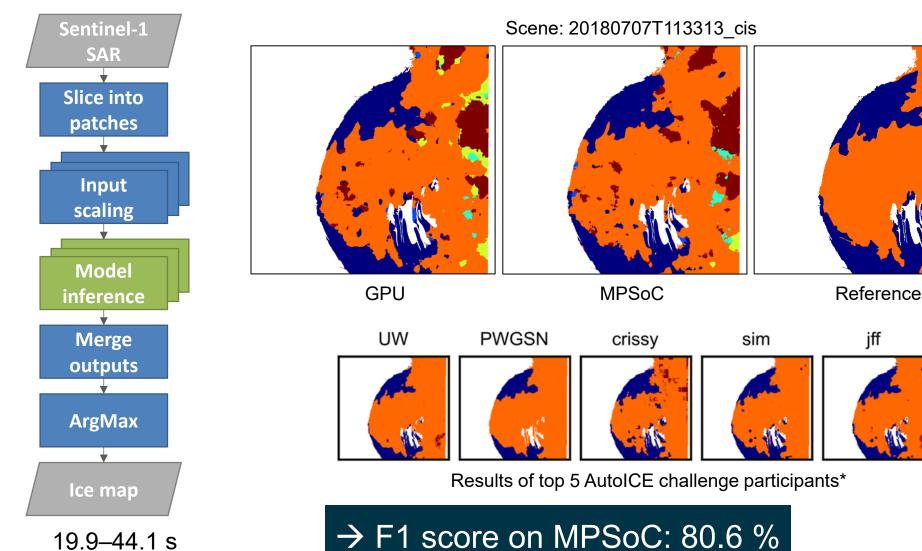
Thick FYI

Thin FYI

Young ice

- New Ice

Open water



Results of top 5 AutoICE challenge participants\*

→ F1 score on MPSoC: 80.6 %

(average 38.0 s)

#### Conclusion

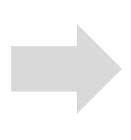


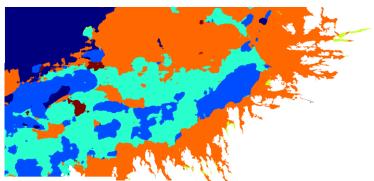
#### **On-board SAR Processing Chain**

Sentinel-1 TOPSAR Image Focusing

Edge Al Use Case: Sea Ice







- Enable near real-time product delivery
- Can be ported to hardware for low Earth orbit
- Possible implementation in future missions?



## Maritime Safety and Security Lab Bremen



#### **Recent Publications**







daiedge.eu

in dAIEDGE

This project has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement No. 101120726



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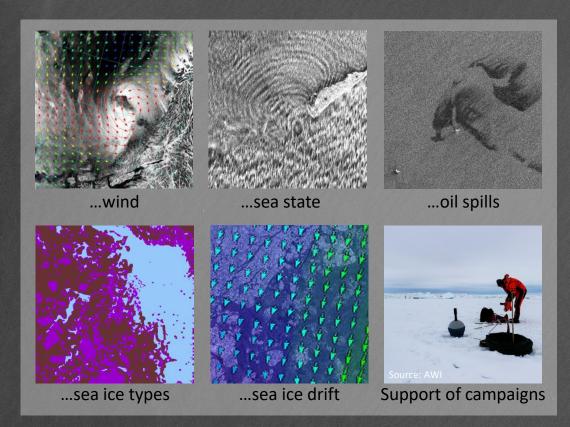
**German Aerospace Center (DLR)** 

Remote Sensing Technology Institute | SAR Signal Processing Maritime Safety and Security Lab Bremen | Germany

## Maritime Safety and Security Lab Bremen



Development of algorithms to derive maritime information from spaceborne SAR data in near real-time on...





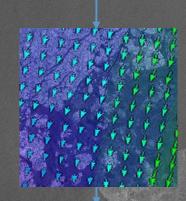


TerraSAR-X

Sentinel-1



Downlink at DLR ground segment Neustrelitz



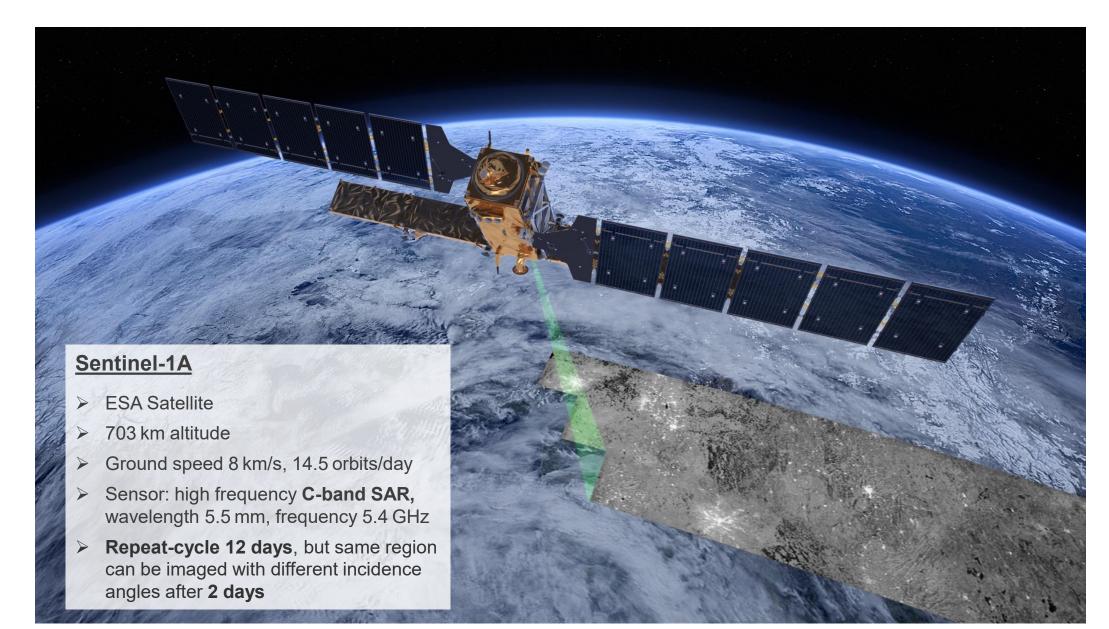
LO processing and value adding

Delivery in NRT



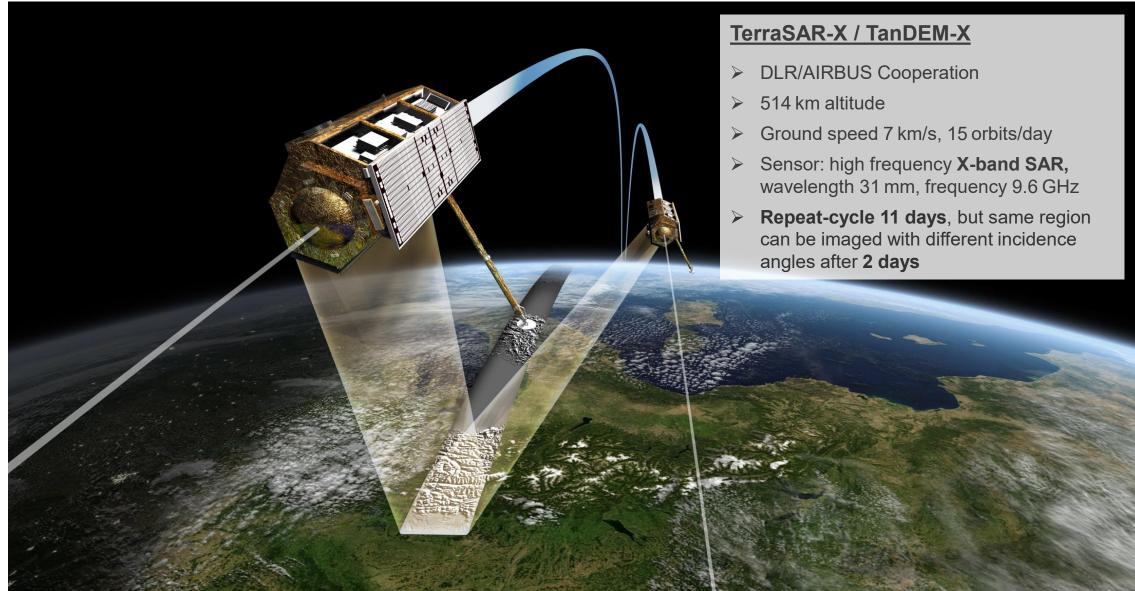
### **SAR Satellites: C-band**





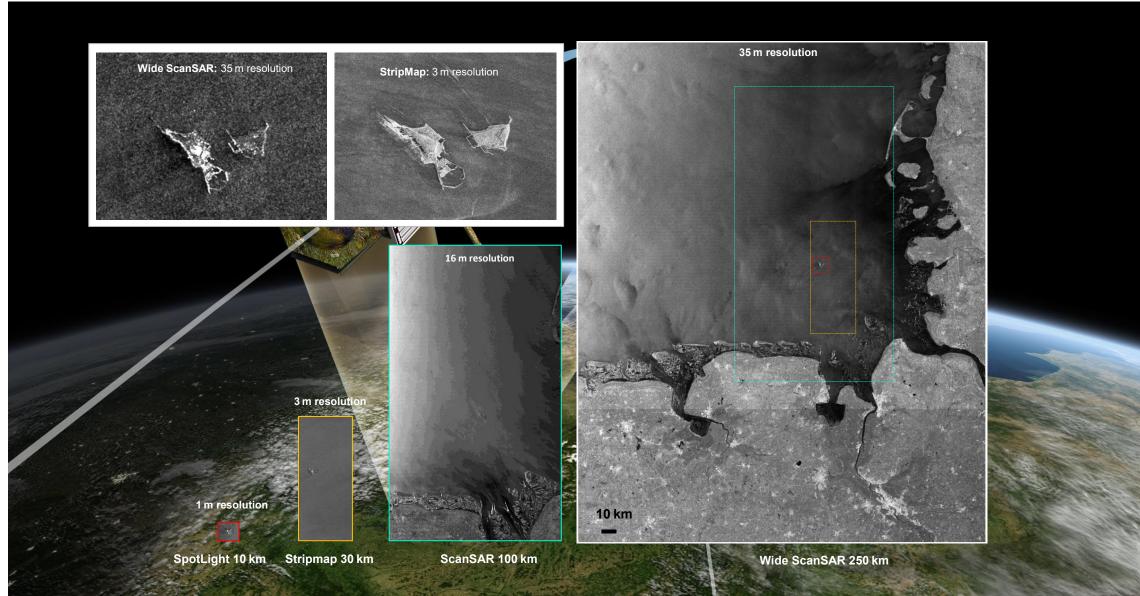
## **SAR Satellites: X-band**





## **TerraSAR-X Acquisition Modes**



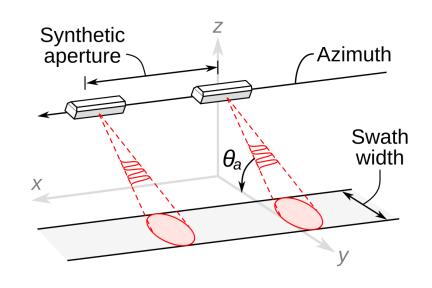


## **SAR: Synthetic Aperture Radar**



- Transmit pulses of electromagnetic waves
- And receive echoes of each pulse (amplitude & phase)
- Satellite moves at constant speed
  - Synthetic aperture much longer than physical antenna width
- Side-looking antenna: Discrimination of objects along ground-range
  - > Two-dimensional imaging
- Always trade-off between spatial resolution and coverage

#### Synthetic aperture radar



## **Sentinel-1 Image Focusing**

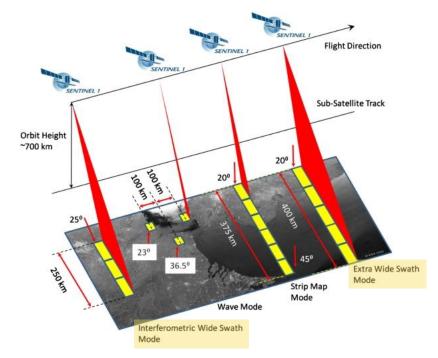


#### **Processor Specifications**

- Support two TOPSAR modes
  - Interferometric wide (IW): 250 km swath width
  - Extra wide (EW): 400 km swath width
- L0 raw data downloaded from Copernicus Data Space Ecosystem
- Chirp scaling algorithm

#### **Preliminary Results**

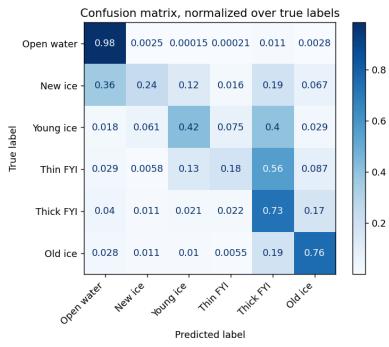
- Full image latency: 26 seconds
- Latency dominated by PS
- Expect 15 seconds after software optimization



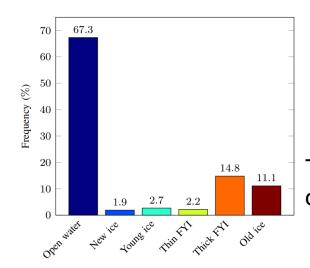
Sentinel-1 acquisition modes (Source: ESA)

#### **Classifier Prediction Results**

- Dataset highly imbalanced
- Training with weighted Cross-Entropy loss
- Evaluation with weighted average F1 score



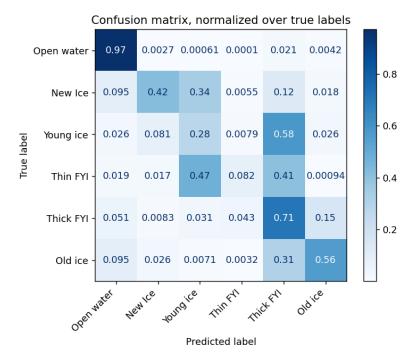






Training dataset class distribution

Ice Stage of Development Class



Test

## **CNN Implementation on FPGA**



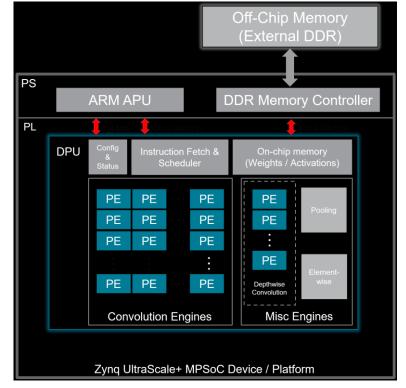
#### **Dataflow Architecture**

- Map each layer to FPGA fabric
- Dedicated circuit compiled for specific model
- Beneficial for deterministic inference latency

#### **Accelerator**

- Implements set of common operators
- Programmed via instruction set
- Supports larger models
- More comprehensive toolchains





AMD Deep Learning Processor Unit (DPU) for Zynq US+ Source: AMD