Decentralized Battery Management System for Improved Reliability and Optimized Battery Operation

vorgelegt von
M. Sc.
Andrea Reindl
ORCID: 0000-0002-8903-4703

an der Fakultät V -Verkehrs- und Maschinensysteme
der Technischen Universität Berlin
zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften
- Dr.-Ing. -

genehmigte Dissertation

Promotionsausschuss:
Vorsitzender: Prof. Dr.-Ing. Dietmar Göhlich
Gutachter: Prof. Dr.-Ing. Sangyoung Park
Gutachter: Prof. Dr.-Ing. Hans Meier
Gutachterin: Prof. Dr.-Ing. Julia Kowal
Gutachter: Prof. Dipl.-Ing. Anton Haumer
Tag der wissenschaftlichen Aussprache: 09. Januar 2024

Berlin 2024

Zusammenfassung

In dieser Dissertation wird eine dezentralisierte Architektur für heterogene Batteriesysteme vorgestellt und die damit verbundenen Herausforderungen in Bezug auf Entwicklung und Regelung werden unter Berücksichtigung der Systemziele einer verbesserten Zuverlässigkeit und Systemverfügbarkeit sowie eines optimierten Batteriebetriebs adressiert.
Mit der Integration von erneuerbaren Energiequellen und der Elektrifizierung des Transportsektors steigt die Nachfrage an Batteriespeichern. Bei sicherheitskritischen Anwendungen wie Elektrofahrzeugen oder Heimspeichersystemen spielen dabei die Zuverlässigkeit, Sicherheit und Verfügbarkeit des Batteriesystems eine entscheidende Rolle.
Die steigende Nachfrage nach Batterien führt zu ständigen Neuentwicklungen mit dem Ziel, die Leistungsfähigkeit und Speicherkapazität zu verbessern. Darüber hinaus steigt mit der zunehmenden Nutzung von Batteriesystemen auch die Zahl der Second-Life-Batterien. Second-Life-Batterien sind Batterien, die aufgrund von erhöhtem Innenwiderstand und verringerter Kapazität nicht mehr in Anwendungen mit hohen Anforderungen an Dynamik und Speicherkapazität, wie z. B. in Elektroautos, eingesetzt werden können. Diese Batterien können noch in Anwendungen wie Heimspeichersystemen mit geringeren Anforderungen an die Dynamik eingesetzt werden.
Heterogene Batteriesysteme kombinieren Batterien mit Unterschieden in der Zellchemie, der verbleibenden Batteriekapazität, dem Ladezustand, dem Gesundheitszustand und dem zulässigen Betriebsbereich in einem System. Sie ermöglichen das Nutzen möglicher Synergieeffekte bei der Verwendung unterschiedlicher Batterieeigenschaften, zum Beispiel die Kombination von leistungs- und energiedichten Batterien, und bieten zusätzlich die Möglichkeit, Second-Life-Batterien zu integrieren.
Für ausreichend hohe Batterieströme und genügend Batteriekapazität werden mehrere Batteriemodule parallel verschaltet. Unterschiedliche Batteriemodule mit verschiedenen Zellchemien weisen dabei abweichende Klemmenspannungen, wobei diese zum Teil zusätzlich vom Ladezustand abhängig sind und sich im Laufe des Betriebs verändern.
Die direkte Parallelschaltung von Batterien, das heißt ohne zusätzliche Leistungselektronik, mit abweichenden Klemmenspannungen führt zu unkontrollierten, unter Umständen sehr hohen, Umlaufströmen zwischen den Batteriemodulen. Dies führt zu einer unkontrollierten Ladung und Entladung der Batterien und im schlimmsten Fall zu einem Batteriebetrieb außerhalb des sicheren Betriebsbereichs, was zu signifikanten Sicherheitsrisiken führt. Außerdem speisen sich die Batterien gegenseitig und das tatsächliche Regelungsziel,die zuverlässige Versorgung einer angeschlossenen Last, wird nicht erreicht.
In dieser Arbeit wird ein Gleichstromsystem betrachtet, das aus einer variablen Anzahl von verschiedenen Batterien, variablen Lasten und Erzeugern besteht. Um die

Zuverlässigkeit und Verfügbarkeit zu verbessern, wird eine dezentrale Architektur vorgeschlagen, bei der alle Systemkomponenten (Batterien, Erzeuger und Lasten) mit lokalen Steuereinheiten ausgestattet sind. Die lokalen Steuereinheiten umfassen einen Mikrocontroller mit Kommunikationsschnittstellen, Strom- und Spannungssensoren, ein Relais, das im Falle einer Störung oder zu Wartungszwecken geöffnet werden kann, sowie DC-DC Wandler. Um den Leistungsfluss in Lade- und Entladerichtung zu realisieren, werden bidirektionale DC-DC-Wandler für die Batterien eingesetzt. Die Systemsteuerung ist auf die funktional gleichwertigen, gleichberechtigten lokalen Steuereinheiten verteilt, wodurch mögliche Single Points of Failures reduziert werden. Trotz der zahlreichen Vorteile, die sich aus der Kombination verschiedener Batterien und der Dezentralisierung des Systems ergeben, gibt es einige offene Herausforderungen bei der Koordinierung der Systemaufgaben, der Regelung und der Implementierung zu bewältigen.
Die Kommunikation zwischen den Komponenten ist erforderlich, um den Informationsaustausch mit übergeordneten Systemkomponenten zu ermöglichen und die Erledigung der Systemaufgaben auf kollaborative Weise zu erreichen. Systemweite Datenkonsistenz, geringe Latenzzeit bei wenigen Nutzdatenbytes, geringer Rechenaufwand und geringer Stromverbrauch sind dabei Anforderungen an die Kommunikation, die sich aus der gewählten Architektur ergeben.
Für die Synchronisation zwischen den Komponenten und die Zuteilung von Systemaufgaben wird eine zentrale Steuereinheit benötigt, ohne die Systemzuverlässigkeit durch die Einführung potentieller Single Points of Failures zu gefährden. Für eine effektive Aufgabenkoordinierung in einem System, das aus vernetzten, funktional gleichwertigen Knoten besteht, wird ein dynamischer, kriteriumsbasierter Algorithmus zur Wahl einer temporären Steuereinheit vorgeschlagen. Einer der Batterieknoten wird in Abhängigkeit von einem definierten Wahlkriterium vorübergehend zur zentralen Steuereinheit gewählt. Er steuert die Ausführung der Systemaufgaben und synchronisiert die lokalen Messungen der einzelnen Knoten.
Das Hauptziel der Systemsteuerung ist die stabile Regelung der Zwischenkreisspannung auf einen vorgegebenen Sollwert bei variablen Lasten und Verbrauchern. Für einen sicheren Betrieb eines heterogenen Batteriesystems ist es notwendig, die unterschiedlichen sicheren Betriebsbereiche der verschiedenen Batterien zu berücksichtigen. Dafür ist eine batteriezustandsabhängige Laststromverteilung in allen Betriebsarten notwendig. Es werden zwei verschiedene Regelungsstrategien zur Realisierung der batteriezustandsabhängigen Laststromverteilung vorgestellt, die sich in den Kommunikationsanforderungen, in der Regelungsgenauigkeit und -dynamik, in der Robustheit und in der Möglichkeit zur Berücksichtigung von Batteriedegradation unterscheiden. Darüber wird eine systemweite eindeutige Zustandsbewertung verschiedener Batterien unter Berücksichtigung ihrer zulässigen Betriebsbereiche vorgestellt.
Für die Umsetzung werden spezielle DC-DC-Wandler benötigt, die einen variablen Eingangsspannungsbereich auf der Niederspannungsseite zur Unterstützung unterschiedlicher Batterien, eine einstellbare Spannung auf der Hochspannungsseite zur Unterstützung mehrerer Anwendungen, wobei hier Niederspannungssysteme in einem Bereich von $18\,V$ bis $24\,V$ betrachtet werden, und eine im aktiven Betrieb einstellbare Strombegrenzung aufweisen. Für erste Tests der Regelung und für Skalierbarkeitsbetrachtungen sind Simulationen der DC-DC-Wandler notwendig. Außerdem ist eine spezielle Testumgebung erforderlich, die die Kommunikationsleitung im Regelkreis berücksichtigt. Für die Mikrocontroller werden spezielle

Algorithmen implementiert, um die Kommunikations-, Koordinations-, Mess- und Steuerungsaufgaben zu erfüllen.
Um die Funktionalität der dezentralen Architektur und die Erfüllung der definierten Regelungsziele zu verifizieren, wurde ein Hardware-Testaufbau bestehend aus vier lokalen Steuereinheiten entwickelt. Experimentelle Daten unter Berücksichtigung verschiedener Lastszenarien zeigen das gewünschte Verhalten. Erste Tests zum Nachweis der Robustheit, z.B. Ausfall eines Knotens, fehlerhafte Strom- oder Spannungsmessung, wurden ebenfalls erfolgreich durchgeführt.

Abstract

In this thesis, a decentralized architecture for heterogeneous battery systems is presented and the corresponding design and control challenges are addressed considering the system objectives of increased reliability and system availability as well as optimized battery operation.
With the integration of renewable energy sources and the electrification of the transportation sector, the demand for battery storage systems is increasing. In safety-critical applications such as electric vehicles or home storage systems, the reliability, safety and availability of the battery system play a crucial role.
The increased demand for batteries is leading to constant new developments with the aim of improving performance and capacity. Furthermore, with the increased use of battery systems, the number of second life batteries is rising. Second life batteries are batteries which, due to increased internal resistance and reduced capacity, can no longer be used in applications with high requirements in terms of dynamics and storage capacity, such as electric cars. These batteries can still be used in applications such as home storage systems with lower requirements in terms of dynamics.
Heterogeneous battery systems combine batteries with differences in cell chemistry, actual battery capacity, state of charge, state of health, and permissible operating range in one system. They enable the exploitation of different battery characteristics, for example the combination of power- and energy-dense batteries, and provide and offer the additional option of integrating second life batteries.
For sufficiently high battery currents and adequate battery capacity, several battery modules are connected in parallel. Different battery modules with various cell chemistries have deviating terminal voltages, whereby these also in some cases depend on the state of charge.
The direct parallel connection of batteries with deviating terminal voltages leads to uncontrolled, potentially very high, circulating currents between the battery modules. This results in uncontrolled charging and discharging of the batteries and, in the worst case, to battery operation outside the safe operating area resulting in serious safety risks. Furthermore, the batteries supply each other and the actual control objective, i.e. the reliable supply of a connected load, is not achieved.
In this thesis, a DC system consisting of a varying number of various batteries, variable loads and generators is considered. For improved reliability and availability, a decentralized architecture is proposed, whereby all system components (batteries, generators and loads) are equipped with local control units. The local control units include a microcontroller with communication interfaces, current and voltage sensors, a relay that can be opened in case of a fault or for maintenance purposes, and DC-DC converters. In order to realize the power flow in charging and discharging direction, bidirectional DC-DC converters are used for the batteries. The system control is distributed among the functional equivalent, equally local control units, thus reducing potential single points of failures.

Despite the numerous advantages that arise from the combination of different batteries and the decentralization of the system, there are several open challenges to be addressed in terms of the coordination of the system tasks, the control and the implementation.
Communication between the nodes is required in order to enable information exchange with higher level system components and to achieve the completion of the system tasks in a collaborative manner. System-wide data consistency, low latency with few user data bytes, low computational effort and low power consumption are communication requirements that arise from the chosen architecture.
A central control unit is required for synchronization between the nodes and the allocation of system tasks without endangering the system reliability by introducing potential single points of failures. For effective task coordination in a system consisting of networked, functionally equal nodes, a dynamic, criterion-based leader election algorithm is proposed. One of the battery nodes is temporarily elected as the leader depending on a defined election criterion. It controls the execution of the system tasks and synchronizes the local measurements of the individual nodes.
The main objectives of the system control is the stable regulation of the DC line voltage to a predefined set point under variable loads and consumers. For a safe operation of a heterogeneous battery system it is necessary to consider the different safe operating areas of the diverse batteries. In order to combine diverse batteries while maintaining the safe operating areas, a battery-state dependent load current distribution is necessary in all operating modes. Therefore, two different control strategies are presented for the realization of the battery-state dependent load current distribution, which differ in the communication requirements, in the control accuracy and dynamics, in robustness, and in the possibility to acount for battery degradation. In addition, a system-wide unambiguous state evaluation of different batteries is required, taking into account their permissible operating ranges.
For the implementation, dedicated DC-DC converters are required which have a variable input voltage range at the low voltage side for the support of different batteries, an adjustable voltage at the high voltage side for supporting different applications, whereby low voltage systems in a range of $18V$ to $24V$ are considered here, and a current limitation which can be adjusted in active operation. For initial tests of the control system and for scalability considerations, simulations of the DC-DC converters are necessary. Furthermore, a special test environment is required which takes into account the communication line in the control loop. Special algorithms are implemented for the microcontrollers to fulfill the communication-, coordination-, measurement- and control-tasks.
A hardware test setup consisting of four local control units was developed to verify the functionality of the decentralized architecture and the fulfillment of the defined control objectives. Experimental data under consideration of different load scenarios exhibits the desired behavior. Initial tests to demonstrate robustness, e.g. failure of a node, faulty measurements, were also carried out successfully.

Dedication

To my parents Anita and Martin Reindl for their everlasting support.
To Sebastian Wolf for his unconditional encouragement and loving guidance.

Acknowledgements

This thesis is the outcome of a cooperative doctorate program between the Ostbayerische Technische Hochschule Regensburg and the Technische Universität Berlin. Numerous people have contributed significantly, and it is my sincere pleasure to express my gratitude.
First of all, I would like to thank Prof. Dr.-Ing. Dietmar Göhlich for chairing the thesis committee and Prof. Dr.-Ing. Julia Kowal for reviewing the thesis. I would like to express my gratitude and sincere appreciation to my valued supervisors, Prof. Dr.-Ing. Sangyoung Park, Prof. Dr.-Ing. Hans Meier, and Prof. Dr. rer. nat. Michael Niemetz for their unwavering support, guidance, and mentorship throughout my research journey. They gave me the opportunity to pursue my doctorate and their expertise, constructive criticism, and insightful feedback have significantly influenced my research work. I am especially grateful to Prof. Dr.-Ing. Hans Meier and Prof. Dr. rer. nat. Michael Niemetz for their longstanding support since my undergraduate studies and the numerous professional and personal development possibilities and the freedom they offered me. I am very grateful to Prof. Dr.-Ing. Lars Eriksson for welcoming me at the Linköping University in Sweden and providing me with valuable insights into modeling and control during our discussions. Furthermore, Prof. Dr.-Ing. Lars Eriksson not only helped me to become a better researcher, but also showed me how much fun and joy research brings and how important reflection is. I would like to thank Prof. Dipl. Ing. Anton Haumer for his tireless support, his everlasting encouragement and his openness to help me realize my ideas. My special thanks go to all the members of the Laboratory of Industrial Electronics, especially Michael Farmbauer, Jochen Pernsteiner and Florian Hollnberger. Without their expert advice, the implementation of the decentralized battery management system would not have been possible.
Furthermore, I would like to thank Prof. Dr.-Ing. Norbert Balbierer, Prof. Dr.-Ing. Claus Brüdigam, Prof. Dr.-Ing. Rainer Holmer, Prof. Dr.-Ing. Bernhard Hopfensperger, Dr. rer. nat. Roland Hornung, Prof. Dr.-Ing. Robert Huber, Prof. Dr.-Ing. Stefan Krämer, Prof. Dr.-Ing. Christian Schimpfle for their expert advice and support. I would like to thank Prof. Dr.-Ing. Armin Merten for welcoming me in his office and for his positive encouragement. I am grateful to my mentor Prof. Dr.-Ing. Birgit Rösel for her guidance on this journey, her support and for the numerous conversations about academia we had.
A number of students have contributed to the success of this project in the form of a project, bachelor's or master's thesis, and I would like to express my gratitude to Maximilian Beck, Michael Beubl, Alexander Demel, Alexander Dischner, Simon Eichhammer, Philipp Eisenbarth, Kilian Garschhammer, Pascal Hammer, Michael Jupke, Dominik Kemeter, Patrick Körner, Ina Kuhn, Andreas Lang, Tobias Langer, Florian Lausser, Christian Lang, Lukas Nützel, Luis Reber, Leonardo Sanmiguel, Viola Schneider, Thomas Singer, Melanie Steinberger and Christian Zwick.

Special thanks to Thomas Eichstetter for his excellent expertise in electromagnetic compatibility and his suggestions for improvement, which resulted in a significantly improved layout of the circuit boards.
I would like to thank Andreas Hofmeister for his open ear and the advice and motivation of a special kind at the Stammtisch "Hans's Apples". Andreas, there is a lot of truth in your somewhat controversial advice and it has helped me a lot.
Without the "Future Doktor Bande" Lea Huber, Tobias Frauenschläger and Manuel Dentgen I would not have started this journey. I am grateful to them for the amazing friendship, the numerous evenings at the Unikat, for rehearsing my conference talks and the fun we had discussing possible improvements. Nina Prem is a valuable companion and I would like to thank her for her continuous support, her friendship and her openness to attend numerous workshops with me.
I would like to thank all the members of the department "Fordonssystem"/ Vehicular Systems at Linköping University for the warm welcome and the numerous fika sessions. Thanks to them, I immediately felt welcome and comfortable in Linköping. Special thanks to Abhijeet Behera, Shadi Hashemniya, Dr. Olov Holmer, Max Johansson, Arman Mohammadi, Theodor Westny and Jian Zhou. Arvind Balachandran, Oskar Lind Jonsson and Moa Nyström welcomed me immediately and showed me the beautiful Sweden. I am grateful to them for the friendship we have and the endless fun we had during the summmer 2022. They all made my stay in Sweden unforgettable.
I would like to thank my colleagues at the Technical University of Berlin for the warm welcome and the exchanges in the doctoral colloquium. Special thanks to Philipp Kremer for the exchange and motivation sessions in Zoom that guided the writing phase of my dissertation.
Thanks to LaKoF Bayern for financially supporting this work and for providing opportunities for further development in the field of higher education pedagogy, especially to Sabine Hoffmann and Dr. Christine Süß-Gebhardt.
I would like to thank the Hanns Seidel Foundation for their financial and idealistic support and the numerous opportunities for further development. Many of my fellows became friends and significantly enriched the time of my doctoral studies. Special thanks go to Dr. Möhringer and Dr. Andreas Burtscheidt for their outstanding engagement - they do an excellent job.
My best friends Anika Mück and Franziska Kinskofer have accompanied this path with interest, openness, unconditional support and advice. They were always insightful that I invested a lot of time in the work - my heartfelt thanks for that.
I would like to thank my parents Anita and Martin and my brother David for their never-ending support, their words of encouragement and their helpful advice. I thank Sebastian Wolf from the bottom of my heart for his loving support along the way, his interest in my work, and for so much more. Without you, Anita, Martin and Sebastian, none of this would have been possible.
Last, I would like to conclude by thanking the thousands of people who have programmed for free for open source projects, written forum posts, and provided help in forums. Thanks to their efforts, scientific work with powerful tools and without endless debugging is possible.

Andrea Reindl

List of Publications

Conference Contributions

[1] **A. Reindl**, A. Lang, M. Niemetz, and H. Meier, "Switching and Averaging Models of a Bidirectional, Half-Bridge Based DC-DC Converter with Load Distribution," 15th International Modelica Conference, Aachen, Germany, 2023.

[2] **A. Reindl**, F. Lausser, L. Eriksson, S. Park, M. Niemetz, and H. Meier, "Mathematical Modeling of a Bidirectional DC-DC Converter - Part 1: Buck Mode," 2023 International Conference on Applied Electronics (AE), Pilsen, Czech Republic, pp. 1–7, IEEE, 2023.

[3] **A. Reindl**, F. Lausser, L. Eriksson, S. Park, M. Niemetz, and H. Meier, "Mathematical Modeling of a Bidirectional DC-DC Converter - Part 2: Boost Mode," 2023 International Conference on Applied Electronics (AE), Pilsen, Czech Republic, pp. 1–7, IEEE, 2023.

[4] **A. Reindl**, D. Wetzel, M. Niemetz, and H. Meier, "Leader Election in a Distributed CAN Based Multi-Microcontroller System," 2023 3rd International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME), Tenerife, Canary Islands, Spain, pp. 1-8, IEEE, 2023.

[5] **A. Reindl**, L. Eriksson, M. Niemetz, S. Park, and H. Meier, "Control Concepts for a Decentralized Battery Management System to Optimize Reliability and Battery Operation," Proceedings of the International Renewable Energy Storage Conference (IRES 2022), vol. 16, p. 401, Springer Nature, 2023.

[6] **A. Reindl**, T. Langer, H. Meier, and M. Niemetz, "Comparative Reliability Analysis for Single and Dual CAN(FD) Systems," 2022 International Conference on Applied Electronics (AE), Pilsen, Czech Republic, pp. 1-6, IEEE, 2022.

[7] D. Wetzel, **A. Reindl**, H. Meier, M. Niemetz, and M. Farmbauer, "A Customized Python Interface for Windows OS for a Low Budget USB-to-CAN-Adapter," 2022 International Conference on Electrical, Computer and Energy Technologies (ICECET), Prague, Czech Republic, pp. 1-5, IEEE, 2022.

[8] P. Körner, **A. Reindl**, and H. Meier, "A Theoretical Comparison of Different Virtual Synchronous Generator Implementations on Inverters," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), pp. 1–9, IEEE, 2022.

[9] **A. Reindl**, H. Meier, M. Niemetz, and S. Park, "Decentralized Battery Management System with Customized Hardware Components," 2021 19th Student Conference on Research and Development (SCOReD), pp. 350–355, IEEE, 2021.

[10] F. Herbold, **A. Reindl**, H. Meier, M. Niemetz, and S. Krämer, "Secure Software Updates: Challenges and Solutions for Embedded IoT Systems," 9th Prague Embedded Systems Workshop, 2021 Czech Republic, 2021.

[11] **A. Reindl**, T. Singer, H. Meier, M. Niemetz, and S. Park, "Framework to Test DC-DC Converters Developed for a Decentralized Battery Management System," 2021 International Conference on Applied Electronics (AE), Pilsen, Czech Republic, pp. 1-6. IEEE, 2021.

[12] M. Jupke, **A. Reindl**, H. Meier, and M. Niemetz, "Bidirectional DC-DC Converter with Digital Droop Parameterization," In 2021 International Conference on Applied Electronics (AE), Pilsen, Czech Republic, pp. 1-6, IEEE, 2021.

[13] **A. Reindl**, D. Wetzel, H. Meier, N. Balbierer, M. Niemetz, and S. Park, "Comparative Analysis of CAN, CAN FD and Ethernet for Networked Control Systems," embedded world digital conference, Nürnberg, 2021.

[14] **A. Reindl**, H. Meier, and M. Niemetz, "Scalable, Decentralized Battery Management System Based on Self-Organizing Nodes," International Conference on Architecture of Computing Systems, pp. 171-184. Cham: Springer International Publishing, 2020.

[15] **A. Reindl**, V. Schneider, H. Meier, and M. Niemetz, "Software Update of a Decentralized, Intelligent Battery Management System Based on Multi-Microcomputers," Symposium Elektronik und Systemintegration: Intelligente Systeme und ihre Komponenten: Forschung und industrielle Anwendung, Landshut, 2020.

[16] **A. Reindl**, H. Meier, and M. Niemetz, "Software Framework for the Simulation of a Decentralized Battery Management System Consisting of Intelligent Battery Cells," 2019 IEEE Student Conference on Research and Development (SCOReD), Bandar Seri Iskandar, Malaysia, IEEE, 2019.

Invited Papers

[1] **A. Reindl**, D. Wetzel, H. Meier, N. Balbierer, M. Niemetz, and S. Park, "Part I: Comparing CAN, CAN FD and Ethernet," CAN in Automation (CiA), CAN Newsletter Hardware + Software + Tools + Engineering, pp. 26–29, 2021.

[2] **A. Reindl**, D. Wetzel, H. Meier, N. Balbierer, M. Niemetz, and S. Park, "Part II: Comparing CAN, CAN FD and Ethernet," CAN in Automation (CiA), CAN Newsletter Hardware + Software + Tools + Engineering, pp. 26–29, 2021.

Software Publications

[1] **A. Reindl**, A. Lang, M. Niemetz, and H. Meier, "Switching and Averaging Models of a Bidirectional, Half-Bridge Based DC-DC Converter with Load Distribution," 15th International Modelica Conference, Aachen, Germany, `https://github.com/rea40157/BidiDCDC`.

Oral Presentations

[1] **A. Reindl**, "Switching and Averaging Models of a Bidirectional, Half-Bridge Based DC-DC Converter with Load Distribution," International Modelica Conference, Aachen, Germany, 9th October 2023.

[2] **A. Reindl**, "Mathematical Modeling of a Bidirectional DC-DC Converter - Part 1: Buck Mode," International Conference on Applied Electronics (IEEE), Pilzen, Czech Republic, 6th September 2023.

[3] **A. Reindl**, "Mathematical Modeling of a Bidirectional DC-DC Converter - Part 2: Boost Mode," International Conference on Applied Electronics (IEEE), Pilzen, Czech Republic, 6th September 2023.

[4] **A. Reindl**, "Leader Election in a Distributed CAN Based Multi-Microcontroller System," International Conference on Electrical, Computer, Communications and Mechatronics Engineering (IEEE), 20th July 2023.

[5] **A. Reindl**, "Aspects of a Battery State Aware Load Current Distribution in a Heterogeneous Battery System", Battery & Power World, Munich, Germany, 1st February 2023.

[6] **A. Reindl**, "Comparative Reliability Analysis for Single and Dual CAN(FD) Systems," International Conference on Applied Electronics (IEEE), 6th September 2022.

[7] **A. Reindl**, "Distributed Battery Management System for Improved Battery Operation and Reliability," DiConBatt, Workshop, Linköping, Sweden, 26th August 2022.

[8] **A. Reindl**, "Distributed Battery Management System for Enhancing Safety and Availability," GRIS Seminar, Linköping University, Sweden, 25th May 2022.

[9] **A. Reindl**, "Decentralized Battery Management System with Customized Hardware Components," Student Conference on Research and Development (IEEE), online, 24th November 2021.

[10] **A. Reindl**, "Framework to Test DC-DC Converters Developed for a Decentralized Battery Management System," International Conference on Applied Electronics (IEEE), online, 7th September 2021.

[11] **A. Reindl**, "Comparative Analysis of CAN, CAN FD and Ethernet for Networked Control Systems," embedded world digital conference, online, 2nd March 2021.

[12] **A. Reindl**,"Distributed Battery Management System for Enhancing Safety and Availability," Pitch your Research, online, 20th October 2020.

[13] **A. Reindl**, "Software Framework for the Simulation of a Decentralized Battery Management System Consisting of Intelligent Battery Cells," IEEE Student Conference on Research and Development, Bandar Seri Iskandar, Malaysia, IEEE, 15th October 2019.

Poster Presentations

[1] **A. Reindl**, "Control Concepts for a Decentralized Battery Management System to Optimize Reliability and Battery Operation," International Renewable Energy Storage Conference, Düsseldorf, Germany, 20th –22th September 2022.

Video Presentations

[1] **A. Reindl**, "Comparative Analysis of CAN, CAN FD and Ethernet for Networked Control Systems," `https://www.youtube.com/watch?v=svUpQC4ZLLE&t=608s&ab_channel=OTHRegensburg`, 2021.

[2] **A. Reindl**, "Decentralized Battery Management System for Improved Reliability and Optimized Battery Operation," 2023.

Table of Contents

Title Page i

Zusammenfassung iii

Abstract vii

1 Introduction 1
- 1.1 Motivation . . . 1
- 1.2 Determination of the Objectives . . . 3
- 1.3 Research Questions . . . 6
- 1.4 Thesis Outline . . . 6
- 1.5 Contributions . . . 9

2 Battery Fundamentals and Characteristic Parameters 11
- 2.1 Non-Lithium Battery Cells . . . 12
- 2.2 Lithium-based Battery Cells . . . 13
- 2.3 Further Improvements of Lithium Battery Cells and Alternative Battery Technologies . . . 15
- 2.4 Reuse of Second Life Batteries . . . 19
- 2.5 Battery Safety Risks and Safe Operation . . . 21
- 2.6 Battery Parameters for the Estimation of the Battery Condition . . . 23
  - 2.6.1 Thévenin Equivalent Circuit Model of Batteries . . . 23
  - 2.6.2 State of Power . . . 24
  - 2.6.3 State of Charge . . . 26
  - 2.6.4 State of Energy . . . 27
  - 2.6.5 State of Function . . . 27
  - 2.6.6 State of Safety . . . 27
  - 2.6.7 State of Temperature . . . 28
  - 2.6.8 State of Health . . . 28

3 General System Description and Requirements Analysis 33
- 3.1 Motivation . . . 33
- 3.2 Related Work: Battery Management System Topologies . . . 35
  - 3.2.1 Centralized . . . 35
  - 3.2.2 Modularized . . . 36
  - 3.2.3 Distributed . . . 36
  - 3.2.4 Decentralized . . . 37
- 3.3 Decentralized Battery Management System Based on Self-Organizing Nodes . . . 39
  - 3.3.1 Distributed Control . . . 39

3.3.2 Communication . . . 41
3.3.3 Safe Operation of a Heterogeneous Battery System and Battery State Aware Load Distribution . . . 42
3.3.4 Scalability and Integration . . . 43
3.3.5 Flexibility . . . 43
3.3.6 Fields of Application . . . 43
3.4 Summary . . . 43

4 Communication Requirements and Comparative Analysis 45
4.1 Motivation . . . 45
4.2 Related Work . . . 48
4.3 Setup of the Test Environment . . . 49
4.3.1 Software Implementation . . . 49
4.3.2 Hardware Components for the Implementation of CAN, CAN FD and Ethernet Communication . . . 50
4.3.3 Test Setup for the Comparative Analysis . . . 50
4.4 Selection of the Comparative Evaluation Criteria and Description of the Acquisition Methods . . . 51
4.4.1 Message Processing Time Acquisition . . . 51
4.4.2 Processor Workload . . . 51
4.4.3 Energy Consumption . . . 52
4.4.4 Error Rate . . . 52
4.4.5 RX-FIFO Load . . . 52
4.5 Results and Discussion . . . 52
4.5.1 Message Processing Time Measurements and Comparison . 53
4.5.2 Measurement and Comparative Analysis of the Processor Workload . . . 54
4.5.3 Comparison of the Energy Consumption . . . 57
4.5.4 Error Rates . . . 57
4.5.5 RX-FIFO Load . . . 60
4.6 Summary . . . 61

5 Leader Election for the Coordination of the System Tasks 67
5.1 Motivation . . . 67
5.2 Related Work . . . 69
5.3 System Description . . . 69
5.3.1 Node Weight . . . 69
5.3.2 Determination of the Node Weight for the Decentralized Battery Management System . . . 71
5.3.3 Participants List . . . 71
5.3.4 Tasks of the Management Level . . . 71
5.4 Requirements Analysis . . . 72
5.5 LEA-CAN: CAN-based Leader Election Algorithm for Distributed Systems . . . 73
5.5.1 Big LEA-CAN . . . 73
5.5.1.1 Description of the Election Process of the Big LEA-CAN . . . 74
5.5.1.2 Termination Criterion of the Big LEA-CAN . . . 76
5.5.1.3 Implementation of the Big LEA-CAN . . . 76
5.5.2 Small LEA-CAN . . . 77

5.5.2.1 Description of the Election Process of the Small LEA-CAN . . . 78
5.5.2.2 Termination Criterion of the Small LEA-CAN . . 78
5.5.2.3 Implementation . . . 80
5.6 Election Messages . . . 81
5.7 Time Complexity and Scalability Analysis . . . 83
5.8 Error Handling . . . 84
5.9 Hardware Test Setup . . . 85
5.10 Summary . . . 86

6 Operation and Control Strategies 89
6.1 Motivation . . . 89
6.2 Related Work . . . 91
6.2.1 Centralized Control Strategies . . . 91
6.2.2 Decentralized Control Strategies . . . 91
6.2.3 Distributed Control Strategies . . . 92
6.2.4 Hierarchical Control Strategies . . . 92
6.2.5 Comparison of Existing BMS Control Architectures in Terms of Reliability, Scalability and Control Quality . . . 93
6.2.6 Adaptation Capabilities of Control Architectures . . . 93
6.3 Control Objectives, Optimizations and Distribution to Separate Control Levels . . . 94
6.3.1 Optimization Scenarios . . . 94
6.3.1.1 Optimal Battery Operation . . . 94
6.3.1.2 Maximum Efficiency . . . 95
6.3.1.3 Long Operation Duration . . . 95
6.3.1.4 Ensured Supply of the Loads . . . 95
6.3.1.5 High System Availability . . . 95
6.4 Global Control Level Strategies . . . 96
6.4.1 Decentralized, Droop-based Control Strategy . . . 96
6.4.2 Hierarchical, Communication-based Control Strategy . . . 98
6.4.2.1 Challenges of Decentralized Systems Consisting of Autonomously Operating Nodes . . . 98
6.4.2.2 Introduction of Control Layers . . . 98
6.5 Local Control Level Strategies . . . 99
6.5.1 Hardware-based Control . . . 101
6.5.2 Software-based Adaptive Control . . . 102
6.6 Assignment of the Control Strategies to the Operating States . . . 103
6.7 Summary . . . 103

7 Mathematical Modeling and Stability Analysis 107
7.1 Motivation . . . 107
7.2 Related Work . . . 109
7.3 Description of the Bidirectional DC-DC Converter . . . 110
7.4 Theoretical Background . . . 111
7.4.1 Operating Modes of the DC-DC Converter . . . 111
7.4.2 Small-Signal Transfer Functions . . . 112
7.5 Buck Mode of the Bidirectional DC-DC Converter . . . 113
7.5.1 Small-Signal Model and Derivations of the Transfer Functions for Buck Mode and CCM . . . 114

7.5.1.1 Duty Cycle to Current Transfer Function $G_{id}(s)$. 114
7.5.1.2 Current to Voltage Transfer Function $G_{vi}(s)$ . . . 116
7.5.1.3 Duty Cycle to Voltage Transfer Function $G_{vd}(s)$. 118
7.5.2 Small-Signal Model and Derivations of the Transfer Functions for Buck Mode in DCM 118
7.5.2.1 Duty Cycle to Current Transfer Function $G_{id}(s)$. 118
7.5.2.2 Current to Voltage Transfer Function $G_{vi}(s)$ . . . 122
7.5.2.3 Duty Cycle to Voltage Transfer Function $G_{vd}(s)$. 122
7.6 Boost Mode of the Bidirectional DC-DC Converter 123
7.6.1 Small-Signal Model and Transfer Function for Boost Mode in CCM 124
7.6.1.1 Current to Output Transfer Function $G_{id}(s)$ 124
7.6.1.2 Duty Cycle to Voltage Transfer Function $G_{vd}(s)$. 125
7.6.1.3 Current to Voltage Transfer Function $G_{vi}(s)$ . . . 127
7.6.2 Small-Signal Model and Transfer Function for Boost Mode in DCM 127
7.6.2.1 Current to Output Transfer Function $G_{id}(s)$ . . . 127
7.6.2.2 Duty Cycle to Voltage Transfer Function $G_{vd}(s)$. 127
7.6.2.3 Current to Voltage Transfer Function $G_{vi}(s)$ . . . 132
7.7 Poles and Zeros Consideration 132
7.8 Summary 132

8 Average Current Mode Control with Outer Voltage Control 135
8.1 Motivation 136
8.2 Theoretical Background 138
8.2.1 Voltage Control 138
8.2.1.1 Direct Duty Cycle Control 138
8.2.1.2 Voltage Feedforward Control 138
8.2.2 Current Control 139
8.2.2.1 Peak Current Mode Control 139
8.2.2.2 Average Current Mode Control 140
8.3 Control Approach Selection for the Bidirectional DC-DC Converter 141
8.3.1 Voltage Control Method 142
8.3.2 Current Control Method 142
8.3.3 General Control Design of the Average Current Mode Control with Outer Voltage Control Loop 143
8.3.4 General Controller Design with the Small-Signal Model . . 147
8.3.5 Multiphase Bidirectional Current Controller 149
8.3.6 Generation of the PWM Signal for Switching the Transistors G_{PWM} 153
8.3.7 Current Transfer Function H_s 153
8.4 Design of the Controller 155
8.4.1 Design of the Current Controller $G_I(s)$ 155
8.4.2 Design of the Voltage Controller $G_V(s)$ 155
8.4.3 Controller Design for Buck Mode 156
8.4.4 Controller Design for Boost Mode 157
8.5 Implementation of the Control 157
8.5.1 Hardware-based Implementation 158
8.5.2 Software-based Implementation 159
8.6 Concrete Implementation and Consideration of the Control Approaches 160

8.6.1 Controller Dimensioning . . . 160
8.6.2 Controller Analysis of the Buck Mode . . . 161
8.6.3 Controller Analysis of the Boost Mode . . . 162
8.7 Verification of the Small-Signal Model by Hardware Measurements 163
8.8 Summary . . . 164

9 Battery-State-Aware Load Distribution Control Strategies for a Parallel Connection of Heterogeneous Batteries 171
9.1 Motivation . . . 171
9.2 Related Work . . . 173
9.2.1 General Load Distribution Approaches . . . 174
9.2.2 Management of Heterogeneity in Battery Systems . . . 177
9.3 Communicationless Droop-based Control . . . 179
9.3.1 Technical Background on Droop-Based Control . . . 180
9.3.2 Hardware-based Implementation of the Droop Control . . . 182
9.3.2.1 Topology of the Droop-based Controller . . . 183
9.3.2.2 Switch between the Controllers . . . 185
9.3.2.3 Limitation of the Output Signal . . . 185
9.4 Communication-based Load Distribution Control . . . 186
9.4.1 Control Structure of Communication-Based, Battery State-Dependent Load Distribution . . . 187
9.4.2 Reference Transfer Functions of the DC-DC converter . . . 187
9.4.2.1 Reference Transfer Function of the Voltage Control Loop . . . 188
9.4.2.2 Current Transfer Function . . . 189
9.4.3 Load Behavior of n DC-DC Converters Connected in Parallel 189
9.4.4 Dimensioning of the Load Distribution Control . . . 190
9.5 Summary . . . 191

10 Battery Fitness for the State Evaluation of Heterogeneous Batteries 195
10.1 Motivation . . . 195
10.2 Related Work . . . 200
10.2.1 Current Derating Strategies . . . 200
10.2.2 Load Distribution Factor Strategies . . . 200
10.3 Requirements . . . 202
10.4 Implementation . . . 202
10.5 Hybrid and Dynamic Battery Current Derating Strategy . . . 203
10.6 Load Current Distribution Strategies . . . 205
10.6.1 Load Distribution According to the Derated Battery Currents 205
10.6.2 Load Distribution Considering Power Electronic Losses . . . 208
10.6.3 Reaching a Common End of Life . . . 209
10.7 Summary . . . 209

11 Switching and Averaging Models of the DC-DC Converter with Load Distribution 211
11.1 Motivation . . . 211
11.1.1 Related Work . . . 213
11.1.2 Main contributions . . . 213
11.2 Bidirectional DC-DC Converter . . . 214
11.3 Strictly Complementary Switching Model . . . 215

11.3.1 Electrical Simulation 215
11.3.2 Simulation of the Control 217
11.3.3 Validation of the Strictly Complementary Switching Model . 219
11.4 Switching Model with Diode Emulated Mode 220
11.4.1 Additional Control Models 222
11.4.2 Validation of the Switching Model with Diode Emulation . . 222
11.5 Averaging Model 223
11.5.1 Physical Simulation 226
11.5.2 Simulation of the Control 228
11.5.3 Validation of the Averaging Model 228
11.6 Comparison of the Models 229
11.7 Parallel Connection of two DC-DC Converters with Load Distribution 231
11.8 Summary 231

12 Framework for Testing and Evaluating Communication-based Controlled DC-DC Converters 233
12.1 Motivation 233
12.2 Requirements Analysis for the Test Framework 236
12.2.1 Hardware Control According to the Simulation Data 236
12.2.2 Scalability and Flexibility of the Test Framework 236
12.2.3 Various Test Scenarios for Improved Testability with Adjustable Profiles 236
12.3 System Architecture of the Test Framework 237
12.3.1 Hardware Components 237
12.3.2 Software Design 238
12.4 Test Scenarios for an Initial Validation and Verification of the DC-DC Converters 239
12.4.1 Test algorithm and Processing of the Results 240
12.4.2 Implemented Test Scenarios 240
12.5 Validation of the Test Framework 243
12.6 Summary 244

13 Hardware Implementation of the Decentralized Battery Management System 247
13.1 Motivation 247
13.2 Local Control Unit 248
13.2.1 Adaptation and Development of Different DC-DC Converters for the Decentralized Battery Management 249
13.2.2 Local Control Unit with Bidirectional DC-DC Converter . . 255
13.2.2.1 Power Circuit of the Bidirectional DC-DC Converter 255
13.2.2.2 Sensing Module 259
13.2.2.3 Computation Module 261
13.2.2.4 Communication Interfaces 261
13.3 Load box: Stepwise Load Switching via CAN Communication Interface 264
13.4 Display Unit for Current Operating Parameters and the State of the Leader Election 265
13.5 Data Logger for Long-term Evaluation 267
13.6 Summary 267

14 Experimental Data and Final Evaluation regarding the System Goals 271
14.1 Experimental Setup 271
14.2 Experimental Data to Validate Droop-based Control 273
14.2.1 Droop-based Control in Boost Mode 273
14.2.2 Droop-based Control in Buck Mode 275
14.3 Experimental Data to Validate Communication-based Control 283
14.3.1 Communication-based Digital Control in Boost Mode . . . 283
14.3.2 Communication-based Digital Control in Buck Mode 284
14.3.3 Communication-based Digital Control using the Filter Math Accelerator Unit 285
14.3.4 Change of the Load Distribution Factors 297
14.4 Selection of Specific Use Cases 302
14.4.1 System Start-up and Change between Droop-based and Communication-based Control 302
14.4.2 Selection of Test Cases for Analyzing Robustness 307
14.5 Summary 311

15 Conclusion and Outlook 313
15.1 Conclusion 313
15.2 Outlook 317

List of Figures 321

List of Tables 341

Abbreviations 343

Symbols 347

References 351

Appendix A Appendix A 393
A.1 Controller Analysis of the Buck Mode 393
A.2 Controller Analysis of the Boost Mode 393

1 Introduction

1.1 Motivation

Global extreme weather and climate phenomena including wildfires, floods, droughts and cyclones on an unprecedented scale, along with the melting of glaciers indicate significant changes in the global climate [1]. While the earth has undergone changes over millions of years, humans have caused the greatest transformation over the recent millennia (Fig. 1.1). Climate change, besides other environmental factors, is contributing to immense changes in the global system today. Greenhouse gases, such as methane, carbon dioxide (CO_2) (Fig. 1.2), and nitrous oxide, have been identified as main cause of the anthropogenic climate change and global warming [3, 4]. A comparison with the evolution of the world population (Fig. 1.3) shows that the CO_2 demand increases with the rising population and that the CO_2 demand per capita has increased since 1950 from about 2.4 t CO_2 per captia (1950) up to 3.5 t CO_2 per capita.

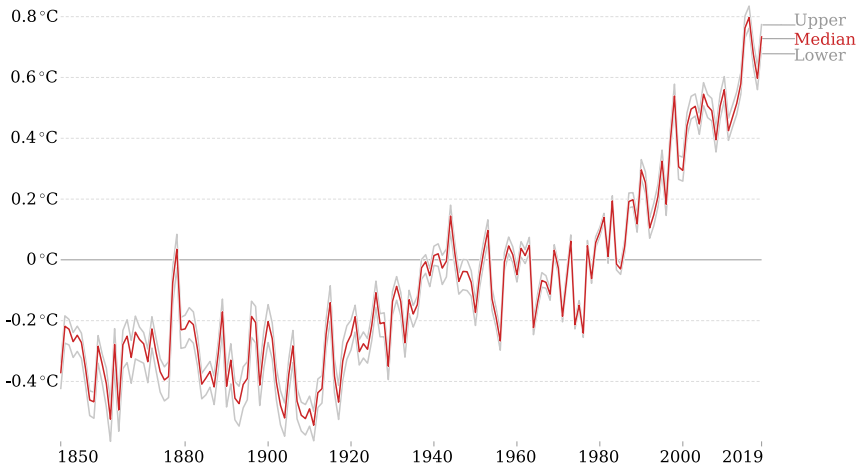


Figure 1.1: Global average land-sea temperature anomaly compared to the average temperature during the years 1961 - 1990 [2].

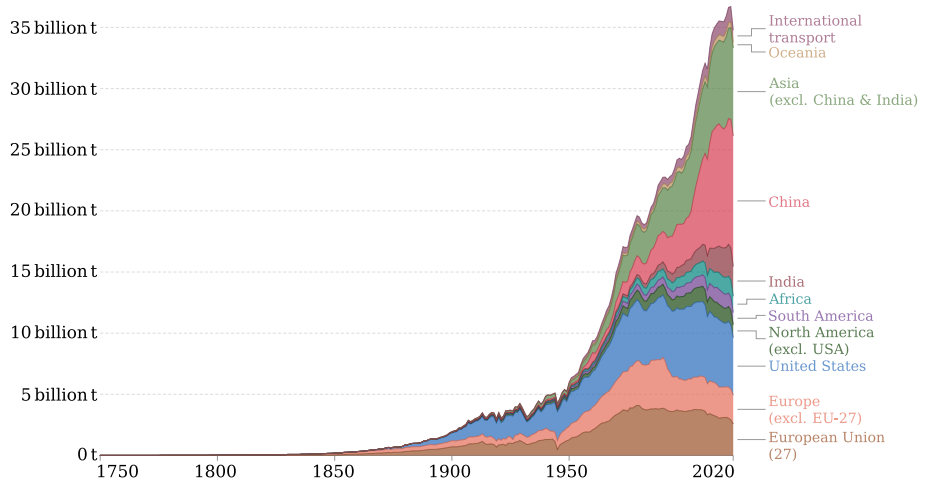


Figure 1.2: Annual CO_2 emissions generated from fossil fuels and cement production split by world regions [5].

The identification of these changes has led to the development of a number of adaptation strategies, including the Paris Agreement and the Kyoto Protocol [6, 7]. In order to mitigate climate change, a majority of the world's countries have committed to limit global warming to at least 2°C compared to the pre-industrial era by signing the Paris Agreement. To achieve this goal, greenhouse gas emissions have to be drastically reduced. Considering the emerging consequences of global climate change [8–10], the European Commission additionally announced the European Green Deal in 2019, which defines the goal of reducing net greenhouse gas emissions to zero in Europe by the year 2050 [11]. The German government has further targeted to reduce the total greenhouse gas emissions by 65% compared to the level produced in 1990 by as early as 2030 [12].
The integration of renewable energy sources and the reduction of fossil energy sources are indispensable in order to reduce the greenhouse gas emissions considering a globally increasing energy demand [13]. In addition, renewable energy sources are more evenly distributed globally compared to fossil fuels and thus can improve the independence in terms of energy supply [14, 15].

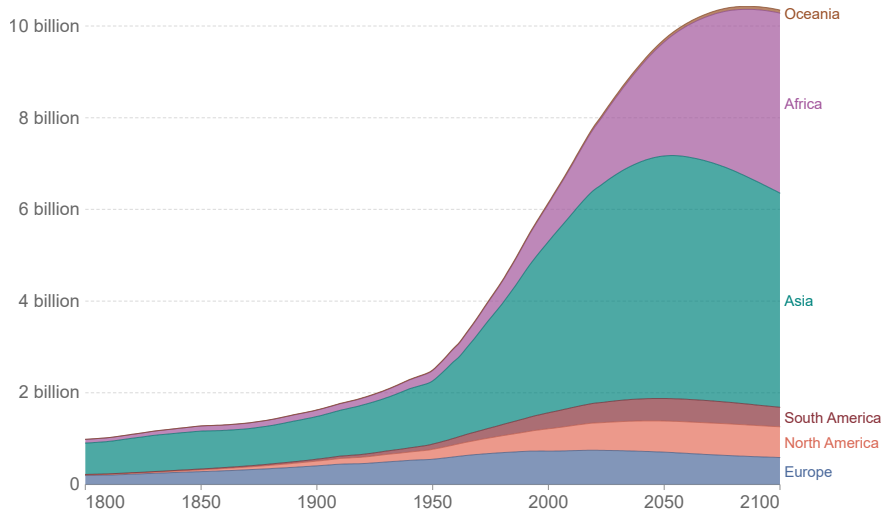


Figure 1.3: Population trends by world region based on historical estimates with future projections based on the UN medium fertility scenario. [2].

The intermittent nature of renewable energy sources and the time difference between energy supply and demand pose a significant challenge to their integration into the power grid [16–18]. Battery systems can play a key role in the transition to a sustainable energy generation, as they provide the possibility to compensate fluctuations and to supply mobile applications and portable devices [19, 20]. They are increasingly used in safety-relevant applications including electric vehicles, unmanned aerial vehicles, large scale systems for the power supply of industrial consumers or for grid stabilization, uninterruptible power supplies and home energy storage systems [21]. This results in sophisticated requirements for the battery system [22]. Reliability, availability, fail-safety, efficiency and durability of the battery system are prerequisites for the use in electric fleets and in systems to supply households or to support the power grid [23–25].
Advanced monitoring of the batteries is required to meet these requirements. Effective Battery Management Systems (BMSs) monitor battery operating parameters and contribute to the prevention of over(dis)charging, overheating, imbalance in charge levels, thermal runaway and fire hazards (Fig. 1.4). They play a critical role in improving the battery performance, safety and the effective service lifetime. The tasks include monitoring and control of the current battery operating parameters and ensuring that the battery is only operated within its Safe Operating Area (SOA).
Therefore BMSs provide

- measurements of operating parameters including temperature, voltage and current,
- state determinations, including State of Charge (SoC) and State of Health (SoH),
- data management and state calculation and
- communication interfaces.

The increasing demand for battery solutions leads to the development of new technologies aiming to achieve various improvements such as high cycle stability, increased capacity or reduced charging time [26]. The availability of used batteries also rises with an increasing number of batteries on the global market (Fig: 1.5).
How to reuse such batteries is one of the major challenges in lowering the environmental impact of batteries throughout their life cycle [27]. Batteries that no longer meet the requirements as an electric vehicle pack due to aging, i.e., decreased capacity, reduced dynamic and increased impedance, can find a second life in applications with less strict requirements such as stationary energy storage applications or off-grid microgrids [28]. Different usage histories result in heterogeneous cell parameters, which pose as a challenge for the second-life application.

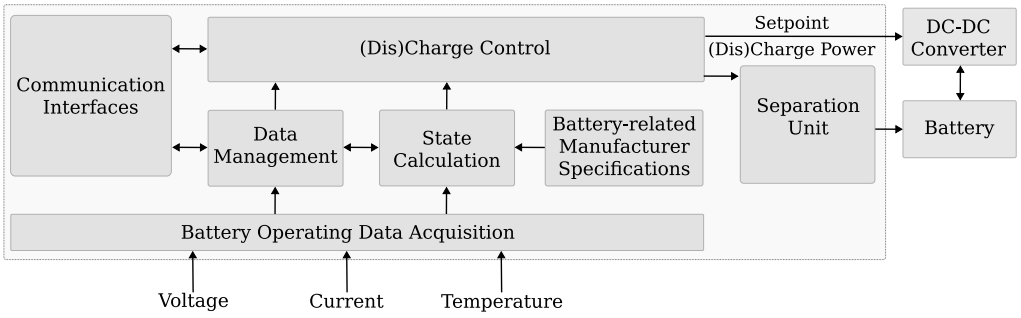


Figure 1.4: Block diagram of a battery management system.

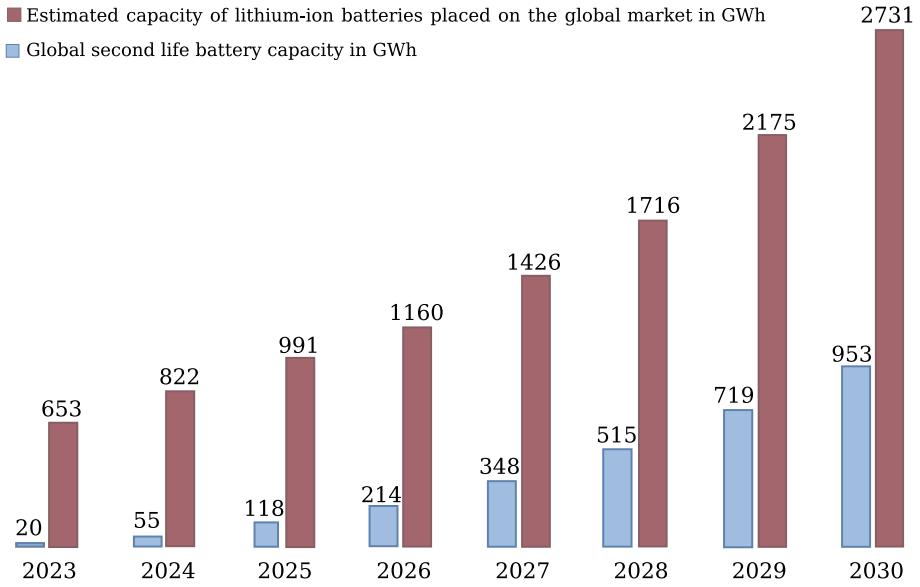


Figure 1.5: Forecast of global new lithium-ion capacity [29] and the available second-life battery capacity [30]: The increasing battery demand resulting from the integration of renewable energy sources along with the electrification of the transport sector leads to an increasing battery capacity in the global market. Besides, the availability of second life batteries is also rising. For comparison: In 2020, annual electricity net consumption in Germany was 511,590 GWh [31].

1.2 Determination of the Objectives

Heterogeneous battery systems integrate batteries with differences in cell chemistry, nominal capacity, SoH, SoC, and age aiming to unite the benefits of each battery technology and to provide second-life batteries a further application. Whereas the combination of different battery technologies can be advantageous in terms of control dynamics, control stability, reliability and availability, it is a challenging task to safely and reliably operate a variety of batteries with different cell chemistries and, in turn, with varying anode, cathode and electrolyte materials resulting in deviating SOAs.
In the context of this thesis, a DC system consisting of a variable number of heterogeneous batteries is investigated. In order to achieve sufficient battery capacities, they are connected in parallel. The parallel connection of batteries with different output voltage potentials endangers the safety, since high equalizing currents can occur between the components (Fig. 1.6) [32, 33].
The objective of this thesis is to develop a battery management system for a heterogeneous battery system, which considers both new and second life batteries with different cell chemistries and nominal capacities, aiming to improve reliability, availability, robustness, scalability, flexibility and optimized battery operation.
Reliability is defined in this context as ensuring availability of the battery system and fault-free operation even in the case of the failure of single components.
Availability describes the ontime and usability of the battery system in different operating states including the start-up of the system or during the maintenance.
Another challenge is to ensure *robustness*, which is defined as stability in the presence of disturbances, i.e. correct operation in the event of transients, sensor drifts or abrupt load changes.
Flexibility and *scalability* are further requirements to ensure that the applicability for a variety of applications. *Scalability* refers to a variable number of components that

can change even after initial implementation and which is restricted to a maximum number of 64 participating nodes.
Flexibility describes the possibility to combine any battery types and to integrate different loads and energy generators.
Optimized battery operation describes the consideration of various battery parameters in changing the (dis)charge current limit during operation with possible improvements in safety, availability and battery lifetime.
In the following, the terms *decentralized* and *distributed* are used to describe the architecture and operation of BMSs. Since the terms are not explicitly defined in the literature, a description of the terms as they are used within the scope of this thesis follows.
Decentralized BMSs are defined as systems consisting of individual batteries or battery cells which have their own independent monitoring and control unit. These units communicate with each other for managing the system tasks in a collaborative manner without relying on a centralized control unit. Each unit is thereby responsible for its own state monitoring, balancing, and safety management. In some application cases, communication takes place between modules, but all decision making and control is distributed throughout the battery system and performed by the local units. The main feature compared to other battery systems is the functionality without central control and, if necessary, without communication between the units.
Distributed battery management systems are characterized by the fact that the control of the system is divided among fully operational, functionally equivalent local units. The failure of individual local units does not endanger the system operation. In this case, the local units communicate with each other and are able to perform monitoring and control tasks independently. In contrast to decentralized BMSs, distributed BMSs use a central unit that collects data from the modules, provides control specifications, and coordinates and synchronizes the execution of system tasks. The central unit is functionally identical to the local ones, but is assigned additional rights. Distributed battery management systems thus represent a hybrid form of decentralized and centralized BMSs.

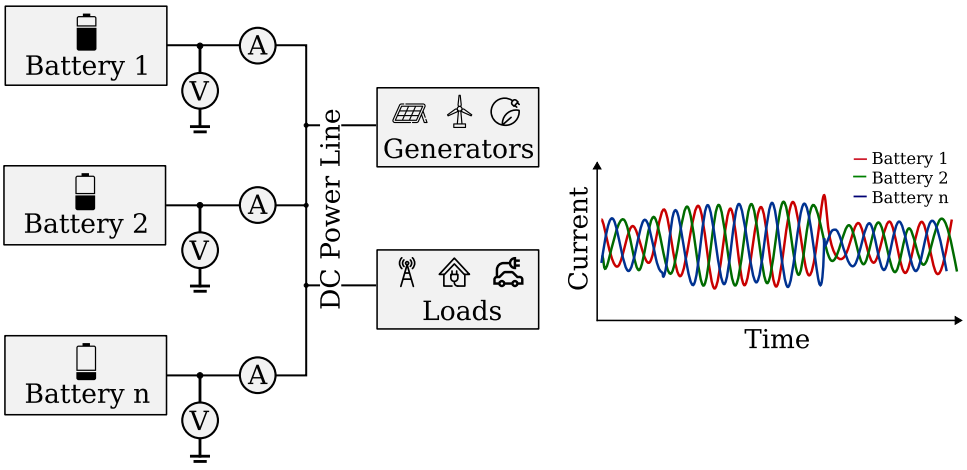


Figure 1.6: Exemplary representation of circulating currents: The parallel connection of batteries with different terminal voltages, for example due to different states of charge or fundamentally different output voltage potentials due to varying cell chemistry, often results in very high circulating currents between the components.

Decentralized systems give more autonomy to individual units, while distributed systems combine the distribution of the system control among several units with the advantages of central control regarding performance and safety optimizations.
The proposed BMS combines both architectures and therefore both terms are used to describe it.

1.3 Research Questions

In order to achieve the defined objectives in a heterogeneous battery system, a corresponding system architecture and appropriate control strategies are required. This results in the following main research questions:

1. Is a stable, decentralized battery system possible and is it technically realizable?
2. How can heterogeneity be managed and controlled in a decentralized manner?
3. How can such a system be designed for robustness and availability?

The research questions are addressed according to the applied research design method (Fig. 1.7). First, the requirements for the functionality and the objectives of the system to be developed are analyzed. In surveys of existing literature, distinctions from existing systems are defined and the open research questions are analyzed. In a next step, the requirements for the individual components of the system are analyzed. For the implementation, mathematical models of individual components are generated first. These are subsequently simulated and initial conclusions are drawn for the implementation of the system. With the hardware test-setup, mathematical models and the simulation can be validated. With the gained knowledge, models, simulations as well as hardware components can be further extended and improved afterwards. The research questions are answered by experimental data and their analysis.

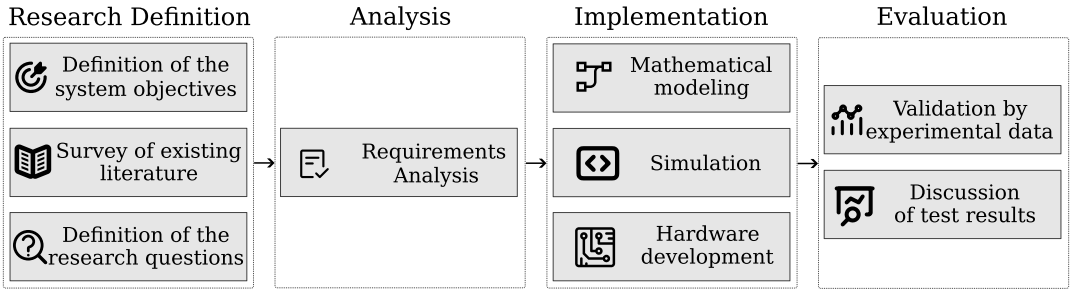


Figure 1.7: In the context of this thesis, the applied research design is applied.

1.4 Thesis Outline

The following thesis is structured in such a way that the individual chapters can be read both sequentially and largely independently of each other, in any order. To investigate the main research questions, it was necessary to examine a variety of fields, which influenced the structure of this thesis (Fig. 1.8). The chapters answer specified research questions and also include theoretical foundations and related work of the corresponding field. Each chapter begins with a brief motivation for considering the specific topic and concludes with a summary and recommendations

for future developments and further extensions. The chapters and their specific research questions are briefly described hereafter.

Chapter 2 gives an fundamental overview of the different types of battery cells divided into non-lithium-based, lithium-based and post-lithium battery cells. An analysis of the variation in anode, electrode, and electrolyte materials and a comparison of key performance indicators is provided. The safety risks and degradation mechanisms of batteries are reviewed. Operating parameters and states to consider to mitigate these are identified and the calculations or determinations thereof are described.

Chapter 3 analyzes existing battery management system architectures and categorizes them. The existing architectures are evaluated together with the control algorithms and the communication structures with regard to reliability, scalability and flexibility. The limitations of existing approaches are discussed, resulting in the proposal of a decentralized, scalable and reconfigurable battery management system. The proposed BMS is based on a distributed architecture with self-organized, locally controlled nodes. The chapter outlines the features, benefits, and challenges associated with this approach. In addition, it analyzes the requirements for the components of the decentralized BMS (DBMS).

Chapter 4 deals with the definition of the requirements for the communication and the selection of a suitable technology. The DBMS as a networked control system consists of sensors, actuators and controllers operating with a communication network as part of the control loop. The crucial role of the data rate and the reliability of the communication network is elaborated, as delays and message losses directly affect the system control. Relevant criteria for the technology comparison are defined. A comprehensive comparison of the communication technologies Controller Area Network (CAN), Controller Area Network Flexible Data-rate (CAN FD) and Ethernet is performed.

Chapter 5 introduces the concept of the leader election. One of the nodes is elected as the temporary leader, i.e., the central control unit, for task coordination within the system as a way to improve the collaboration among the multiple nodes. The emphasis of this chapter is on the development of a self-stabilizing algorithm for the leader election in dynamically reconfigurable bus topology-based broadcast systems. This algorithm features low message and time complexity of $\mathcal{O}(1)$. It provides a dynamic and criterion-based leader election to ensure effective task assignment and reduced failure rates. The system objectives are satisfactorily addressed in the implementation of the algorithm.

The performance and benefits of the selected system architecture and of the heterogeneous battery system are closely linked to the employed control strategies. **Chapter 6** therefore provides a comprehensive analysis of the requirements for the control strategy considering various operating states such as start-up, high fluctuations at the DC line, and safe shutdown. It addresses the effect of the system objectives and the decentralized architecture on the control system. A novel control scheme that allows switching between two inherently different control methods, a droop-based, decentralized and a communication-based, distributed one, is proposed. Switching between the control schemes is thereby accomplished in accordance of the actual operating state.

The analysis of the small-signal model, the knowledge of both, the static and dynamic characteristics of the DC-DC converter, and the derivation of the transfer functions are required as the basis for the controller design. In **chapter 7**, the small-signal behavior of a DC-DC converter in buck and in boost mode is analyzed for both the

Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) using the circuit averaging technique. The control and line to output transfer functions relevant for the average current control with outer voltage control loop are derived using the averaging equivalent circuits. In addition, the poles and zeros of these transfer functions are determined. The transfer functions, together with the poles and zeros, form the basis for the control analysis and stability considerations as well as for the controller design.
For the safe operation of heterogeneous batteries, it is necessary to limit the (dis)charge current depending on the battery state. In addition, it is required to convert the various terminal voltages of the different batteries to a common higher-level DC voltage level. **Chapter 8** first describes general approaches to control DC-DC converters. The selection of the control method is justified and the average current mode control with outer voltage control loop is developed on the basis of the transfer functions derived in chapter 7. Two controller implementations are realized and described, a hardware- and a software-based one. Accurate current and voltage control in buck and boost mode as well as in CCM and DCM are prerequisite for a stable system operation. Bode measurements using both, the hardware- and software-based controller implementation, validate the mathematical models and the derived transfer functions. Furthermore, they show the effect of the designed controllers.
Chapter 9 addresses the load current distribution control of the DBMS. Due to the parallel connection of heterogeneous batteries, load current distribution factors are required, which are adapted according to the actual state of the batteries during active operation and without influencing the control stability. In developing the load distribution control, the system-wide objectives, in particular robustness, reliability and availability, were taken into account. The realization of these objectives is achieved by introducing two different control approaches, which are presented in detail in this chapter. First, the established droop-based method is presented followed by a novel communication-based approach. The design of both control methods is described in detail, with particular emphasis on their respective characteristics.
Chapter 10 presents a method for a system-wide unambiguous battery state assessment of a variety of heterogeneous batteries considering the three operating states of charging, discharging, and storing. Thereby, the method offers the possibility to choose between a safe and an optimized battery operation depending on the available battery capacity. The value evaluating the battery state, the battery fitness value, is the basis for determining the battery state dependent current limiting factor (δ) and load current distribution factor (α), which in turn are used in the load current distribution control (chapter 9). A generic software template is presented for determining the battery fitness, which allows flexible and dynamic limit adjustments during operation.
Bidirectional DC-DC converters realize the power flow in charging and discharging direction and they are essential for the battery integration. Their modeling is helpful, especially for the design of larger, complex systems consisting of multiple DC-DC converters connected in parallel. Due to the high switching frequencies, the simulation of DC-DC converters requires increased computational effort. Therefore, in the **chapter 11**, three Modelica models of different complexity, accuracy and computational effort are proposed for a bidirectional DC-DC converter consisting of two phase-shifted half-bridges.
Chapter 12 presents a self-developed test framework for testing DC-DC converters and their control methods. It considers the communication line in the control loop and offers the possibility to steer different electronic loads and supplies. A software

test framework simulates several nodes of the DBMS and generates appropriate specifications for the hardware components (electronic loads, supplies and DC-DC converters). The specifications are processed within the test framework and the commands are sent via respective communication interfaces (CAN (FD), RS232). This enables the testing of different DC-DC converters with communication lines in the control loop using flexibly adaptable load and generation profiles.

Chapter 13 provides an overview of the hardware test setup implemented to demonstrate a proof of concept of the DBMS and to evaluate the functionality of the control and coordination strategies. Implementation details of the various hardware and software modules of the DBMS are discussed. The hardware components in this case consist of custom, commercially available hardware that has been adapted to meet the system requirements, as well as custom-designed printed circuit boards (PCBs) that have been implemented using commercially available components.

Chapter 14 presents experimental data to validate the DBMS architecture and the proposed control methods. The droop-based and the communication-based control methods in buck and boost modes are validated and analyzed. System start-up and switching between control methods are tested. The influence of an initial election process on the control is examined. Furthermore, the abrupt change in the values of the load distribution factors is investigated. For a first estimation of the system robustness and reliability, the influence of erroneous measurements and an unannounced shutdown of a DC-DC converter is assessed.

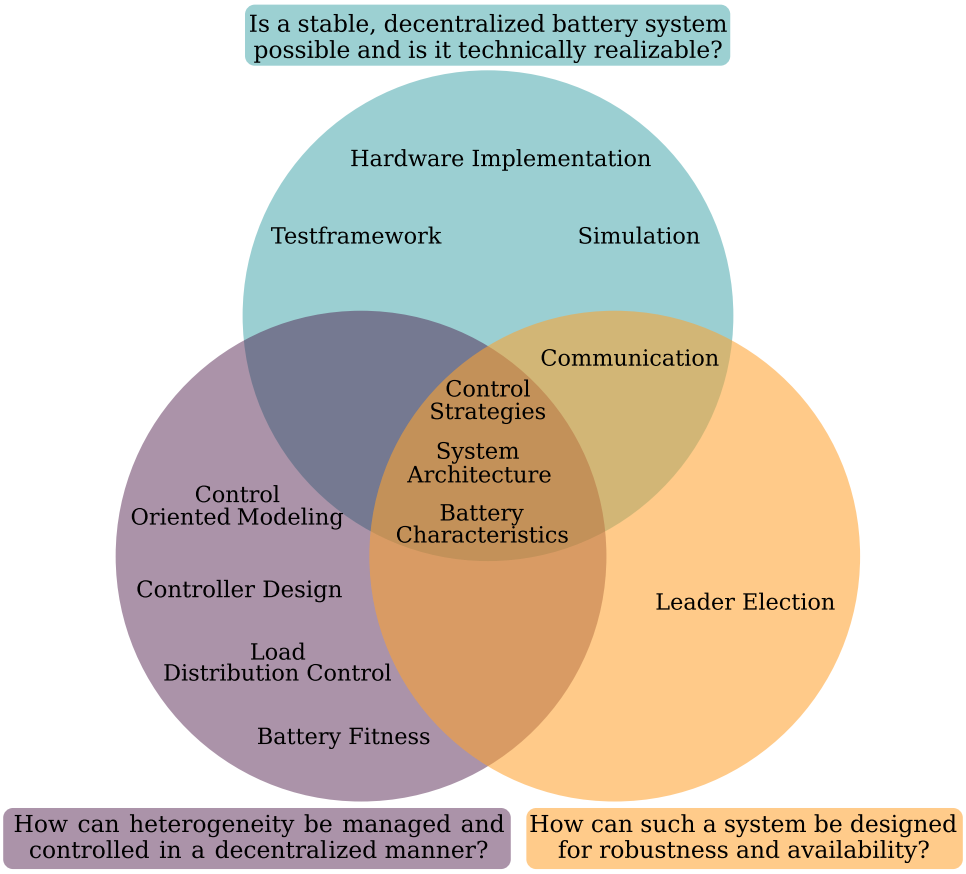


Figure 1.8: Assignment of the individual chapters to the research questions

1.5 Contributions

The main contributions of this work are summarized in the following:

- Overview of existing battery cells, their differences in the anodes, cathodes and electrolyte materials, comparison of performance indices and listing and description of the parameters relevant for safe battery operation.
- Introduction of a decentralized battery management system architecture for heterogeneous battery systems offering improved reliability, robustness, availability and reconfigurability as well as optimized battery operation.
- Analysis of the requirements for the communication in DBMSs, definition of the comparison criteria and comparative evaluation of a selection of available communication technologies.
- Implementation of a leader election algorithm for the selection of a central control unit with continued fulfillment of the system objectives of improved reliability and availability.
- Development of a control concept that switches between two control methods depending on the operating state to achieve increased reliability and control accuracy.
- Complete mathematical modeling of a bidirectional DC-DC converter including consideration of the continuous and discontinuous conduction mode as well as derivation of the transfer functions relevant for the average current mode control with outer voltage control and the load distribution control.
- Design of a novel, communication-based control for load current distribution between DC-DC converters connected in parallel, taking into account adaptable, battery state-dependent distribution factors.
- Hardware- and software-based implementation of the virtual droop-based control and the communications-based control as well as detailed derivation.
- Conceptual approach for a safe operation of heterogeneous battery systems considering various, and during operation variable, limits of the safe as well as the Optimized Operating Area (OOA) by the introduction of the battery fitness, a system-wide unique metric for the evaluation of the battery state considering the operating states charging, discharging and storing.
- Development of a test environment to control various electronic loads and supplies in order to test different DC-DC converters with a communication line in the control loop and variable load and generation profiles.
- Modeling of the bidirectional DC-DC converter on three different abstraction levels with differences in accuracy, scalability and computational effort offering the possibility to accurately simulate single components and to perform system simulations consisting of a number of parallel connected DC-DC converters.
- Development of a complete hardware test setup to demonstrate the functionality of the proposed architecture together with the control concepts. Various DC-DC converters allow the integration of different loads and batteries. Specially developed display units provide monitoring of the instantaneous current and voltage values and show the current state of the leader election. A load box controllable via CAN FD offers the possibility to connect and disconnect loads according to the available energy. A logging system enables data to be recorded for long-term evaluation.
- Execution of various test series and recording of these to demonstrate the improved accuracy and robustness of the proposed control method.

2

Battery Fundamentals and Characteristic Parameters

In this chapter, the basics of batteries are first described and the characteristic values to be considered for battery state evaluation and safe operation and their determination are defined. This forms the basis for the battery state-dependent load current distribution. An overview of currently used batteries and new technologies is given, with a particular focus on the key performance indicators.
Batteries belong to the electrochemical energy storage systems, whereby the energy is stored in chemical compounds of the electrodes. Each battery is composed of at least one electrochemical cell. An electrochemical cell consists of two electrodes separated by a certain distance. The space between the electrodes is filled with an electrolyte (Fig. 2.1). The positive electrode, the anode emits electrons and the negative electrode, the cathode absorbs them. The energy is stored in the individual compounds of which the anode, cathode and electrolyte are composed, e.g., in zinc or copper. [34]

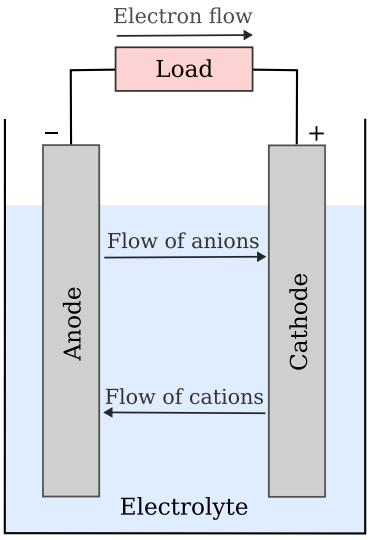


Figure 2.1: Basic structure of a battery cell [34].

Electrochemical cells and batteries are divided into two categories according to their operating principle: Primary cells and secondary cells. The primary cell is characterized by an irreversible chemical reaction. It is discharged only once and cannot be recharged. A secondary cell, in contrast, can be charged and discharged repeatedly. A reversible chemical reaction allows electrical energy to be stored and released again by the opposite reaction. In this work, only batteries consisting of secondary cells are considered. The cells can be further divided into non-lithium, lithium-based and post-lithium ones.

2.1 Non-Lithium Battery Cells

The non-lithium based cells were mainly used before the market introduction of lithium-ion batteries and are divided into *aqueous electrolyte batteries*, *high temperature batteries* and *redox flow battery systems* [35].

Aqueous Electrolyte Batteries

Among the *aqueous-based electrolyte* batteries, the three mostly used battery cell technologies are

- Lead-Acid (LA)
- Nickel-Cadmium (NiCd) and
- Nickel-Metal-Hydride (NiMH).

They are still common in various commercial applications, although they are increasingly replaced by lithium-ion battery systems. Lead-acid and nickel-cadmium batteries are nearly eliminated from the portable market due to environmental concerns and the use of hazardous heavy metals, but they are still used for industrial applications and in the drive system. In particular, for Starting Lighting Ignition (SLI) in internal combustion engines, lead-acid batteries are still state of the art.
Nickel-metal hydride device batteries exhibit higher energy densities compared to nickel-cadmium batteries and they are more environmentally compatible. They are still commonly used in portable devices, where they mostly serve as a replacement for alkaline primary cells. Furthermore, they are still the predominant battery technology in power-assist hybrid vehicles.

High-temperature Batteries

High-temperature batteries are operated at temperatures (T) around 300 °C and are characterized by their energy storage capacity and their energy densities, comparable to those of lithium-ion batteries.
The key representatives of high-temperature battery systems are

- Sodium-Sulfur (NaS) and
- Sodium-Nickel-Chloride (Na-$NiCl_2$).

They were originally developed for electric vehicles and traction applications, but have not gained widespread acceptance due to various technical, safety and economic drawbacks. They are still used sporadically in traction applications, e.g. in electric buses or in stationary applications.

Redox flow Batteries

Redox flow batteries are also aqueous systems. The energy conversion is similar to fuel cells. The conversion between electrical and chemical energy occurs when the liquid electrolytes are pumped from storage tanks to the flow electrodes. The electrolytes flowing through the cathode and anode are often distinct and are referred to as anolyte and catholyte, respectively. An ion-conducting separator between the electrodes prevents the two electrolytes from mixing. Redox flow batteries have a comparable energy density to lead-acid batteries with a significantly longer service lifetime. They are also characterized by their ability to store large amounts of electrical energy relatively cost-effectively and efficiently, making them one of the preferred storage systems for medium- and large-scale applications, including grid-scale ones. [35]

2.2 Lithium-based Battery Cells

Lithium-based rechargeable cells offer high energy and power density without memory effect and presently dominate the battery market. Depending on the basic cell chemistry (Fig. 2.2, Table 2.1), lithium-based batteries are further subdivided into lithium-ion and lithium-metal batteries (Fig. 2.2). Additional categorizations are made according to the applied electrode (Figs. 2.3, 2.4) and electrolyte (Fig. 2.5) material. The electrode material properties influence the cell potential, the capacity and the energy density. The stability of the structure of the electrode materials and the nature and stability of the electrode-electrolyte interfaces affect cycle life, effective service lifetime and safety. [36]
Table 2.1 shows battery-powered applications and their most commonly applied electrode materials as well as their electrical properties. In the following, the key characteristics of selected, commonly used (Tab. 2.1) lithium-based electrode materials are summarized.

Lithium-cobalt-oxide (LCO)

Lithium-cobalt-oxide (LCO) electrodes are characterized by high cycle stability (over 500 cycles with $80-90\%$ capacity retention), low self discharge rates, a moderate gravimetric capacity (C_{grav}) (theoretical $C_{\text{grav}} = 274\,\frac{mAh}{g}$, experimental $C_{\text{grav}} = \approx 140\,\frac{mAh}{g}$) and a superior volumetric capacity (C_{vol}) (theoretical $C_{\text{vol}} = 1363\,\frac{mAh}{cm^3}$). They are among the most commonly used electrode types in lithium-ion batteries. The technology is considered mature and safe for consumer applications in portable devices. Compared to other electrode materials, LCO battery cells have a relatively short lifetime, low thermal stability and lower charge capacity. Therefore, they are not used in electric vehicles. A further drawback is that cobalt is associated with environmental and toxic hazards. [34, 36, 43–45]

Nickel-manganese-cobalt-oxide (NMC)

For high energy and high performance applications, such as electric vehicles, cost, safety and performance of the battery cells used are key factors. Nickel-manganese-cobalt-oxide (NMC) electrodes combine improved safety with lower cost compared to LCO electrodes without significantly compromising performance (theoretical $C_{\text{grav}} = 190\,\frac{mAh}{g}$, experimental $C_{\text{grav}} \approx 154\,\frac{mAh}{g}$). Furthermore, they are characterized

Table 2.1: Applications, commonly used electrode materials therein and their electrical characteristics. [37–42]

Application	Cathode Chemistry	Nominal Cell Capacity (C_N)	Output Voltage (V_{out})	Total Energy
Cell Phones	LCO, NMC	2-4 Ah	4 V	8-16 Wh
Laptops	LCO, NMC, LNO	3-4 Ah	8-16 V	24-60 Wh
Hybrid Electric Vehicles	NMC, LNO, LMO, LFP	4-30 Ah	48-150 V	0.5-15 kWh
Electric Vehicles	NMC, LNO, LMO, LFP	4-80 Ah	300-800 V	15-100 kWh
Heavy Duty Vehicles	LFP, NMC	40-80 Ah	400-800 V	100-400 kWh
Home Storage Systems	NMC, LNO, LMO, LFP	4-40 Ah	100-200 V	3-10 kWh
Industrial Storage Systems	NMC, LFP	30-80 Ah	200-800 V	100-500 kWh
Grid-scale Storage Systems	NMC, LFP	60-80 Ah	800 V	2000-30000 kWh

by operation over a wide voltage range, sufficient structural and thermal stability, average cycle life and high specific energy density ($150 - 220\,\frac{Wh}{kg}$). [34, 36, 46, 47]

Lithium-nickel-oxide (LNO) and Nickel-cobalt-aluminum-oxide (LNO)

Considering the sustainability of a battery cell, a high recycling efficiency and low environmental risks are essential. In further developments, efforts are made to partly or entirely replace cobalt as a cathode material using alternative transition metals such as manganese or nickel. Lithium-nickel-oxide (LNO) electrodes have a higher specific capacity (experimental $C_{grav} \approx 170\,\frac{mAh}{g}$) compared to lithium cobalt oxide (LCO) ones. A disadvantage is the low thermal stability, which results in safety concerns. A further development is the electrode material lithium nickel-cobalt-aluminum-oxide (LNO) (experimental $C_{grav} \approx 188\,\frac{mAh}{g}$). The addition of cobalt and aluminum-oxide improves stability, although safety concerns at high operating temperatures remain. The thermal stability especially in a charged state is limited and LNO electrodes experience moisture sensitivity. Battery cells with LNO electrodes exhibit high specific energy and power density and high cyclic lifetime, making them suitable for the use in electric vehicles. Typically, LNO electrode materials are combined with other materials such as LFP and LMO to increase safety. [34, 36, 48–50]

Lithium-manganese-oxide (LMO)

Battery cells with lithium-manganese-oxide (LMO) electrodes are characterized by higher temperature resistance, improved chemical stability, increased safety,

environmentally friendly and abundant materials, and lower cost compared to lithium cobalt oxide. They have a gravimetric capacity (C_{grav}) of about 120 $\frac{mAh}{g}$, resulting in 10% up to 20% lower energy densities compared to lithium-cobalt-oxide (LCO) electrodes. The architecture forms a three-dimensional spinel structure that improves ion flow at the electrode. This results in lower internal resistance and improved electron absorption, enabling charging with high currents (20 A to 30 A, current pulses up to 50 A). Structural changes at elevated temperatures result in poor cycling and storage stability. Battery systems based on LMO electrodes can be optimized for either optimum longevity, maximum load current (specific power), or high capacity (specific energy). A combination of the electrode materials lithium-manganese spinel with lithium-nickel-manganese-cobalt oxide (NMC) increases the specific energy and improves the lifetime. Most of the battery systems used in electric vehicles are based on a combination of LMO and NMC. [34, 36, 51]

Lithium iron phosphate (LFP)

Lithium iron phosphate (LFP) electrodes offer stable output voltages over a wide range of states of charge, excellent thermal and chemical stability, environmental friendliness, cost efficiency, high safety and long cycle life. Furthermore, lithium iron phosphate withstands high temperatures without decomposing and is quite stable under overcharge and short circuit conditions. If not handled properly, the phosphate-based material will not burn or release oxygen, thus preventing thermal runaway. A drawback is the about 15% lower energy density compared to the one of LCO. [34, 36, 44, 52–54]

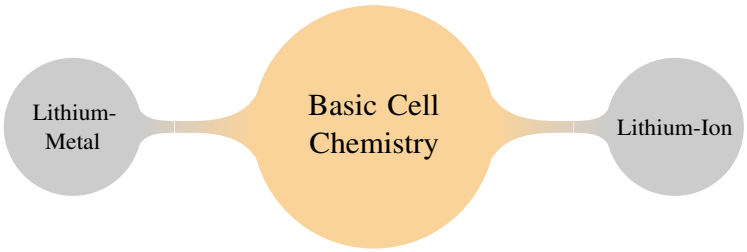


Figure 2.2: Lithium-based cells are divided into lithium-ion and lithium-metal cells according to their basic cell chemistry.

2.3 Further Improvements of Lithium Battery Cells and Alternative Battery Technologies

Lithium-ion batteries are currently the most advanced electrochemical energy storage technology due to their energy density and performance. With the goal of further reducing cost, improving performance, and increasing energy density, lithium-ion technologies continue to be investigated and developed. In the following, a brief overview of a selection of improvements of lithium technologies and alternative battery technologies is provided [26, 145]. These further battery developments are often called post-lithium battery technologies in the literature [145–148], describing new battery cell types overcoming challenges of lithium-ion battery cells and improvements of lithium-based battery cells. These can be divided into further developments in electrode materials and the development of new cell types.

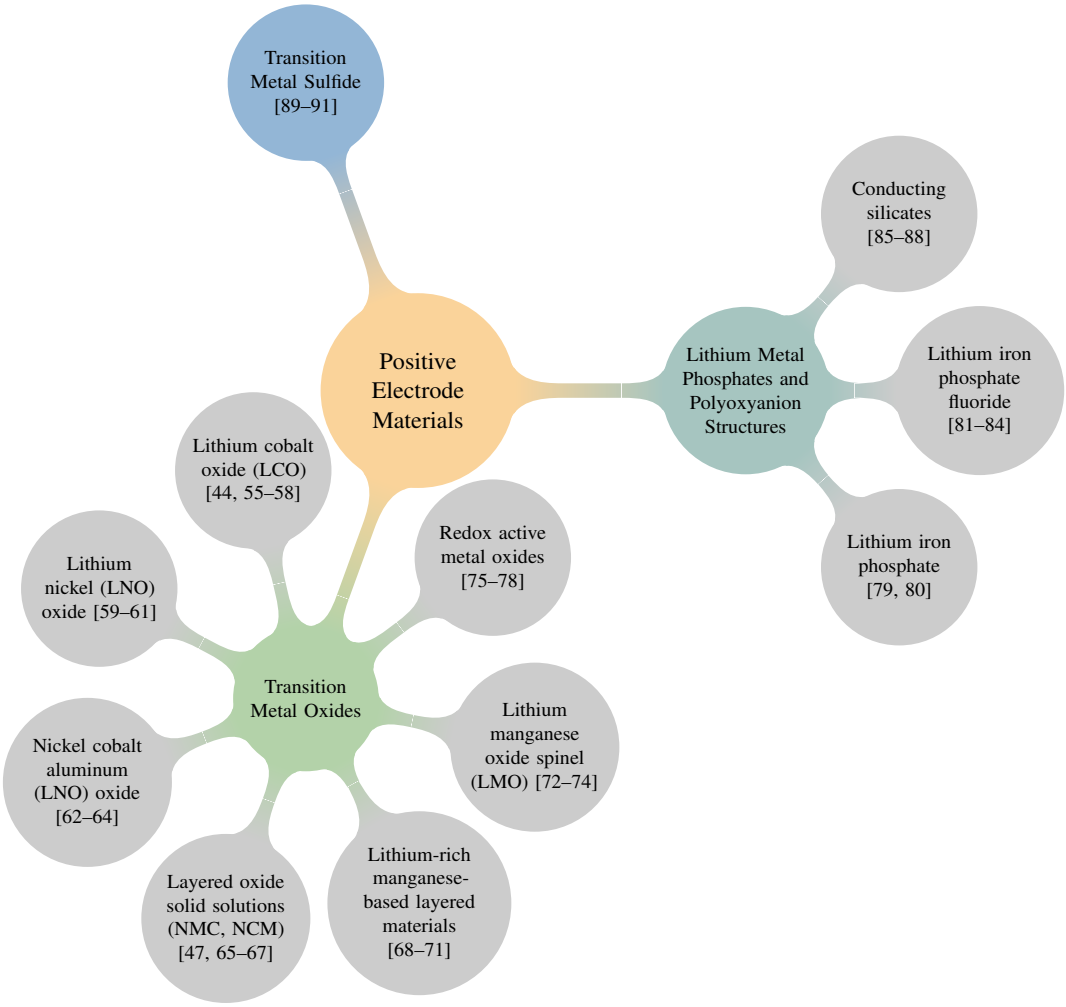


Figure 2.3: Overview of positive electrode materials of lithium-based cells.

Silicon anodes

Silicon provides an around ten times higher specific capacity (theoretical capacity: $\approx 4000\,\frac{mAh}{g}$) compared to the currently most common anode material graphite and a promising operating voltage. However, its application as an anode in post-lithium-ion batteries faces significant challenges, especially in terms of cyclability. Silicon anodes experience large volume expansion (up to 400%) during lithiation, leading to mechanical failure of the anode structure and instability of the Solid Electrolyte Interphase (SEI). A number of approaches exist to improve cyclability. Electrode structures that buffer the volume expansion of Silicon by conductive nanoporous structures show remarkable improvements in cyclability. Furthermore, new electrolyte materials that prevent the particles from detaching from each other and form elastic SEIs have been investigated. Due to the numerous developments and improvements, silicon anodes are now on the verge of commercialization. [145, 149, 150]

Layered nickel-rich and lithium- and manganese-rich cathode materials

Layered nickel-rich and lithium- and manganese-rich cathode materials offer high energy density, low cost, higher (dis)charge capacities and environment friendliness. They provide a higher specific capacity compared to the conventional lithium cobalt

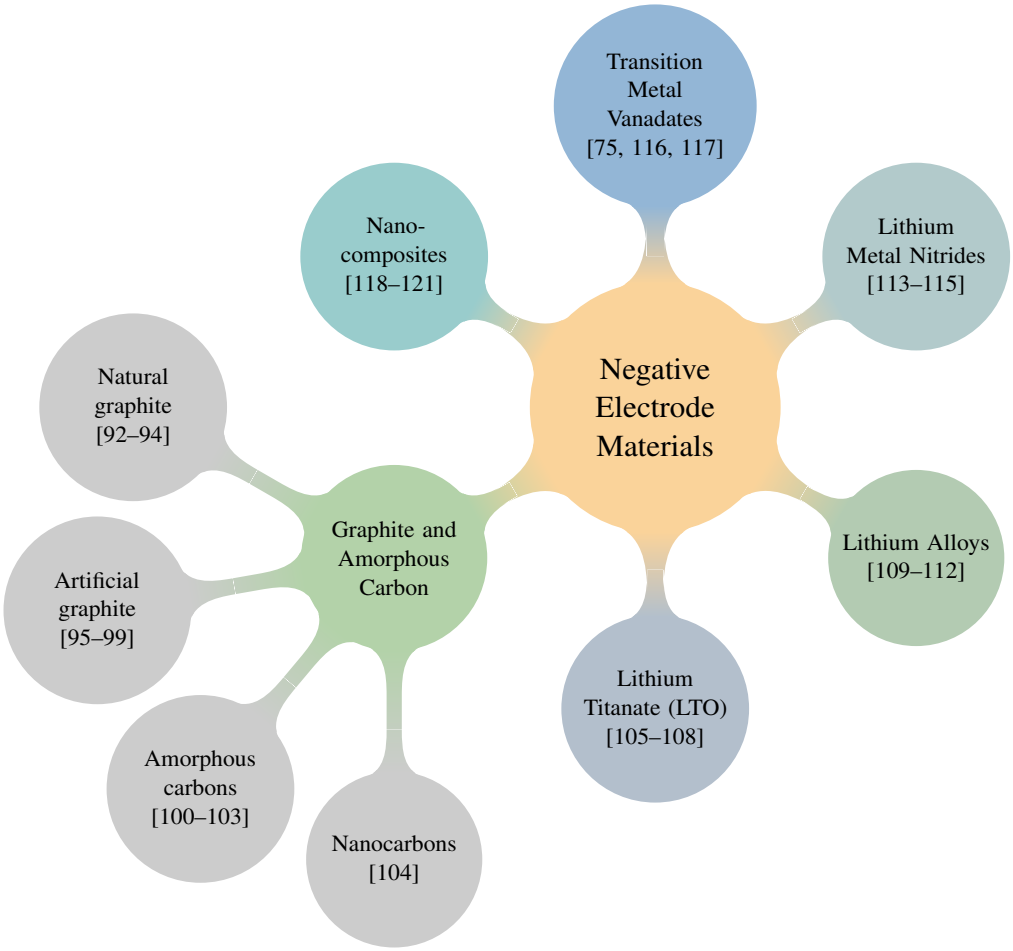


Figure 2.4: Overview of negative electrode materials of lithium-based cells.

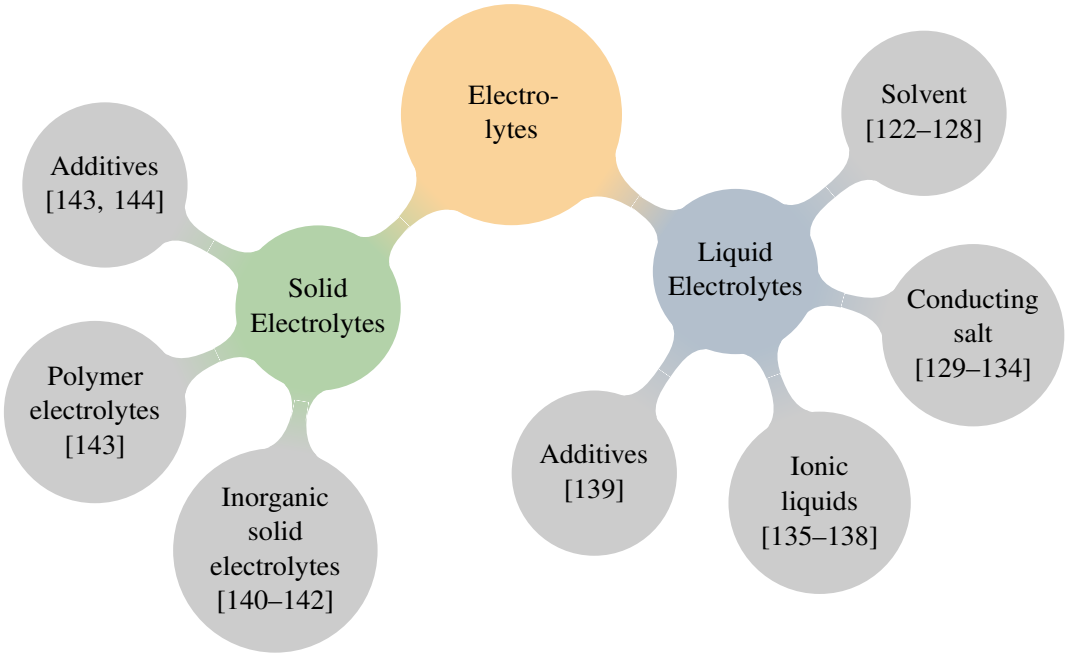


Figure 2.5: Electrolytes for lithium-based cells can be divided into liquid and solid. The respective ectrolyte groups further differ in the selected materials and their composition.

oxide (LCO) cathode material. In fact, these materials are already included in commercial products. Despite the increased capacity (theoretical capacity: 300 $\frac{mAh}{g}$),

they suffer from structural degradation and instability caused by an unstable interface (SEI). Furthermore, severe voltage and capacity drops occur during discharge, especially at high temperatures resulting in a poor cycling performance. Ongoing research is addressing the improvement of cyclability and stability as well as the potential use in high voltage application, e.g., electric vehicles. [145, 151–153]

Lithium-metal anode

Lithium metal as anode material offers high specific capacity (theoretical capacity $3860\,\frac{mAh}{g}$) and low redox potential, which makes it promising for next generation batteries. The commercialization and widespread use of lithium metal anodes is still hindered by the strong dendrite formation at the surface, which leads to poor interfacial stability and safety issues. In addition, extreme volume variations occur during cycling. To suppress dendrite growth, various coating materials such as glasses and composites are investigated and electrolyte materials are under further research. [154–156]

Battery Technologies

Table 2.2 shows four common post-lithium battery technologies. Lithium-sulfur batteries, solid-state batteries, and lithium-air batteries use lithium-metal anodes, which promise high energy content. Nevertheless, the described challenges of lithium metal anodes equally apply in these cases.
Metal-ion concepts are a replication of lithium-ion battery technology using alternative charge carriers, with sodium-ion being one of the most promising technologies. Sodium-ion batteries are considered to be an alternative technology for lithium-ion batteries and could gain importance if limited resources, such as lithium supply, become an issue in the future. Sodium-ion batteries have similar electrochemical properties compared to lithium-ion batteries, which promises rapid progress. The basic physical and chemical principle of these batteries is based on the electrochemical reaction between sodium ions at the anode, which is usually made of hard carbon as graphite is inactive towards Na-ions, and a cathode material during the discharge and charge cycle, similar to lithium-ion batteries. Challenging is the size of sodium ions compared to lithium ions, which leads to significant differences in crystal structure and intercalation behavior. The difference in the ionic radius of the shuttling ions means that different physical properties of the ion storage materials, solvents and salts are required for the electrolyte. The choice of anode is limited to hard carbon, which offers capacities of over $300\frac{mAh}{g}$ and shows promising performance. [157]
The possibility of producing hard carbon from biowaste increases the sustainability of the batteries [158]. However, it suffers from an irreversible loss of capacity after the first cycle, reducing the achievable energy density [159]. Sodium salts have a higher solubility which leads to serious interfacial instability problems. This leads to rapid decomposition of the electrolyte and reduces cycle life. In addition, the migration of soluble species to the cathode leads to self-discharge. [160]
Possible fields of application for sodium-ion batteries are limited to large energy storage systems and light vehicles for short-distance transportation due to the lower energy density. Sodium-ion batteries with sodium layered transition metal (TM) oxides (Na_xTMO_2) as cathode material exhibit an energy density comparable to the one of lithium-ion batteries with the potential to reduce costs, increase energy density, cycling stability, and improve the safety [161].

Lithium-sulfur batteries are characterized by high specific energy (currently $\approx 400\,\frac{Wh}{kg}$), which is continuously increased by optimizing the electrode architecture and minimizing the excess electrolyte. They have limited cyclability and high self-discharge rates and are therefore likely to be limited to specific applications such as aerospace where high gravimetric energy density is the key criterion. A further challenge is the electrolyte consumption at the anode-electrolyte interface, which causes electrolyte detypletion [162]. The necessity for an excess of electrolyte and lithium in the cell reduces the gravimetric and volumetric energy density. Improvement of the lithium-sulfur battery technology relies on the development of a stable and reversible lithium-metal electrode [163, 164]. Furthermore, a stable electrolyte system is necessary for improved stability of the anode-electrolyte interface [165, 166]. The realization of a stable lithium anode can further improve specific energy, energy density, safety, and power performance [167].
Another disadvantage are insoluble polysulphides, which tend to inhibit precipitation at the lithium metal anode, leading to material loss and impedance increase. Exceeding a certain sulfur loading leads to polysulfide shuttling at the anode and to an increase in the total current density at the anode and cathode, which in turn accelerates the growth of lithium dendrites. The addition of new solvents and additives over and above lithium nitrate is crucial for electrolyte adjustment and thus for reducing anode corrosion. The solid-state electrolyte based on sulfidic inorganic glasses is the one promising concept to achieve adequate performance [168, 169].
Solid-state batteries have higher energy content ($\approx 350\,\frac{Wh}{kg}$) achieved by using lithium metal and improved safety by implementing a non-flammable solid electrolyte. Possible electrolyte versions are polymers, inorganic (sulfidic or oxidic) electrolytes or a hybrid electrolyte, which is a combination of the three. Regardless of the electrolyte, the electrochemical performance (energy, power, lifetime) remains lower compared to lithium-ion batteries.
Lithium-air batteries exhibit challenging technical issues, including clogging of the air electrode during operation. The potential achievable energy content is outstanding high (currently $\approx 1200\,\frac{Wh}{kg}$ up to $\approx 3500\,\frac{Wh}{kg}$ and peak energy densities of $\approx 4000\,\frac{Wh}{kg}$ [170–172]).

2.4 Reuse of Second Life Batteries

Over the service life of batteries, degradation mechanisms lead to a loss of capacity and increasing internal resistance, among other things. If the remaining capacity of the battery is approximately less than 80% of the nominal capacity (Fig. 2.10 on p. 29), in some applications, such as electric vehicles, it is declared, that the battery reached its end of life.
Accelerated, non-linear aging of the vehicle battery occurs approximately from that point [185, 186]. While the batteries can no longer be used for applications with high requirements in terms of dynamics and capacity as well as high load current demands, they can still be used as energy storage in systems with reduced requirements (second life application). Due to the reduced load in second life applications, the entire battery service life can be extended, which has a positive impact on the ecological and economic aspects of the battery.
Besides the evident advantages of using second-life batteries, such as reduced costs, less waste and conservation of scarce resources, there are still significant challenges. Before reusing the second life batteries, it is necessary to detect their

Table 2.2: Overview of a selection of common post-lithium battery systems, their key advantages and disadvantages as well as their gravimetric capacity [26, 145].

Technology	Capacity	(Dis)Advantages
Lithium-sulfur battery [173, 174]	1675 $\frac{mAh}{g}$	+ high theoretical gravimetric energy density (E_{grav}= 2600 $\frac{Wh}{kg}$) + low cost and natural abundance of materials – small volumetric energy density (283 – 314 $\frac{Wh}{l}$) – limited cycability – large excess of electrolyte required – large volumetric expansion of sulfur after lithiation (80%) – shuttling effect of lithium polysulfides → limits electrochemical performance – high self-discharge rates
Solid-state batteries [175–177]	155.7 $\frac{mAh}{g}$	+ higher gravimetric energy density (up to $E_{grav} \leq$ 350 $\frac{Wh}{kg}$) + enhanced safety by replacing liquid flammable electrolytes with solid, non-flammable ones + reduced lithium dendrite growth + selected systems offer a wide temperature range + high cycle stability + high energy density with lithium metal – poor ionic conduction in solid electrolytes – uncertain material and processing costs – promising chemistries not yet decided – lower electrochemical performance (including energy, power, service lifetime) compared to LIBs
Lithium-air battery [178–180]	10000 $\frac{mAh}{g}$	+ most appealing potentially attainable gravimetric energy density ($E_{grav} \approx$ 3505 $\frac{Wh}{kg}$) – low long-term cyclability and (dis)charge efficiency – poor energy efficiency due to pronounced voltage hysteresis – sensitive to air impurities – open technical challenges including pore clogging of air electrode – promising chemistry not yet decided
Sodium-Ion batteries [181–184]	349 – 445 $\frac{mAh}{g}$	+ low cost, easy exploitation and natural abundance of the material + promising for large-scale systems + electrolytes with lower decomposition potentials are used due to higher potential (0.3 V higher than the one of LIBs) resulting in improved safety + no overdischarge characteristics → discharge to zero volts and maximization of energy density – low specific capacity – lack of lightweight materials – moderate volumetric and gravimetric energy densities – promising chemistries not finally decided

state of degradation. This in turn cannot be measured, as there are a number of different degradation mechanisms, some of which lead to apparent capacity loss, while other degradation mechanisms occur without capacity loss, but still affect the use of the batteries [187]. Estimates of the degradation therefore require the usage history of the battery. Measurement data collection and management is part of the battery management system. Consequently, for an improved integration of second life batteries, BMSs with usage history recording are required.
A concise summary of the challenges for the life cycle strategy of second-life batteries is given in [188]. The entire process for the integration of second-life batteries is considered and obstacles in the individual process steps are presented, including technical, economic and legal obstacles. Regarding the battery management system for second life batteries, the necessity for balancing due to larger performance differences is highlighted [188].
An assessment of the feasibility of second-life battery applications and a derivation of the key technologies required for improved integration was described in [189]. These technologies include automated battery disassembly and inspection, rapid screening and sorting, non-destructive testing and data-driven forecasting. This article also emphasizes the need to collect battery usage data. Furthermore, the service life of the batteries in their second life application is identified as a key factor regarding the cost-effectiveness. For a longer service life and minimized degradation, improved strategies for monitoring the degradation rate and a battery management system that can dynamically adjust the limit values for the (dis)charge current and the (dis)charge depth are proposed. [189]
Summarizing, the key requirements for improving the integration of second life batteries regarding the BMS are the recording of the battery usage history and adjustable (dis)charge current and depth in order to further limit the battery operating area.

2.5 Battery Safety Risks and Safe Operation

Unsafe operating conditions and external disturbances destroy the battery and can lead to safety hazards such as thermal runaway and fire, particularly in the case of lithium-ion based cells. Battery safety hazards (Fig. 2.6) can be divided according to their cause into

- mechanical (case damage, compression, and twisting of cells),
- thermal (thermal shock, localized heating, thermal runaway),
- electrical (over(dis)charge, short circuit), and
- electrochemical (solid electrolyte interface (SEI) decomposition, oxygen release followed by a blow up, parasitic electrolyte–electrode side reactions).

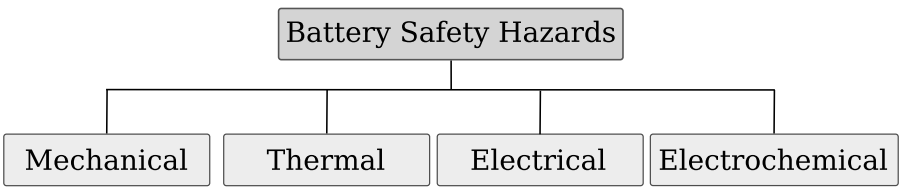


Figure 2.6: Overview of battery safety hazard categories.

To reduce the risk of battery safety hazards, it is necessary to keep the battery within its Safe Operating Area (SOA) (Fig. 2.7).

Battery damage and safety hazards occur when the battery voltage exceeds or falls below defined limits. During charge, a maximum voltage limit must not be exceeded, and during discharge, the voltage must not fall below a defined minimum value. The same applies to the operating temperature. In lithium-ion batteries, only Li+ ions shuttle occurs at the cathode and anode during the approved voltage and temperature ranges. High temperature and high voltage operation in contrast can cause side reactions including decomposition of the solid electrolyte interface, oxygen release on the cathode side, and additional parasitic electrolyte–electrode side reactions. The decomposition of the solid electrolyte interface film accelerates the rise in internal temperature and increases the risk of oxygen release on the cathode side. Eventually, these reactions lead to thermal runaway.
The charge current and the State of Charge (SoC) must also be kept within certain limits. Operating lithium-ion based batteries at higher currents increases the likelihood of failure due to mechanical stress generated in the battery during cycling, but also stimulates lithium plating during the charge process. A combination of low temperature, high SoC, high charge current and high cell voltage significantly increases the risk of lithium plating, which reduces the usable battery capacity and leads to power fading.

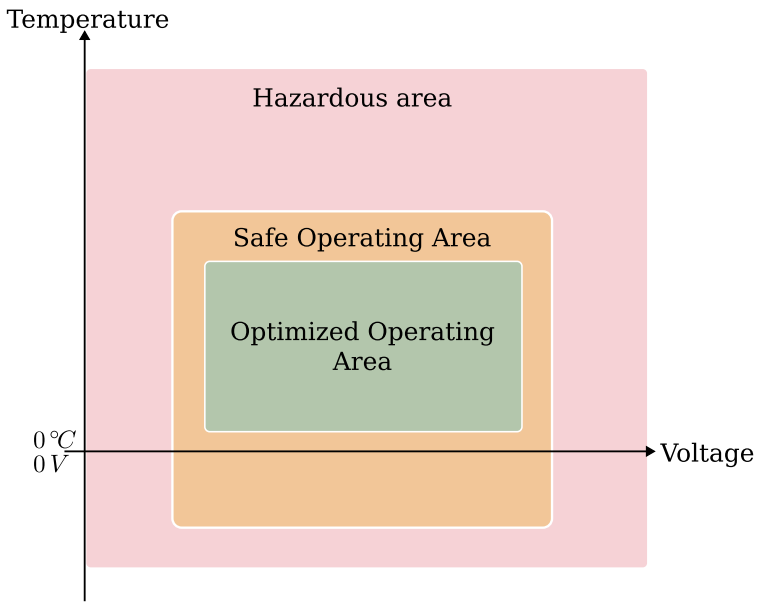


Figure 2.7: Subdivision of the operating areas into optimized operating area (OOA), safe operating area (SOA) and hazardous area. For safe operation of the batteries, the limits of the SOA must be observed, whereby these vary for each battery depending on the cell chemistry and design. Operation outside the SOA poses a significant safety risk. Further reduction of the SOA enables the OOA, whereby the limits in this case are depending on the battery cell and they have to be adjusted individually.

Considering the permissible operating areas, it is necessary to distinguish between the safe operating area and the optimized one (Fig. 2.7). Violation of the limits of the safe operating area leads to critical operating conditions, which can result in the destruction of the battery and entail associated hazards. The optimized operating area defines limits to restrict battery degradation.
Battery degradation is indicated by a decrease in capacity and an increase in internal resistance followed by power fade. Capacity degradation implies the loss of usable (dis)charge capacity due to internal mechanisms, such as lithium plating in lithium

ion based batteries. Capacity fade is induced by certain stress factors such as high or very low temperatures or high (dis)charge currents.
The internal resistance affects the ability of the battery to effectively release stored capacity and to dynamically respond to high load changes. An increase in internal resistance leads to a decrease in performance and can further lead to increased battery temperature and voltage drop under load.
Battery degradation occurs not only during cycling but also during storage and cannot be fully avoided. It can only be limited by avoiding stress factors such as adverse temperatures and state of charge ranges. This is achieved by the prevention of exceeding or falling below certain limits.
Exceeding the optimized operating range leads to operating conditions that accelerate battery degradation without immediate danger or direct destruction of the battery.
Battery management systems (BMS) control compliance with the safe operating range and strive for the optimized operating range. For this purpose, they perform the necessary measurements and corresponding state determinations to evaluate the battery condition. [190, 191]

2.6 Battery Parameters, State Indicators and Required Measurements for the Estimation of the Battery Condition

Characteristic parameters for battery state assessment and their determination are described subsequently. Accurate battery state determination is the basis for safe operation and further optimization, such as the reduction of operation-related degradation.
The amount of electric charge ($Q(t)$) delivered from a source such as an electrical energy storage system is

$$Q(t) = \int_{t_0}^{t} i(t)dt \tag{2.1}$$

where t is time. For batteries, the capacity is expressed in ampere-hours (Ah). Assuming full utilization of active materials, batteries have a theoretical capacity (C_T), which is calculated using Faraday's law

$$C_\mathrm{T} = \frac{n \cdot F}{3600 \cdot Mw} \frac{Ah}{g} \tag{2.2}$$

where n is the number of charge carrier, F is the Faraday constant and Mw is the molecular weight of the active material used in the electrode.
Under real conditions, only a part of the active material is used and ambient conditions including e.g., the discharge rate and the temperature, determine the actual available capacity of the battery. The nominal capacity (C_N) is defined by the manufacturer under certain conditions, i.e. the amount of charge delivered by a fully charged battery under certain temperature and charging conditions.
The actual capacity (C_act) is the maximum available capacity and is used to calculate the State of Charge SoC and the State of Health SoH. The released capacity (C_rel) is the capacity that is released during discharge. The remaining capacity (C_rem) is the

available capacity after discharge, so basically

$$C_{\text{act}} = C_{\text{rem}} + C_{\text{rel}} \tag{2.3}$$

2.6.1 Thévenin Equivalent Circuit Model of Batteries

Battery models are required to perform battery state estimations and to predict the short-term behaviour of voltage and current during the (dis)charge of batteries. Battery models are used for simulation and state determination. They can be basically divided into electrochemical models and equivalent circuit models, whereby the latter ones are computationally significantly less demanding and therefore dominate in parameter and state estimation applications.
The Thévenin model is a widely used equivalent circuit model of batteries. It is based on the Rint model, which uses an ideal voltage source v_{OC} for the terminal voltage and the internal resistance R_0 of the battery in series to describe the dynamic battery characteristics. The voltage and the internal resistance are thereby functions of the SoC and the temperature. In the Thévenin model, one or more networks consisting of a resistor and capacitor connected in parallel (RC-networks) are added to the Rint model. In contrast to the Rint model, the internal ohmic and diffusion polarization effects are also simulated and taken into account. Polarization effects affect the voltage changes at high and low SoC ranges. In the Thévenin model, R_0 is used to simulate the abrupt resistance characteristics, and the RC-networks consisting of $R_{1...\text{n}}$ and $C_{1...\text{n}}$ are used to simulate the characteristics of the gradual voltage changes.

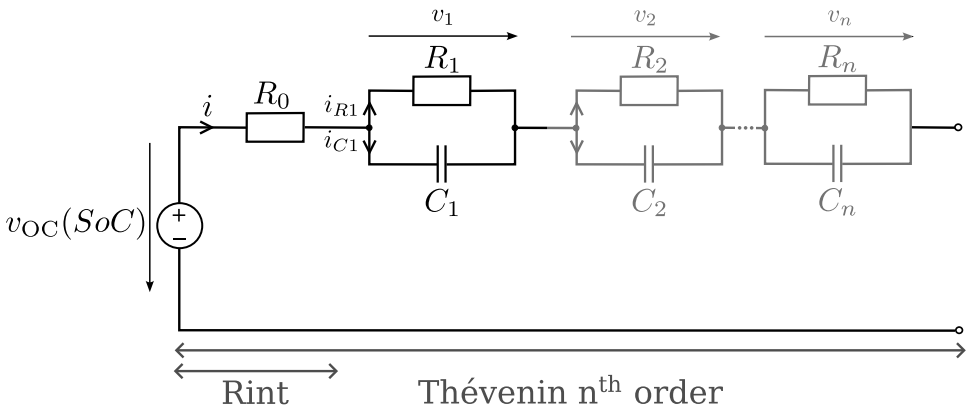


Figure 2.8: Thévenin equivalent circuit model of a battery [192, 193]

The Thévenin model consisting of one RC-network is referred to as a first-order model and takes into account both the ohmic polarization and the electrochemical one. Under the condition that the State of Health (SoH) and thus the internal resistance of the battery does not change significantly, the (dis)charge behaviour can be simulated accurately for a constant current and constant temperature. As the battery ages or the temperature changes considerably, the accuracy of the model significantly decreases. The second-order model adds a further RC-network in series and takes into account ohmic, electrochemical and concentration polarization. As the number of RC-networks increases, the accuracy improves but also the complexity and the computational effort increase.
For short-term predictions, it is usually considered sufficient to use a first-order

model, but for longer prediction horizons or low temperatures, the addition of a second RC-network to consider further polarisation effects can improve the accuracy. The following battery state parameters are not uniformed defined and specified explicitly. According to recent literature, definitions for the corresponding state values are described.

2.6.2 State of Power

The State of Power (SoP) provides information about the power capability of a battery by determining how much it can be (dis)charged within a given period of time. For the determination of the SoP, the variables to be tracked include the maximum (dis)charge current and the actual battery voltage v_{B} (Fig. 2.8), which depends on the SoC.
Since there is no general definition of SoP, a definition according to [194] is used within the scope of this thesis:
The behaviour of the battery is described by a first order Thévenin model consisting of one RC-network in series to the Rint model (Fig. 2.8). In the following, the SoP estimation for charging a battery is performed, where the maximum constant charging current $i_{\max}$ is determined, which results in the maximum allowed charging voltage $v_{\max}$ at the time $t+\Delta t$.
Applying Kirchhoff's second law, the loop rule, the following linear ordinary differential equation is obtained

$$\frac{d}{dt}v_1(t) = \frac{1}{C}\cdot\left(i(t) - \frac{v_1(t)}{R_1}\right) = \frac{1}{C}\cdot i(t) - \frac{1}{R_1\cdot C}\cdot v_1(t) \tag{2.4}$$

with the analytical solution:

$$v_1(t) = e^{\frac{t_0-t_1}{R_1\cdot C}}\cdot v_1(t_0) + \frac{1}{C}\int_{t_0}^{t_1} e^{\frac{\tau-t}{R_1\cdot C}}\cdot i(t)dt \tag{2.5}$$

With the condition, that a constant current I is used for the time period between t_1 and t_0 , the voltage at time t can be determined as follows:

$$v_1(t) = v_1(t_0)\cdot e^{-\frac{1}{R_1\cdot C}\cdot(t-t_0)} + R_1\cdot I\cdot\left(1 - e^{-\frac{1}{R_1\cdot C}\cdot(t-t_0)}\right) \tag{2.6}$$

Subsequently the voltage prediction at time $(t+\Delta t)$ results in:

$$v_1(t+\Delta t) = v_1(t)\cdot e^{-\frac{\Delta t}{R_1\cdot C}} + R_1\cdot I\cdot\left(1 - e^{-\frac{\Delta t}{R_1\cdot C}}\right) \tag{2.7}$$

Assuming that the voltage $v_{\mathrm{OC}}(SoC)$ does not change during the given time period, the following is obtained for the battery output voltage v_{B}:

$$v_{\mathrm{B}}(t) = v_{\mathrm{OC}} + R_0\cdot i(t) + v_1(t) \tag{2.8}$$

$$v_{\mathrm{B}}(t+\Delta t) = v_{\mathrm{OC}} + R_0 \cdot I + v_1(t+\Delta t) \tag{2.9}$$

The voltage margin is then:

$$\begin{aligned} \Delta v_{\mathrm{B}}(t) &= v_{\max} - v_{\mathrm{B}}(t) = \\ &= R_0 \cdot (i_{\max} - i(t)) + v_1(t) \cdot \left(e^{-\frac{\Delta t}{R_1 \cdot C}} - 1 \right) + R_1 \cdot i_{\max} \cdot \left(1 - e^{-\frac{\Delta t}{R_1 \cdot C}} \right) \\ &= \left(R_0 + R_1 - R_1 \cdot e^{-\frac{\Delta t}{R_1 \cdot C}} \right) \cdot i_{\max} - R_0 \cdot i(t) + v_1(t) \cdot \left(1 - e^{-\frac{\Delta t}{R_1 \cdot C}} \right) \end{aligned} \tag{2.10}$$

At each time instant, the maximum charge current $i_{\max}$ can be determined using the following equation, whereas the voltage v_1 can not be directly measured but is an estimated value ($\widehat{v_1}(t)$).

$$i_{\max} = \frac{\Delta v_{\mathrm{B}}(t) + R_0 \cdot i(t) + \widehat{v}_1(t) \cdot \left(1 - e^{-\frac{\Delta t}{R_1 \cdot C}} \right)}{R_0 + R_1 \cdot \left(1 - e^{-\frac{\Delta t}{R_1 \cdot C}} \right)} \tag{2.11}$$

With the maximum current the corresponding power can be obtained. The actual voltage shortly after starting the charge process with the current $i_{\max}$ is

$$v_{\mathrm{B}}(t+\Delta t) = v_{\mathrm{B}}(t) + R_0 \cdot (i_{\max} - i(t)) \tag{2.12}$$

For the instantly available power follows:

$$P_{\max}(t) = i_{\max} \cdot (v_{\mathrm{B}}(t) + R_0 \cdot (i_{\max} - i(t))) \tag{2.13}$$

2.6.3 State of Charge

The SoC describes the ratio between the remaining capacity and the actual capacity (C_{act}) in percent:

$$SoC = \frac{C_{\mathrm{rem}}}{C_{\mathrm{act}}} \tag{2.14}$$

It describes how much (dis)charge capacity remains in the battery.
The SoC describes the remaining (dis)charge capacity and is used together with the actual capacity as a performance indicator to determine how much energy can be supplied or absorbed by a battery.
It serves as the basis for preventing over(dis)charge and also provides the data for other battery state indicators, such as the State of Function (SoF) and State of Safety (SoS).
The SoC cannot be measured directly [195]. Several methods for SoC estimation have been introduced, but a precise definition is still pending, as it requires further analytical work, such as predicting the remaining useful life and estimating the

capacity. One common method for SoC estimation is the current integration, which expresses the ratio between the present maximum available capacity (C_{rem}) and the actual capacity (C_{act}):

$$SoC(t) = SoC(t_0) + \int_{t_0}^{t} \frac{i(t) \cdot \eta_{\text{C}}}{C_{\text{act}}} dt \tag{2.15}$$

where t is time, $SoC(t_0)$ is the initial SoC value, $i(t)$ is the battery (dis)charge current and η_{C} is the Coulomb efficiency. The Coulomb efficiency is defined as the ratio of the discharge energy compared to the required charge energy to regain the initial remaining capacity value:

$$\eta_{\text{C}} = \frac{E_{\text{discharge}}}{E_{\text{charge}}} \tag{2.16}$$

An overview of different SoC determination methods and their (dis)advantages is given in [196].

2.6.4 State of Energy

The open-collector voltage (v_{oc}) of most battery types is not constant over the entire SoC range, but increases at high SoC values and decreases at low charge levels. Consequently, the same charge rate at different SoC values results in varying quantities of supplied/absorbed energy, especially as the two end ranges are approached. Furthermore, the temperature, the load cycling and the discharge rates affect the useable energy. For example, high discharge rates result in significant internal energy losses compared to negligible capacity losses [197]. This is not observable only considering the SoC value, which provides information about the remaining capacity. The State of Energy (SoE) is defined as the ratio between the remaining energy usable under certain operating conditions and the total available energy of the battery. The definition of the SoE is given by

$$SoE(t) = SoE(t_0) - \frac{\int_{t_0}^{t} p(t) dt}{E_{\text{act}}} = SoE(t_0) - \frac{\int_{t_0}^{t} i(t) \cdot v_{\text{B}}(t) dt}{E_{\text{act}}} \tag{2.17}$$

where t is time, $SoE(t_0)$ is the initial SoE value, $p(t)$, $i(t)$ and $v(t)$ denote the power, current and voltage respectively at the time t and E_{act} is the total available energy of the battery. The SoE is taken into account, for example, for estimating the remaining driving range in electric vehicles [197].

2.6.5 State of Function

In order to avoid hazardous battery operating conditions, batteries have to be operated within the safe operating area (Fig. 2.7 on p. 22). Restrictions such as maintaining the minimum/maximum limits of the voltage, the (dis)charge current, the operating temperature and the SoC constrain the maximum usable power. The indicator State of Function (SoF) is used to predict the maximum usable power considering the safe operating area. According to the definitions [198, 199], the SoF is determined as follows

$$SoF(t) = \frac{P_{\mathrm{B}}(t) - P_{\mathrm{d}}(t)}{P_{\max} - P_{\mathrm{d}}(t)} \tag{2.18}$$

where $P_{\mathrm{B}}(t)$ is the power provided by the battery and $P_{\mathrm{d}}(t)$ the power demand at time t, respectively. $P_{\max}$ is the maximum power that a non-degraded, fully charged battery can deliver to a load under ideal operating conditions.
The battery power depends, among other things, on the SoC and the SoH:

$$P_{\mathrm{B}}(t) = P_{\max} \cdot SoC(t) \cdot SoH(t) \tag{2.19}$$

Additional limiting factors such as temperature or maximum permissible charging current according to the SOA can further limit the usable battery power.

2.6.6 State of Safety

The State of Safety (SoS) according to the definition in [198] indicates the probability that the battery is in a safe operating state. For the determination of the SoS, various potentially safety-endangering parameters such as temperature, current, voltage, State of Charge, State of Health and internal resistance as well as mechanical stress are taken into account.
Hazard functions describe the probability of a hazard arising from the corresponding parameter, with the value 1 describing a completely safe state and 0 an unsafe state.

$$SoS(x) = f_1(x_1) \cdot f_2(x_2) \cdot \ldots \cdot f_n(x_n) \tag{2.20}$$

The functions f_1 to f_n indicate the individual failure probabilities for potential failures. The definition of these failure probabilities is a subject of functional safety and will not be further discussed within the scope of this thesis.
With the additional condition that each sub-function has a lower value ζ to ensure safe behaviour, the most relevant SoS values are given below:

$$SoS \begin{cases} = 1.0, & \rightarrow \text{completely safe, all subfunctions are 1.0} \\ = \zeta, & \rightarrow \text{warning, one function is at } \zeta \\ = \zeta^n, & \text{where } n \text{ is the number of subfunctions} \rightarrow \text{warning, all subfunctions are } \zeta, \\ < \zeta^n, & \text{where } n \text{ is the number of subfunctions} \rightarrow \text{unsafe} \end{cases} \tag{2.21}$$

2.6.7 State of Temperature

Batteries are sensitive to high and low temperatures. If batteries are operated outside the specified temperature range, the decrease in battery capacity and the increase in resistance are accelerated. In addition, thermal runaway of the battery can occur due to mechanical, electrical or thermal stresses. Therefore, it is necessary to consider heat generation and dissipation in batteries:

$$\frac{d}{dt} Q_{\mathrm{accu}} = \rho \cdot C_{\mathrm{P}} \cdot \frac{dT}{dt} = \frac{d}{dt} Q_{\mathrm{gen}} - \frac{d}{dt} Q_{\mathrm{dis}} \tag{2.22}$$

where ρ is the battery (cell) density, C_P is the heat capacity,T is the battery (cell) temperature, and t is the time. Q_{accu} is the accumulated heat and is derived from the generated heat Q_{gen}, which includes both reversible and irreversible heat resulting from chemical reactions, and the dissipated heat Q_{dis}, which takes into account heat transfer mechanisms such as conduction, convection and radiation.
In addition to temperature measurements on the surface of the battery cells, the consideration of the interaction with neighboring battery cells using thermal equivalent circuit models [200] and the internal cell temperature [201] is also relevant for the assessment of temperature.

2.6.8 State of Health

The usable capacity is not constant over the lifetime of a battery. At the Begin of Life (BoL) of a battery, the actual capacity (C_{act}) is equal to the nominal one (C_N). Over time, the actual capacity is reduced due to age-related capacity loss. The Remaining Useful Life (RUL) describes the service life until the battery reaches its End of Life (EoL). The EoL for vehicle batteries, e.g., is reached when the actual capacity is less than 80% of the nominal capacity (C_N) (Fig. 2.9).

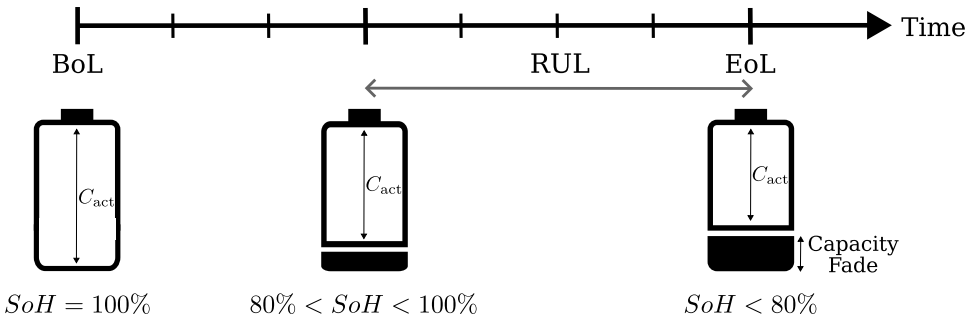


Figure 2.9: Capacity fade over the lifetime of a battery.

Various aging mechanisms cause capacity degradation over time (Fig. 2.11).
Aging is divided into two types: the calendaric one is the aging that always takes place. It occurs even when the battery is not connected, i.e. not in operation, for example during battery storage. Increased calendaric aging occurs especially due to adverse SoC and high temperatures [203]. Consequently, cyclic aging describes the one occurring due to operation. It occurs at an accelerated rate, e.g., at high load currents and at SoC and temperature values above or below the permissible operating range [204] (Fig. 2.11).
The SoH describes the ratio of the actual capacity (C_{act}) to the nominal capacity (C_N) in percent

$$SoH = \frac{C_{act}}{C_N} \tag{2.23}$$

where C_{act} is the maximum available (dis)charge capacity under consideration of age related capacity loss and C_N is the nominal capacity. The state determinations, the measurements required for these, and the data management of the measured values are tasks of the battery management system.

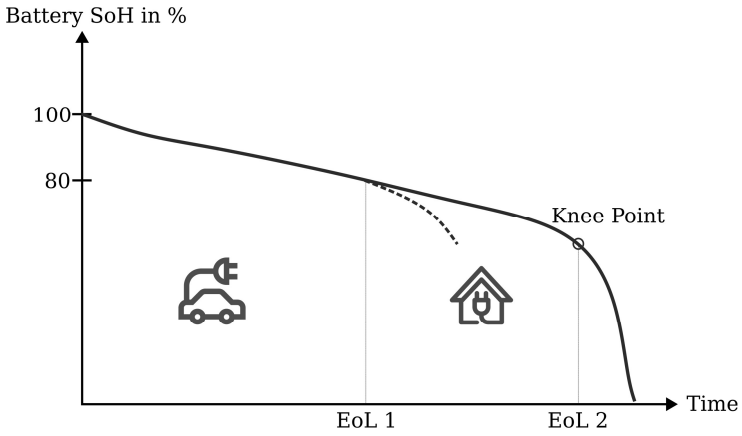


Figure 2.10: Shifting the knee point: When the batteries reach a SoH of 80%, they are no longer used in electric vehicles, as these have increased requirements in terms of capacity and, above all, dynamics. High discharge currents, such as those caused by acceleration when starting uphill, put a strain on the batteries. If they were still used in the vehicle, they would soon reach the EoL (dashed line). Using the batteries in applications with lower demands and strains allows the knee point to be shifted to the left and the actual EoL to be delayed. The knee point describes the point at which capacity fade occurs at an increased rate. Up to the knee point, the capacity fade is approximately linear, followed by an increased degradation rate after exceeding this point [202].

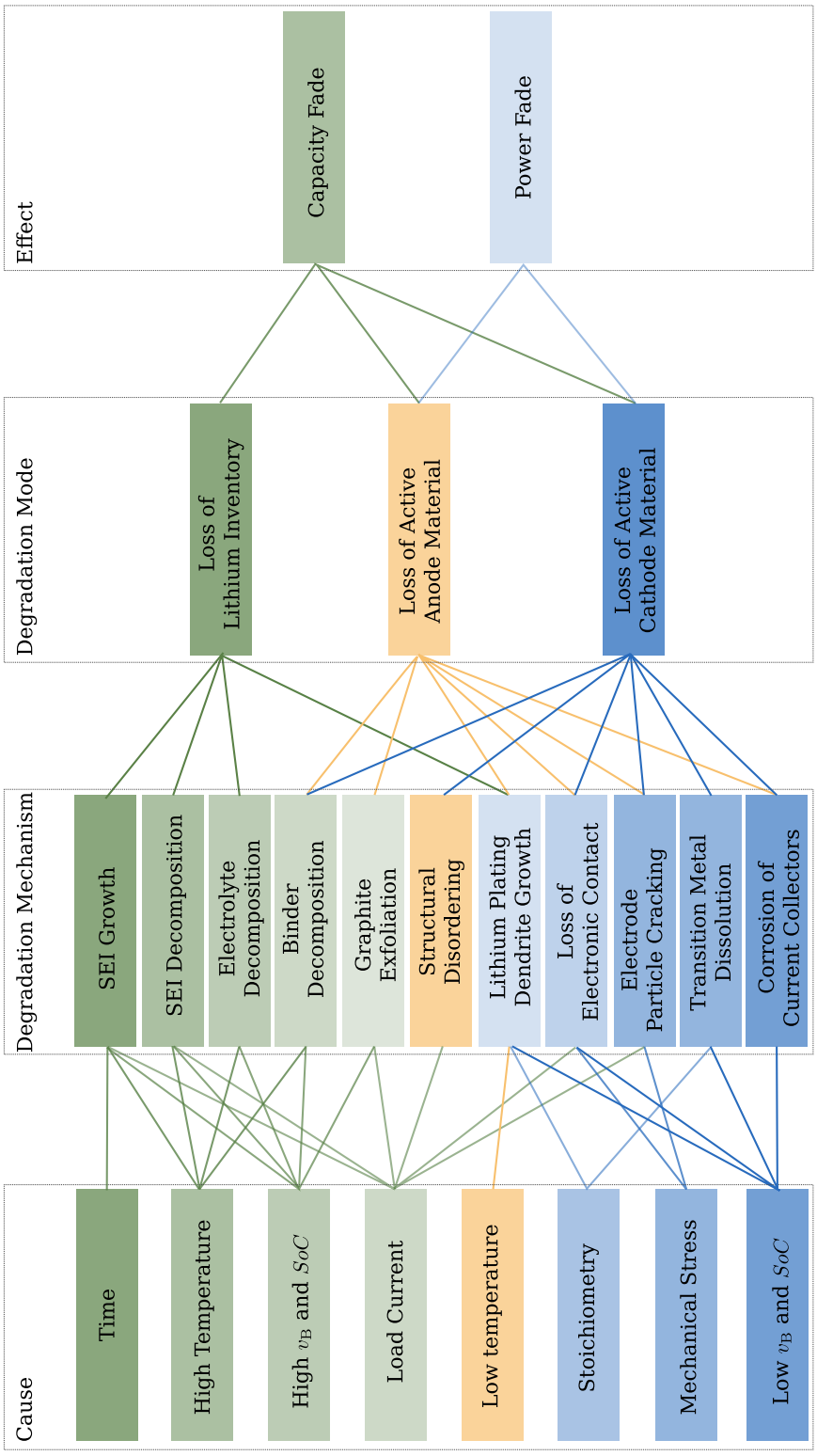


Figure 2.11: Interdependencies and interaction of lithium-ion battery cell degradation mechanisms including their causes and effects. [190].

3

General System Description and Requirements Analysis

Battery management systems are required for safe and reliable battery operation. In this chapter, at first existing battery management systems including their architecture, control algorithms and communication protocols are presented and evaluated in terms of reliability, scalability and flexibility. The decentralization of battery management systems and the associated benefits are highlighted. Limitations of existing approaches are discussed and a decentralized, scalable, reconfigurable battery management system based on a distributed architecture of self-organized, locally controlled nodes is proposed. The features, benefits, and challenges of the proposed approach are described. Furthermore, the requirements for the components of the distributed BMS resulting from the architecture are analyzed.

3.1 Motivation

With an increasing share of renewable energy sources and electric vehicles, batteries are one of the most utilized energy storage media [205]. Battery use is essential for maintaining the energy balance and for improving the quality as well as the reliability of power supply in renewable energy systems [206]. A critical challenge facing the widespread adoption of battery technology is to ensure uninterrupted, fail-safe power supply with increased reliability and, simultaneously, safe, optimal battery operation to extend battery life.
Battery Management Systems (BMS) are used for these purposes and provide the interfaces between energy producers, consumers and batteries (Fig. 3.1).
They administer system control and management with regard to energy storage and transmission. Main functions of the BMS include charge and discharge control, battery charge monitoring and equalization, input/output current and voltage monitoring, temperature control, battery protection, fault diagnosis and evaluation. [207]
For this purpose, the following functional requirements are relevant for a BMS:

- Current, voltage and temperature measurement,
- State of Charge (SoC) and State of Health (SoH) determination,

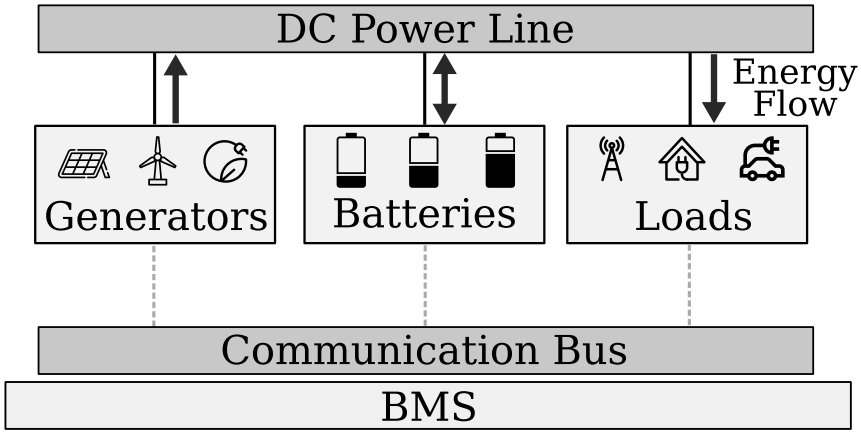


Figure 3.1: Principle architecture of a battery management system indicating participants, communication and power flow. The participants consist of a variable number of heterogeneous batteries, variable loads and renewable energy generators.

- communication,
- robustness against electromagnetic interference (EMI),
- redundancy of the system in terms of functional safety,
- electrical isolation of the functional systems and
- balancing [208, 209].

Besides the BMS unit, which includes data acquisition, state monitoring and control, the topology of the BMS is crucial for large-scale battery management. The topology covers the electrical connection of the individual batteries or battery cells, the control structure and the communication architecture. It directly influences costs, ease of installation, maintenance, measurement accuracy and above all the reliability of the system.

This chapter first describes existing BMS topologies together with relevant literature and outlines their benefits and limitations. The proposed classification divides the BMS topologies into

- centralized,
- modularized,
- distributed and
- decentralized.

The identified trend towards the decentralization of battery management systems is shown subsequently: Centralized battery management systems with a single control unit [210–212] are increasingly replaced by a decentralized management systems, whereby sensor, control and computing resources are distributed [213–217]. The characteristics of the control strategies are therefore analyzed and compared.

An approach for a fully decentralized, distributed battery management system based on autonomous, locally operating units is proposed. The characteristics and advantages of the proposed approach are described. The requirements, particularly in terms of system control and management, are analyzed and challenges to be overcome are identified. The aim is to provide a holistic overview of the features of the proposed battery management system and the resulting system requirements.

3.2 Related Work: Battery Management System Topologies

In the following, existing work on battery management systems is reviewed and categorized according to their BMS architecture. Characteristics, advantages and disadvantages of the architectures are described.

3.2.1 Centralized

Centralized battery management systems are characterized by integrating all functionality into a single, central module. The batteries or cells are connected to the central control unit via several lines (Fig. 3.2) [218]. The central BMS allows measurement of single cell voltage, string current, and temperature. In [219], a central battery management system based on a single chip is described. The protection function is divided into two stages. The first stage monitors voltage, current and temperature and coordinates the active or passive balancing function. The second stage is used for handling severe, safety-critical faults.
Another approach for a centralized BMS is presented in [220]. The central control unit provides monitoring, balancing and state determination via a gaugemeter for twelve to fifteen Li-ion cells.

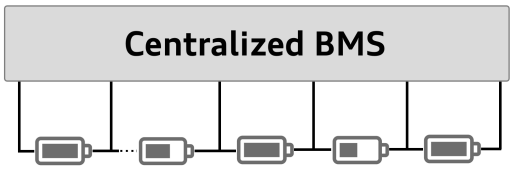


Figure 3.2: Simplified block diagram of a battery management system based on centralized topology, which records the operating data of the individual cells, monitors them and coordinates the system control.

Conventional BMS are often centrally organized, with a master controller, the central control unit, recording and controlling all battery characteristics and activities. In most cases, only one microcontroller is used. The advantages of a centralized BMS include low cost and ease of maintenance and repair. Using only a single integrated circuit reduces costs and facilitates detection of faults. Another advantage is accuracy, since centralized BMSs use the same offsets for all cells. Furthermore, the clearly defined coordination structure enables effective system control.
Disadvantages include the many, relatively long cable connections, which significantly increase the risk of short circuits. In addition, inputs can be easily confused and incorrectly connected, and connections can become loose, increasing the susceptibility to errors. Another disadvantage is the lack of scalability and flexibility of the system architecture. In centralized master-slave battery management systems, the maximum number of batteries is strictly defined. During system development, the number of actively used batteries is determined and can usually only be changed afterwards by changing the wiring. Adding additional cells is not possible at all if all input connections are occupied. Furthermore, only predefined, mostly single battery technologies are supported, combinations of them are not possible.
In addition, the master controller is a single point of failure. The entire system control depends on the error-free operation of the master controller. In the event of a failure or malfunction of the master controller, the entire system operation is at risk. This is

a significant disadvantage, especially with regard to a reliable, uninterruptible power supply.

3.2.2 Modularized

Modularized battery management systems are characterized by several identical modules, which are connected to the individual batteries or battery cells via cables, similar to centralized BMS (Fig. 3.3). The BMS modules provide data acquisition (single cell voltage, current, temperature) and communication interfaces to the other BMS modules. Often one of the modules is assigned to the role of master or a separate module serves as master.
The master module controls the entire battery pack and communicates with the rest of the system, while the other modules merely record the measured data and transmit it to the master.
A modularized battery management system is proposed in [207] with the aim of improving the performance of BMS to provide a safe, reliable and cost-efficient solution for smart grids and electric vehicles.
The modularized battery management system for electric vehicles presented in [221] focuses on effective single cell monitoring and balancing for a large number of battery cells with comparatively small size and complexity.

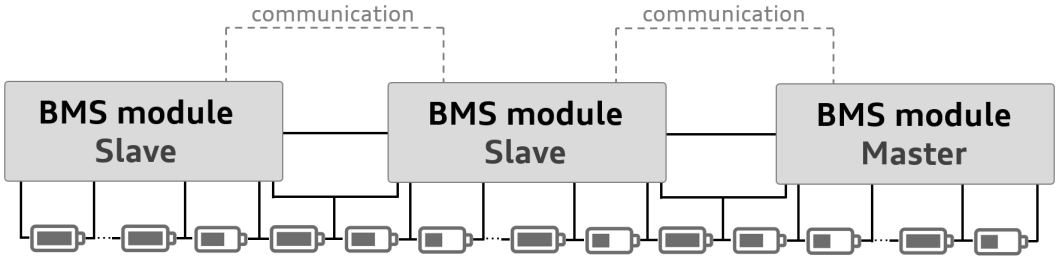


Figure 3.3: Block diagram of a battery management system based on a modular topology.

An advantage of modularized battery management systems is the improved manageability. The modules are placed close to the batteries, which avoids long cables. To improve functional safety, the function of the BMS can be easily replicated on the individual modules. The scalability is also increased compared to centralized battery management systems. If the battery pack is extended by further cells, another BMS module is simply appended.

The number of inputs of the BMS modules is still fixed and under certain circumstances, inputs may remain unused. In addition, the costs of modularized battery management systems are higher. Compared to centralized BMS, the failure of one BMS module does not endanger the entire battery operation. Defective battery cells or batteries are simply removed from the system, reducing capacity but maintaining operation.

3.2.3 Distributed

In distributed battery management systems, each cell string or cell is equipped with its own BMS module. The cell BMS modules provide measurement of operating parameters, balancing and communication. The BMS controller handles the calculation and communication (Fig. 3.4).

A distributed battery management system divided into a master and several battery modules for real-time monitoring and reporting of battery operating conditions is proposed in [222]. This approach combines central control management and distributed data collection.
In order to reduce costs and time-to-market and to increase flexibility, scalability and adaptability, [223] proposes a distributed battery management system with smart battery cell monitoring. The smart battery cell monitoring consists of electronics for monitoring and a data transmission interface for bidirectional communication with the superordinate battery management system. The battery management system functions as the master and controls energy storage at system level. The distributed

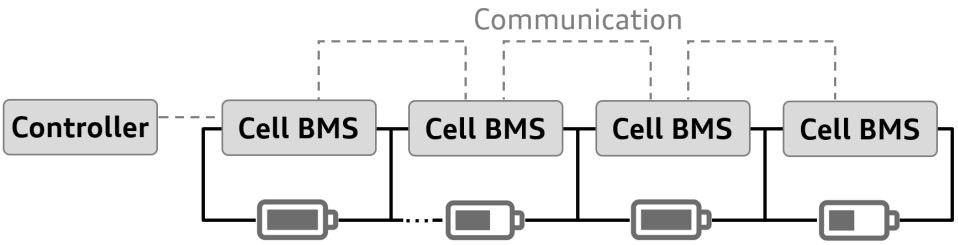


Figure 3.4: Block diagram of a battery management system based on a distributed topology

battery management system simultaneously offers a high level of reliability and robustness as well as a cost-efficient development process, allowing a significant reduction in the cost of the final battery pack.
The advantages of distributed battery management systems compared to centralized and modularized topologies are scalability and flexibility. No maximum number of inputs is defined and cells can be added or removed even after installation. This allows easy hardware integration for homogeneous modules. Scaling the battery pack to the size required for different applications does not result in any changes to the hardware or software of the modules – only additional battery cell modules have to be assembled or removed.
Furthermore, the single point of failure of centralized approaches is avoided. Local control of each cell additionally increases safety. Sensor information only needs to be processed for the local cell and mandatory actions can be triggered immediately. A further advantage is the high measurement accuracy, which is achieved by the specialization of the battery cell module. Furthermore, shorter connecting wires enable more accurate voltage measurement and better interference immunity. Maintenance or replacement of defective parts is facilitated by the modular, distributed architecture.
Disadvantageous are the increased costs for the battery management system, as a separate BMS module is required for each cell and for most applications also an additional master module.

3.2.4 Decentralized

The decentralization of battery management systems is a possible solution to overcome the disadvantages of central control structures. Decentralized battery management systems consist of several equal units, which provide the entire functionality locally and autonomously. Each of the individual BMS units is able to operate independently of the remaining ones. Communication lines between the

units enable information exchange and task coordination between the units. They are used in several decentralized BMS (Fig. 3.5). While this architecture offers advantages like scalability, minimal integration effort and increased functional safety, the development requires new methods. Decentralized battery management systems are further subdivided into communication-less, wireless and wired communication based topologies.
In [224] a decentralized battery management system without communication requirements is proposed. The smart cells work locally and autonomously, which increases safety and reliability.
A decentralized battery management system based on droop control for a series connection of battery cells is proposed in [225].
Droop control is applied to components connected in parallel to ensure power sharing among them. Droop characteristics are used for power distribution, which correspond to V-I characteristics in voltage droop control. They determine the required output/input current according to the actual voltage deviation. Physically the droop control behaves like an output resistance. Therefore the droop characteristic is also called virtual resistance. [226, 227]
Droop control offers high reliability due to the decentralized architecture and the communication-less control. A drawback of the droop-based control is the imprecise control [228]. With the consideration of line resistance in a droop-controlled system, the output voltage of each converter cannot be exactly the same. Therefore, the output current sharing accuracy is affected. In addition, the voltage deviation increases with the load due to the droop characteristic. [229]
Due to the possibility of cable breaks in wired communication systems like CAN or I^2C, BMS approaches based on wireless communication are developed [230]. As a possible solution, [230] proposes a distributed and decentralized wireless battery management system based on an Internet of Things (IoT) network.
In [231], a fully decentralized battery management system is proposed, whereby the entire BMS functionality is integrated into the cell management units. One cell management unit per cell is used, providing local sensing and management capabilities autonomously and system-level functionality by coordination via communication. A CAN bus is used for wired communication, which enables broadcast communication between the cells.
The major advantage of decentralized battery management systems is the absence

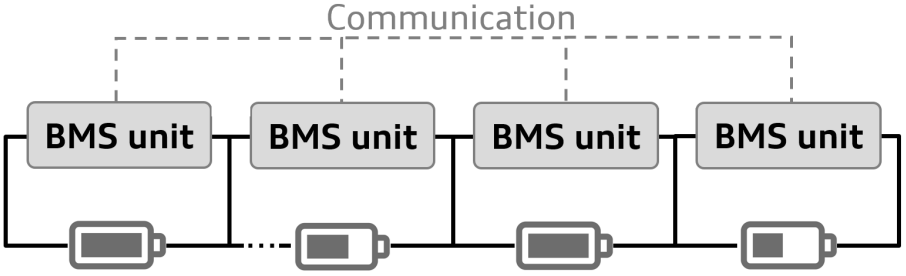


Figure 3.5: Block diagram of a decentralized battery management system

of a central control unit, on which error-free function the entire operation depends. Furthermore, the scalability and flexibility are advantageous. The number of inputs is not fixed and can be extended/reduced even after installation.
A challenging feature is the distributed system control based on the equal, parallel-operating and autonomous nodes. In addition, it has to be ensured that the single

point of failure is not only shifted but eliminated. For a reliable system, a holistic approach is required.
Table 3.1 summarizes the evaluation of existing battery management system topologies in terms of reliability, scalability and flexibility. Compliance with the criteria is evaluated, where ++ means full compliance, + partial compliance, 0 neutral, – partially not satisfied, and – – not satisfied at all.

Table 3.1: Evaluation of existing battery management system topologies in terms of reliability, scalability and flexibility.

BMS Topology	Reliability	Scalability	Flexibility
Centralized	– –	– –	– –
Modularized	0	–	–
Distributed	+	+	+
Decentralized	++	++	++

3.3 Decentralized Battery Management System Based on Self-Organizing Nodes

The proposed decentralized, heterogeneous battery system consists of renewable energy sources, variable loads and of batteries with differences in cell chemistry, rated capacity, SoC and SoH. All components are connected together with a common power line and at least one global communication bus (Fig. 3.6).

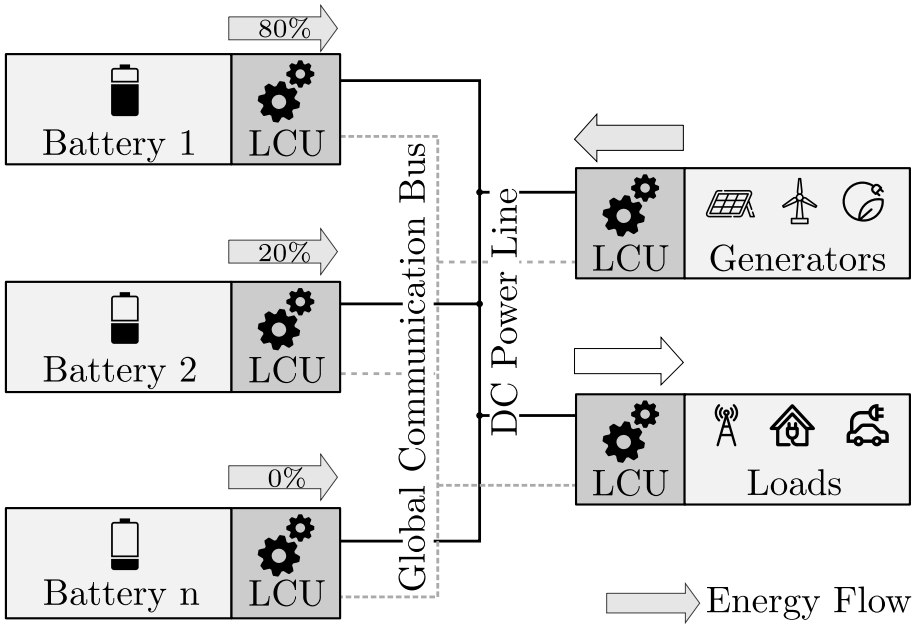


Figure 3.6: Overview of the decentralized battery management system with battery state-aware load distribution: The local control units are the basis for distributed control and battery state-dependent load sharing.

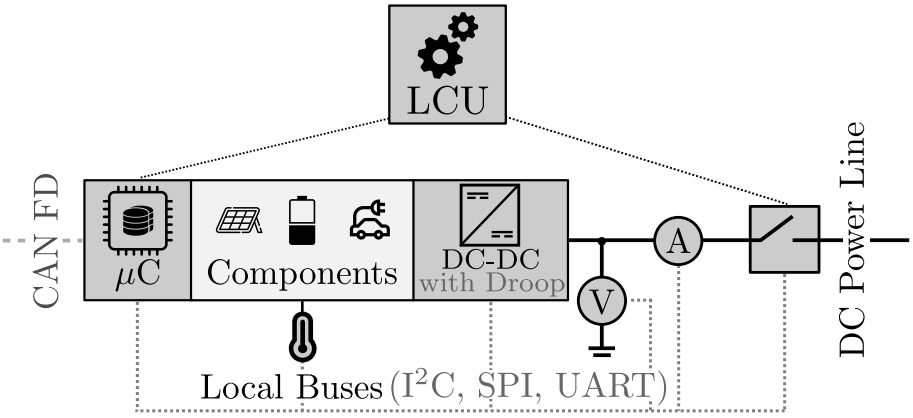


Figure 3.7: The Local Control Units (LCUs) consist of microcontrollers, current, voltage and temperature sensors and relays. The operating parameters are recorded and managed by the LCUs. This allows to apply predictive energy management strategies and helps to estimate the residual value of the batteries.

3.3.1 Distributed Control

For distributed, autonomous control, each of these components is equipped with its own Local Control Unit (LCU) (Fig. 3.7). The LCU consists of

- current, voltage and temperature measurement to record actual operating parameters,
- various communication interfaces for data exchange between the system components
- a microcontroller for calculation, data management and evaluation,
- a DC/DC or AC/DC converter, and
- a relay which is opened in case of failures, to avoid safety critical voltage levels or for maintenance purposes.

For system-wide data consistency, each microcontroller manages all operating data required for the control and sends them via the global communication bus to all the remaining participants. Consequently, each microcontroller manages all the data required for system control. The loads and generators also have LCUs and send their operating parameters to all components as well. They use the LCU to provide their operating parameters for load/generation forecasts and for voltage control.
Batteries provide the ability to absorb excess power or deliver missing power and thus are able to control the system. Therefore, additional algorithms for system control and leader election are implemented on the LCUs of the batteries.
The implemented software for system control manages both the actual operating data such as current, voltage and temperature and the system states resulting from previous measurements.
Based on the data, the LCU determines the SoC and the SoH. In addition, the battery fitness is defined. The battery fitness is an own numerical value based primarily on state of charge, state of health, number of charge cycles, time of last charge/discharge, the system-wide normalized capacity and the actual operating parameters. Taking into account the optimum operating range of the respective battery technology, the battery condition is evaluated. The criteria, e.g. SoC or temperature, are weighted. The criteria weighting can be adjusted depending on the battery technology and

the system state. The adjustment of the weighting provides the basis for system optimization according to various criteria such as cost minimization, maximum safety or availability. A unique feature of the proposed technique of the thesis is the control based on the battery fitness.
The battery fitness enables a system-wide definite evaluation of different battery technologies. In turn, this enables the combination of different battery technologies in a single system. The combination of different battery technologies offers advantages including optimization of the system control, extending battery life and increasing system reliability [232]. Additionally, it offers a second life application to a wide range of used batteries [233, 234].
The battery fitness also influences the decision criterion for the leader election. The participating nodes work autonomously and locally and control the system in a collaborative manner. In contrast, the challenging task in the context of the proposed approach is to structure, adequately equip and network the nodes to such an extent that the overall system and its control interact harmoniously. The LCUs are interacting in the physical domain in their control task while communication latency for negotiations is high compared to the control requirements. In addition, in reality the nodes do not work perfectly synchronized but asynchronously [235]. Therefore, the development of a system control consisting of decentralized, autonomous, distributed, asynchronous nodes is a non-trivial, challenging task.
The target of the decentralized control structure is to make the system independent of the error-free function of single components. This can be achieved if the role of the central control unit is not permanently assigned to a single component. Therefore, instead of the decentralized system control being distributed to all nodes, the approach of the system control coordinated by a temporary master which gets reassigned on a regular basis was chosen. One LCU of the batteries is chosen as the temporary central control unit applying a leader election algorithm. The temporary central control unit determines the required (dis)charge power of the remaining battery nodes, taking into account their battery fitness. In case of failure, malfunction or changes in control capability, one of the battery nodes is selected as the new central control unit. As a result, potential single point of failures of existing centralized approaches is reduced. This results in specific requirements for the control of the system. The main control objective is to maintain the DC link voltage at the predefined setpoint with variable loads and generators while safely operating a heterogeneous battery system. This requires load sharing between the batteries connected in parallel and individual limitation of the (dis)charging currents of the separate batteries taking into account their specific SOA.
Additional requirements arise to ensure reliability and high system availability: The control stability should not be endangered even in case of measurement deviations, asynchronous clocks of the microcontrollers, message delays, failure of individual nodes and failure of the communication.

3.3.2 Communication

Communication between the peer nodes is the basis for system-wide data consistency and for the independent, local control of the decentralized battery management system. For autonomous decision making and system control, the nodes communicate their operating parameters and collaborate based on a system-wide uniform database. To enable fast and energy-efficient communication between nodes, a suitable communication technology is required. In addition, a robust communication

architecture is needed, that can withstand the harsh environmental conditions, e.g., in the automotive sector, and the high availability requirements, such as in uninterruptible power supply systems. Therefore, the establishment of a safe communication protocol between the individual nodes is essential for the reliable operation of the BMS.
In summary, a proven, robust, noise-free, fast, and reliable communication technology is required. To achieve minimal integration overhead and effective reconfigurability, an architecture with minimal wiring harness is required for the distributed topology. Since system-wide data consistency is mandatory, the communication technology needs to be broadcast-capable. The measurements of the individual nodes contain only a few bytes of useful data, but form part of the system-wide feedback loop of the control system. Therefore, high transmission rates, low message overhead with few user data bytes and low latencies are essential. Besides the feedback values, the messages also contain the control specifications. Therefore, reliable communication with a low error rate is required. Error detection mechanisms are helpful to react to corresponding errors.
The requirements for the communication in the DBMS can be summarized as follows:

- Broadcast capability,
- low message overhead for a small number of user data bytes,
- low latencies and high transfer rates,
- robustness and reliability and
- low error rates, error detection and error handling.

Chapter 4 presents a comparative analysis between CAN, CAN FD, and Ethernet communication technologies and justifies the choice of communication technology for the DBMS. In addition to the presented analysis, dual CAN communication [236] and CAN in combination with optical data transmission via Polymer Optical Fiber (POF) were also investigated.

3.3.3 Safe Operation of a Heterogeneous Battery System and Battery State Aware Load Distribution

Various batteries have different terminal voltages and SOAs. In order to be able to use them safely in combination in a system and to take advantage of their inherent properties, such as tolerance to high peak currents, low-temperature capability, high power or energy density, special requirements arise for the necessary measurements, condition determinations and, above all, for the power electronics and the control strategies.
Accurate current, voltage and temperature measurements as well as determination of the SoC are the basis for compliance with the SOA of the batteries and, possibly, even the Optimized Operating Area (OOA). DC/DC converters are required to convert the divergent terminal voltages to a common DC line voltage value. Bidirectional DC/DC converters are particularly suitable for realizing the power flow in the (dis)charging direction. To meet the demand for flexibility, a wide voltage range is required on the low voltage side connected to the battery and an adjustable voltage value on the high voltage side connected to the common DC link.
For safe, battery-degradation-aware operation, the total current is divided between the batteries to be used safely and connected in parallel. The sharing factor is determined depending on the battery condition. For the realization, a current limitation of the

DC/DC converter used that can be adjusted in active operation is required, as well as corresponding control strategies.
The requirements for the DC/DC converter can be summarized as:

- Wide voltage range at the low voltage side to support a large variety of batteries,
- Adjustable voltage level at the high voltage side to enable the use in as many different applications as possible and
- (Dis)charge current limit adjustable during active operation by the microcontroller for i, safe or ii, optimized operation of the heterogeneous battery system.

3.3.4 Scalability and Integration

The number of inputs and thus of participants is not fixed in the proposed decentralized battery management system. A minimum of two batteries is recommended for a reliable supply. Adding and removing nodes is possible even after installation and during operation. Both hardware and software are required to be designed for effective integration and reconfiguration [237]. The variable number of participants, which can be adjusted and changed during operation, allows the system to be adapted to requirements changing over its lifetime, e.g., in- or decreased required energy storage capacity depending on the power of the load or generation. Optimizations in terms of e.g., cost efficiency, total storage capacity, safety or maximum service life can be implemented or changed. The reconfigurable architecture increases reliability, performance and flexibility of the proposed BMS [238]. The requirement for scalability and expandability influences both the design of the software and the selection of hardware components, especially the communication technology as well as the connections. It also affects the control strategy, which must be able to achieve the control objective even if components are added or removed during active operation.

3.3.5 Flexibility

The variable number of participants and the possibility to use and combine different battery technologies increases the flexibility of the system. Existing approaches tend to specialize in a single battery technology [239, 240]. In order to improve the performance and energy density, new battery technologies are constantly being developed [241–243]. The battery management system is flexible and effective in adapting to changing conditions for optimal and safe battery operation. The software is effectively expandable and software updates during operation support the effective integration and potentially necessary software adjustments supporting new battery technologies [244]. Flexibility also influences the overall system design, especially the choice of DC-DC converters used and their supported voltage ranges.

3.3.6 Fields of Application

The flexible, scalable, reconfigurable architecture opens up various fields of application including uninterruptible power supply, electric vehicles, (islanded) dc microgrids, grid support for peak load shaving or load management. The applications result in different requirements for the BMS. For electric vehicles, for instance, high availability, safety and energy density with minimum size and weight are required. For islanded microgrids, the relevant criteria include effective service lifetime, cost efficiency, reliability and resistance to environmental effects.

3.4 Summary

In this chapter, existing battery management system topologies were presented and discussed in terms of scalability, flexibility and reliability. The distributed battery management system based on self-organized and locally operating nodes and its distributed system control were described. Resulting requirements for the design of the software and the hardware were analyzed and possible fields of application for the DBMS were discussed.

4 Communication Requirements and Comparative Analysis

The proposed decentralized battery management system is a networked control system consisting of sensors, actuators and controllers with a communication network in the control loop. The data rate and the reliability of the underlying communication network are key factors since delays or message losses directly affect the system control. In addition, the processor load caused by the communication is significant as it influences the calculation of system states and the setting of control parameters. The power consumption of the communication network has a further impact on the overall energy efficiency of the respective application. In this chapter, the communication technologies Controller Area Network (CAN), Controller Area Network Flexible Data-rate (CAN FD) and Ethernet are compared in the context of networked control systems with focus on a decentralized battery management system. First, the message processing time and the processor load are measured. The maximum power consumption is determined with regard to energy efficiency, which is significant as the communication is used for an energy management system. The Bit Error Rates (BER) and the Residual Error Rates (RER) are calculated to evaluate the reliability. Finally, the receive FIFO load under high traffic conditions is examined.

4.1 Motivation

Within a networked control system the tasks are distributed among several nodes. Communication between the participants is required in order to achieve the common control objective. Networked control systems offer several advantages including reconfigurability. Nodes can be added or removed even after an initial installation. This increases flexibility and enables a variety of different applications. Furthermore, networked control systems allow decentralization of the control system (Chapter 3). Instead of a fixed coordination unit setting the control parameters, communication-based coordination of the control tasks is possible. This increases the reliability and

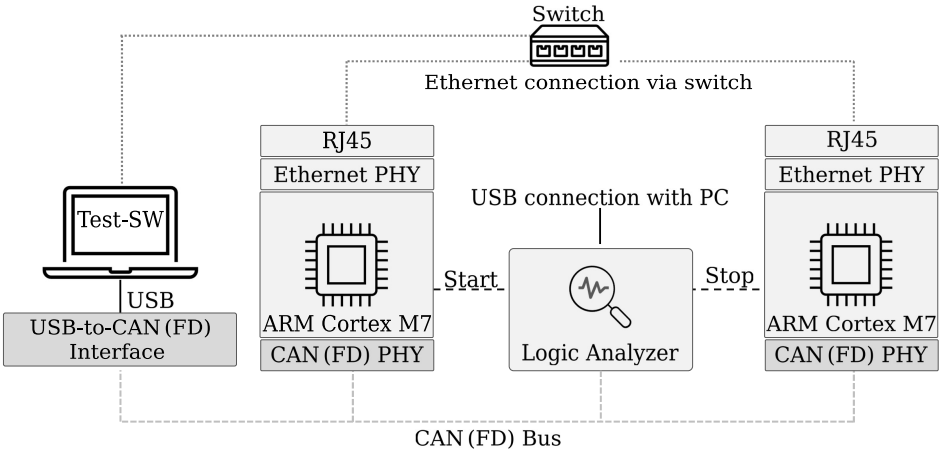


Figure 4.1: Test setup for the comparative analysis of CAN, CAN FD and Ethernet communication.

availability of the system compared to centrally structured systems whose operation depends on the error-free function of the coordinating master unit. Furthermore, communication-based control enables system-state-dependent set points.
Despite the various advantages, there are several challenges to overcome in networked control systems. The communication network causes unpredictable delays which can affect the system control. For CAN communication, e.g., only the latency of the highest prioritized message can be determined. For the remaining messages, the delay depends on the situation on the bus and is not predictable. These network-induced delays may increase the time jitter of the control loop, which consequently can lead to instability. In addition, possible data or information loss or data manipulation, endanger the control coordination. Therefore the data rate and the reliability of the underlying communication network are key factors of the networked control system. In addition, the processor load caused by the communication is relevant as it affects the calculation of system states and the setting of control parameters.

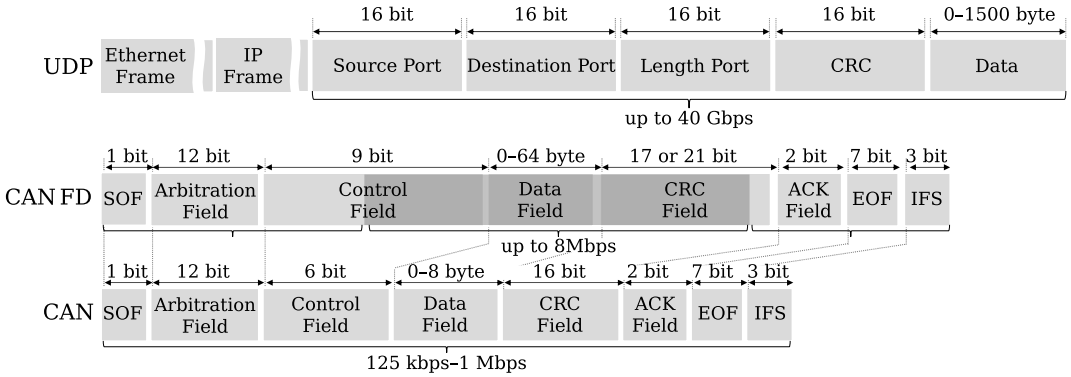


Figure 4.2: Structure and size of the User Datagram Protocol (UDP), CAN FD and CAN frames and the maximum transmission rates, With CAN FD, a part of the message is sent with a maximum of 1 Mbps for downward compatibility to CAN and a part with increased transmission rates up to 8 Mbps. The part of the message frame sent with increased transmission rates is highlighted in dark gray.

The energy required for the communication network influences the system efficiency of the respective application. Energy efficiency, small latency, and reliability are key features for the communication within network controlled systems like the DBMS. For battery condition-dependent control, the battery-specific data are communicated regularly. Based on these values, the (dis)charging power of the batteries is set by adjusting the DC-DC converters. With respect to the DBMS, additional conditions arise in addition to the aforementioned requirements. Current, voltage and temperature are measured regularly in millisecond intervals by all the participating nodes. Each data packet contains a time stamp and comprises only a few bytes in total. The measurement data are sent simultaneously to all participating nodes as quickly as possible. These data form the basis for the collaborative system control. Within the DBMS, it is therefore required to regularly send messages with few user data bytes quickly, reliably and without errors in order to achieve system-wide data consistency.
Subsequently the communication technologies Controller Area Network (CAN), Controller Area Network Flexible Data-rate (CAN FD) and Ethernet (Fig. 4.3) are compared. In the following, the term CAN (FD) is used when referring to both communication technologies CAN and CAN FD.

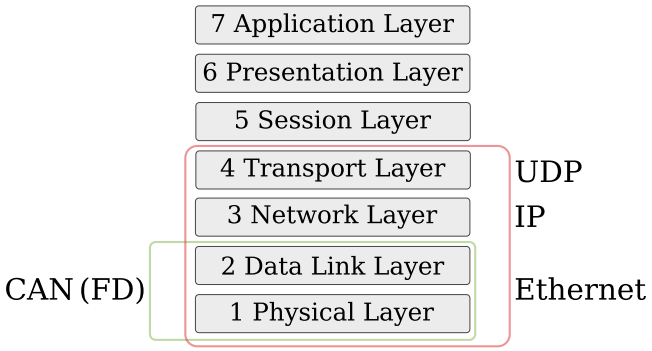


Figure 4.3: Layer of the Open Systems Interconnection (OSI) model covered by CAN, CAN FD and Ethernet.

CAN and CAN FD

CAN is a widely used bus protocol in distributed embedded cyber-physical systems. Its limited communication bandwidth (up to 1 Mbps) and payload size (up to 8 user data bytes) restrict the applicability in increasingly complex electronic systems (Fig. 4.2). CAN FD is a next generation of CAN with higher data transfer rate (up to 8 Mbps for the user data) and larger user data size (up to 64 user data bytes). Due to the compatibility between CAN and CAN FD and the increased user data rate, 0…8, 12, 16, 20, 24, 48 or 64 user data bytes per message frame are supported.

Ethernet based on User Datagram Protocol (UDP)

State-of-the-art Ethernet offers data rates up to the high Gbps (40 Gbps with 40 Gigabit Ethernet (GbE), 100 Gbps with 100 GbE) range via Twisted Pair (TP). In embedded systems, 100BASE-TX with 100 Mbps is most common, since higher data rates also increase processor and memory requirements. It offers a payload size up to 1500 bytes and provides low latency but is also more complex compared to CAN and

CAN FD. Ethernet offers various protocols, whereby the User Datagram Protocol (UDP) is used within this work as it is a relatively simple protocol compared to the Transmission Control Protocol (TCP). It avoids confirmation of correct message reception and thus supports unicast, multicast and broadcast communication. The size of the message header of the UDP is significantly reduced with a size of 8 bytes compared to the up to 60 byte header of the TCP. This offers additional advantages with regard to the transmission rate and the ratio of user data to overhead. Ethernet is not linked to TCP/IP, there are many other protocols, e.g., IEEE 1788 or Real-Time Streaming Protocol (RTSP). In the scope of this work the UDP/IP protocol stack is examined and is only one of several options.
For the evaluation of the energy efficiency, the maximum power consumption of the communication technologies are measured. To evaluate the transmission reliability, the Bit Error Rates (BER) and the Residual Error Rates (RER) are determined. Furthermore the message processing time and the processor load of each communication technology are measured as both influence the system control. Since networked control systems may consist of numerous participants, the behavior of the communication technologies under high network load is investigated.
Theoretical comparisons are made for a substantiated evaluation of the communication technologies. Data sheets, existing literature and simulations are referenced for this purpose. In addition, comparative tests within a hardware test setup enable practical, realistic results, especially for transmission speed, error susceptibility and behavior under high message load.
Section 4.3 provides a brief description of the required software components and presents the test setup (Fig. 4.1). Section 4.4 describes the evaluation criteria and the methods used to determine them. Section 4.5 shows and discusses the results. Finally, the communication technologies CAN, CAN FD and Ethernet are evaluated and compared with regard to the message processing time, processor load, energy consumption, error rate and receive-FIFO load at high traffic. A conclusion is drawn and a recommendation is given, especially for the DBMS.

4.2 Related Work

Existing work can be divided into analysis of communication in energy systems like smart grids or battery systems, in the automotive sector, and in networked control systems in general. For communication in smart grid applications [245–249], the technologies are mainly evaluated in terms of data rate, channel bandwidth, power consumption, and a coverage range. Furthermore, the effective retrofitting of existing power grid systems plays a significant role.
The considerations for battery management systems can be divided into wireless [250–252] and wired [253–255] approaches. Here, implementations are primarily described and criteria such as low power consumption, small volume, effective expandability, high message frame arrival ratio and low delay are used.
A majority of the papers comparing communication technologies focus on automotive applications [256–262]. The most important properties for in-vehicle communication include high transmission rates, low latency, appropriate bandwidth, low energy consumption and high reliability. Often it is investigated whether and to what extent Ethernet can replace more classical automotive communication technologies such as FlexRay, MOST or CAN and which (dis)advantages the replacement offers [257, 258, 260–262].

Communication analysis for general networked control systems [263, 264] mainly compare the communication technologies CAN and Ethernet or different Ethernet protocols with each other. Criteria include communication delays, real time capability, determinism, and the influence of all the previously mentioned on the overall control dynamics.
The following comparative analysis focuses on the relatively new (2015) CAN FD in addition to Ethernet and CAN. Furthermore, own comparison criteria adapted to the later use in the DBMS are defined. The results are relevant for communication in battery management systems as well as for networked control systems with low to medium distance between the controllers.

4.3 Setup of the Test Environment

The basis for the comparative analysis between CAN, CAN FD and Ethernet is the software implementation (Fig. 4.4) of the communication technologies and a test environment (Fig. 4.1). The test setup consists of software and hardware components.

4.3.1 Software Implementation

For a direct comparative analysis, the three communication technologies are utilized and measured individually. In addition, combined operation enables comparisons under identical conditions. The real time operating system FreeRTOS [265] is used in order to support multi threading (Fig. 4.4). CAN and CAN FD use the same

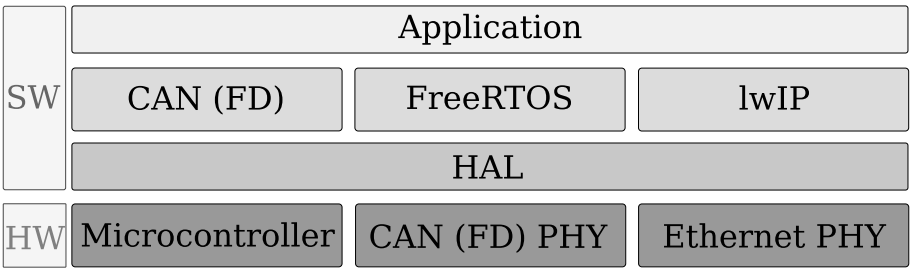


Figure 4.4: Overview of the software components and the interfaces between them required for the comparative analysis between CAN, CAN FD and Ethernet.

hardware module on the microcontroller and are therefore combined into one thread. To switch between CAN and CAN FD, mainly the header of the message frame, the CRC and the transmission rates are modified. Ethernet communication requires a software design that supports the protocols from the physical to the transport layer. The TCP/IP stack lightweight IP (lwIP) was specially developed for embedded systems and offers advantages in efficiency and program scope [266, 267]. lwIP supports several application program interfaces, whereby the RAW API offers high performance. lwIP provides functions to initialize the UDP module and also handles the Internet Protocol (IP), e.g., setting the IP address, subnet mask or gateway mask. The UDP thread is created after initialization and manages the sending and receiving of messages. The initialization of the entire periphery is performed by functions of the hardware abstraction layer (HAL).

4.3.2 Hardware Components for the Implementation of CAN, CAN FD and Ethernet Communication

For the hardware realization of the CAN, CAN FD and Ethernet communication, the evaluation board STM32H743ZI [268] and an external CAN transceiver [269] is used (Fig. 4.5).

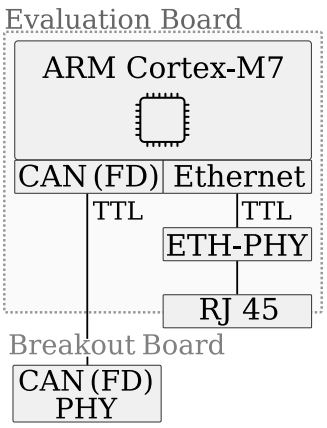


Figure 4.5: Block diagram of the hardware components for the implementation of the CAN, CAN FD and Ethernet communication: An evaluation board is used together with an external breakout board.

The evaluation board integrates an ARM Cortex-M7 processor and provides two modules for CAN (FD) and one module for Ethernet. Furthermore there is an Ethernet PHY and a RJ45 connector on the board, thus no further external hardware components are required for the implementation of the Ethernet communication. For CAN (FD) only the logic modules are available, therefore an external breakout board is added.

4.3.3 Test Setup for the Comparative Analysis

For the comparative measurements, two microcontrollers with corresponding interfaces and a test PC are connected to each other (Fig. 4.1). The test PC is used to monitor the network and to perform the tests.
The microcontrollers are connected to the CAN FD bus via CAN FD transceivers. For a connection between the test PC and the CAN FD bus a CAN-to-USB interface [270] is used. Both the test PC and the microcontroller used already integrate an Ethernet PHY and are connected directly to the Ethernet network via a Unshielded Twisted Pair (UTP) line. The Ethernet network is connected via a switch. For the determination of the message processing time of the Ethernet communication, the microcontrollers are also directly connected to each other via the RJ45-interface. For the measurement of the message processing time a logic analyzer is used, which is connected to the test PC via USB. The software is adapted for testing purposes in such a way that one GPIO pin is set high as a start signal when the messages are generated and another GPIO pin is set on the receiver side when the message is successfully extracted signaling the end of the transmission.

4.4 Selection of the Comparative Evaluation Criteria and Description of the Acquisition Methods

For a comparative analysis of the communication technologies CAN, CAN FD and Ethernet with regard to their application in networked control systems and especially within the DBMS, the following comparative evaluation criteria are determined:

- Message processing time,
- processor workload,
- energy consumption,
- error rate and
- RX-FIFO load.

All comparative measurements are performed with a transmission speed of 500 kbps for CAN, 500 kbps, 1 Mbps and 4 Mbps for CAN FD and with a transmission speed of 100 Mbps for Ethernet.

4.4.1 Message Processing Time Acquisition

For the comparison of the message processing time, the same number of user data is transmitted at identical link length of 1.5 meter between a transceiver and a receiver. The message processing time is measured with a logic port that monitors the start and stop pin. It consists largely of the transmission time and additionally of the computing time for packing/unpacking the message. The start pin is set to high immediately before the send command, while the stop pin is set after the message has been completely received (Fig. 4.6). This approach allows a comparison of the message processing times of the communication technologies.

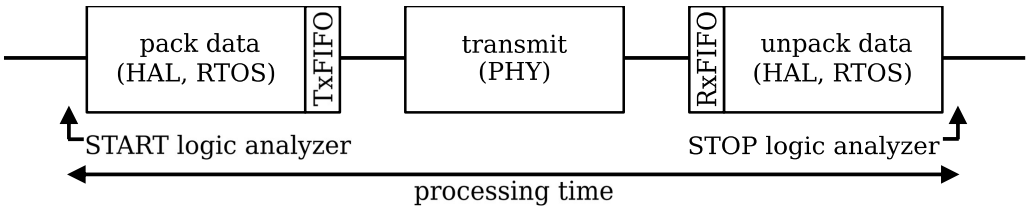


Figure 4.6: Measurement of message processing time: The start pin of the logic analyzer is set before the message is created and the stop pin is set after the message is completely received.

4.4.2 Processor Workload

For system control, operating parameters are recorded, system states are calculated and the corresponding data are managed by the microcontroller. Communication, in particular the preparation of message frames, sending and receiving messages, also places a load on the microcontroller. The processor load due to communication therefore also interacts with the system control. For this reason, the processor workload caused by the individual communication technologies is determined. The software adapted for measurement purposes causes an additional workload for setting the GPIO pins.

To specify the processor workload, the processor time allocated to the communication is measured. The measurement of the processor workload is divided into workload caused by the initialization and the sending or receiving of messages.

4.4.3 Energy Consumption

The energy consumption of the three communication technologies CAN, CAN FD and Ethernet is especially relevant for designing a battery management system, where overall system energy efficiency plays a significant role. Therefore, the energy consumption is determined both for each communication technology separately using the Power Consumption Calculator (PCC) from STMicroelectronics. The calculation is based on the data provided by the data sheet. The CAN (FD) and Ethernet sequences are analyzed. CAN and CAN FD use the identical peripherals and are therefore examined collectively in the CAN (FD) sequence. In each sequence, the energy consumption in run, idle and sleep mode are determined.

4.4.4 Error Rate

Correct data transmission is the basis for achieving effective control in networked control systems. Therefore, the error rate is also taken into account. In this context, the focus is on errors that occur during transmission or processing of the messages. Furthermore, a distinction is made between detected errors which are handled and undetected errors which are not handled and therefore have exceptionally damaging consequences.
To determine the probability of occurrence, the BER and the Residual Error Rate (RER) are defined. The BER is the number of bit errors in relation to the total number of bits sent (Equation (4.1)).

$$\mathrm{BER} = \frac{\#\text{Bit errors}}{\#\mathrm{Bits}_{\mathsf{total}}} \tag{4.1}$$

, whereby # represents the number.
The RER is the number of undetected, erroneous messages in relation to the total number of messages, whereby the Residual Package Error (RPE) is the number of undetected messages with errors (Equation (4.2)).

$$\mathrm{RER} = \frac{\mathrm{RPE}}{\#\mathrm{Messages}_{\mathsf{total}}} \tag{4.2}$$

For comparison of error rates, existing literature and data sheets are referenced.

4.4.5 RX-FIFO Load

A high transmission rate with a large volume of message traffic can lead to information loss. The messages are first stored in the corresponding RX-FIFOs and subsequently processed. If the messages are processed too slowly with constantly new incoming messages, a RX-FIFO overflow may occur and entries that have not yet been processed are overwritten. The load of the RX-FIFO is investigated in case of a high message load. Therefore, the test PC generates a correspondingly high quantity of numbered test messages.

4.5 Results and Discussion

In the following, experimental data as well as calculated values are presented and discussed for the comparative analysis of CAN, CAN FD and Ethernet.

4.5.1 Message Processing Time Measurements and Comparison

The message processing times were first measured for different user data lengths of 0, 8, 64 and 1500 bytes aligned with the maximum frame sizes of CAN, CAN FD and Ethernet (Tab. 4.1). The message processing time was measured using CAN with 500 kbps, CAN FD with 500 kbps, 1 Mbps and 4 Mbps as well as the direct Ethernet with 100 Mbps.
The highest message processing duration for a user data transmission of 0 up to 8 bytes is consistently CAN FD with 500 kbps. At the identical transmission rate as CAN, CAN FD is on an average 27 μs slower because of the significantly more extensive message header of CAN FD (Fig. 4.2). The main advantage of CAN FD is the Bit Rate Switch (BRS), i.e. the increased data rate compared to the arbitration rate. This is not exploited in case of a constant transmission rate of 500 kbps, but at a transmission speed of 1 Mbps and higher, the transmission time is reduced and CAN FD reveals its advantage over CAN.

Table 4.1: Measured message processing times for various transmission rates and user data bytes.

	Message processing time in μs				
User data bytes	CAN (500 kbps)	CAN FD (500 kbps// 500 kbps)	CAN FD (1 Mbps// 1 Mbps)	CAN FD (1 Mbps// 4 Mbps)	Ethernet (100 Mbps)
0	99.2	126.2	91.3	69.5	44.3
1	114.5	140.7	99.3	71.2	43.8
2	133.1	158.5	108.7	73.5	43.7
4	163.4	190.9	125.2	78	44
8	227.6	257.4	158.4	86.7	44
16	-	389.5	222.6	103.9	44.1
32	-	657.2	355.8	139.4	46.8
64	-	1171.4	611.8	208.3	53.4
1500	-	-	-	-	314.7

// is used to indicate the difference between the normal and the increased data transmission rates used for CAN FD

Since only the transmission time of the data phase is reduced, the effect of the BRS increases with an increasing number of user data (Tab. 4.1). The increased data rate is used for the user data and the CRC (Fig. 4.2). A further increase of the CAN FD data rate to 4 Mbps shows a considerable improvement of the message processing time, which is especially effective with a high amount of transmitted data bytes.

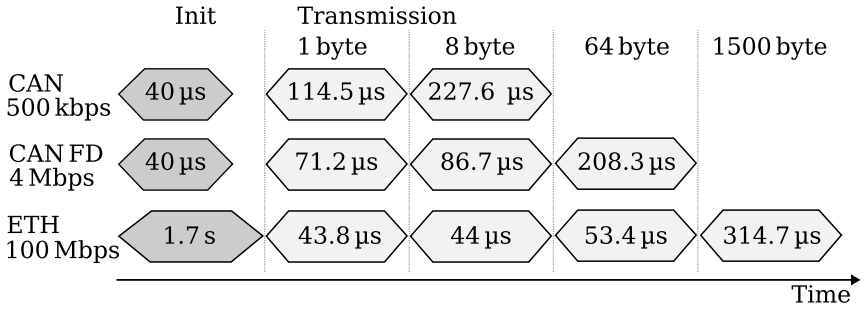


Figure 4.7: Init and message processing time for varying user data byte.

The message processing time of CAN FD is at any time significantly higher than the one of Ethernet. At 64 user data bytes, the time difference between CAN FD (4 Mbps) and Ethernet has increased to 155 µs. These differences become even more striking when the payload exceeds the frame size, i.e. multiple message packets are necessary.

Conclusion on the Message Processing Time Measurements

With a focus on the fastest possible data transmission, Ethernet is the communication technology of choice. Even with a payload of up to 64 bytes, the data transmission is significantly faster than with CAN FD. In addition, Ethernet enables user data transmission of up to 1500 bytes per message frame, which is significantly higher than the maximum of 8 user data bytes to be transmitted with CAN and the maximum of 64 user data bytes with CAN FD (Fig. 4.7).
Comparing CAN FD and CAN, it becomes clear that CAN FD only shows advantages over CAN when bit rate switching is used and the data rate is increased. Furthermore, it is shown that the effect of bit rate switching becomes more significant as the payload increases.
When selecting the communication technology, the number of user data bytes to be transmitted and the ratio between user data bytes and overhead due to the message frame should be taken into account. If the objective is to transmit as much user data as possible within minimum time, the advantages of Ethernet clearly outweigh those of CAN and CAN FD. For the transmission of fewer user data bytes in short intervals, as it is the case for example within the DBMS, CAN FD is definitely an option, especially if the transmission rate is further increased up to the maximum of 8 Mbps.

4.5.2 Measurement and Comparative Analysis of the Processor Workload

The processor time is measured to compare the processor load caused by the respective communication type. The measurement is divided into required processor time for initialization, for CAN and CAN FD and for Ethernet. For the determination of the processor load of the individual communication technologies, the computing time of the individual threads is determined. Measuring processor time is fundamentally challenging because it is affected by several factors. Ethernet communication requires multiple threads and consequently variations in processing time are expected. A

function already provided by FreeRTOS (`vTaskGetRunTimeStats`) is used for this purpose.
The function `vTaskGetRunTimeStats` is passed a char pointer to a sufficiently large memory area in which the data are stored. The computation time is determined by summing up the number of ticks a thread spends in the active state. For this purpose a timer with an appropriate sampling frequency is used. For the sampling frequency a value 10 to 100 times higher than the frequency of the RTOS interrupt is recommended [266]. In this case, the 32 bit timer TIM5 was selected with a sampling frequency of 100 MHz. The ticks are calculated by periodically retrieving the timer's count register.
The following steps are prerequisites for the data collection:

- The macro for creating the statistic in FreeRTOSConfig.h must be set to the value one.
- The macro `Configure_TIMER_FOR_RUN_TIME_STATS` must be configured to start the timer required for the ticks.
- The macro `GET_RUN_TIME_COUNTER_VALUE` must be configured to return the current timer count value.

The recorded computation times of the single threads are transmitted via UART to the terminal of the test PC.

Processor Time Required for Initialization

The initialization of the communication technologies is executed once at system startup or after a reset. The initialization time for CAN (FD) is approx. 40 µs, whereas Ethernet requires 1.7 s and is over the factor 40000 greater than the initialization time of CAN (FD) (Fig. 4.7). Especially if an unexpected restart of the microcontroller and the applied real time system occurs, the long downtime of the subscriber has consequences, including loss of information and the associated effects on system control and coordination.

Processor Workload Required for CAN (FD) Communication

First, the processor load for CAN (FD) communication for sending and subsequent receiving 1000 messages is measured. Varying numbers of messages showed a linear behavior between the CAN FD process and the number of messages. The processor time of the CAN FD process increases with the number of messages.
The processor times were measured for intervals of 0.2 ms, 0.3 ms, 1 ms and 10 ms (Figs. 4.8, 4.9). For shorter intervals between messages, the processor time share for the CAN FD thread increases slightly. With the shortest message interval of 0.2 ms, the share of the CAN FD thread process still is only 1.5% (Fig. 4.9). The measurements show that the CAN FD communication only places a low overall load on the processor and cannot overload the processor due to communication channel restrictions limiting the transmission speed beforehand.
Measurements for CAN communication showed that it requires 10 µs less processor time for 1000 messages compared to CAN FD communication. Examining the percentage processor utilization, there are no differences compared to CAN FD communication. Therefore only the CAN FD measurements are used for the comparison with Ethernet.

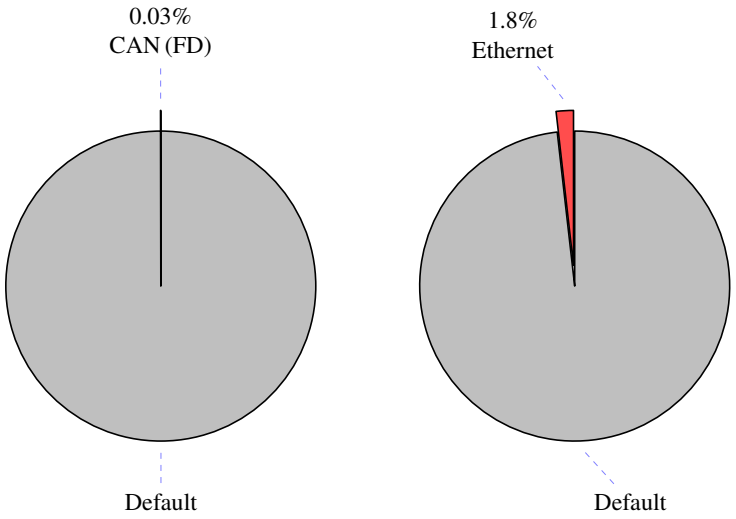


Figure 4.8: Processor times for a periodic send interval of 10 ms.

Receiving and unpacking CAN (FD) messages is handled by an interrupt service routine and depends on the length of the user data. For 8 user data bytes, e.g., it takes 3.3 µs whereas it takes 7.8 µs for 64 user data bytes (Fig. 4.13).

Processor Workload Required for Ethernet Communication

The measurement of the processor times for sending Ethernet messages show that the processor times do not behave linearly, especially for a few messages, in contrast to the processor times for CAN (FD). The reason for this are threads, which are executed in a fixed time interval independent of the number of messages.
The shorter the message interval, the more processor time is required by the Ethernet threads. With a send interval of 10 ms the Ethernet communication requires only 1.8% of the processor time while with a send interval of 0.2 ms it already requires 23.8% of the processor time (Figs. 4.8, 4.9).
If the increase is linear to the send intervals, it is possible that the processor utilization limit occurs before the send interval limit of Ethernet, which is 5 µs. This behavior was not investigated in this work because such a short send interval is not necessary for the DBMS.

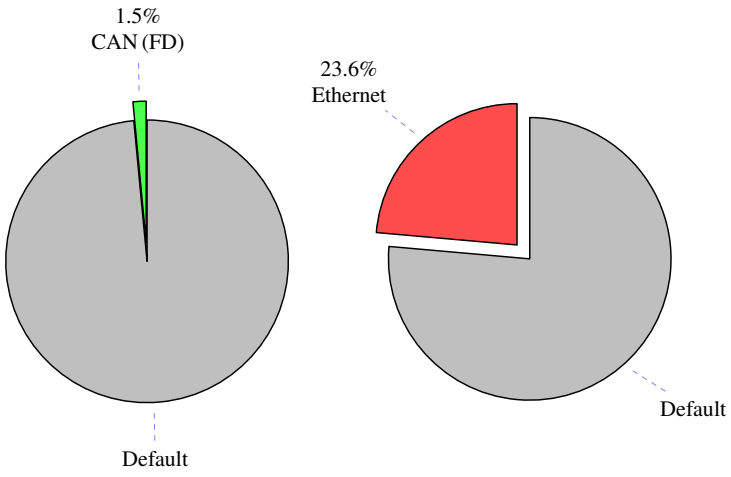


Figure 4.9: Processor times for a periodic send interval of 0.02 ms.

The measurements show that Ethernet communication requires significantly more processor time than CAN (FD) communication. At a transmission interval of 0.02 ms, Ethernet requires 23.8%, while CAN (FD) requires only 1.5%. The processor times are additionally strongly dependent on the transmission intervals. With a message interval of 10 ms, e.g., Ethernet only requires 1.8% of the processor time. The processor load therefore depends on the communication technology and additionally on the selected message interval. For the selected minimum message interval, neither Ethernet nor CAN (FD) communication significantly burdens the processor.
For receiving and unpacking Ethernet messages a separate thread and an interrupt service routine is used. For 8 user data bytes, it takes 18 µs, which is significantly longer compared to the duration of 3.3 µs for CAN (FD) messages. With the maximum of 1500 user data bytes, receiving and unpacking the message takes 83.9 µs.

4.5.3 Comparison of the Energy Consumption

The energy consumption of the communication technologies is calculated in run, idle and sleep mode respectively. Since the same peripheral units are used for CAN and CAN FD communication, the energy consumption is combined for both types of communication. The processor operates constantly with a frequency of 400 MHz and an operating core voltage of 1.2 V. The operating voltage of the peripherals is 3.3 V. The total energy consumption is calculated in each case, including the necessary peripheral units, system components and the supply of external peripherals. For Ethernet communication, significantly more peripheral units and system components are required and additionally the cache is utilized.

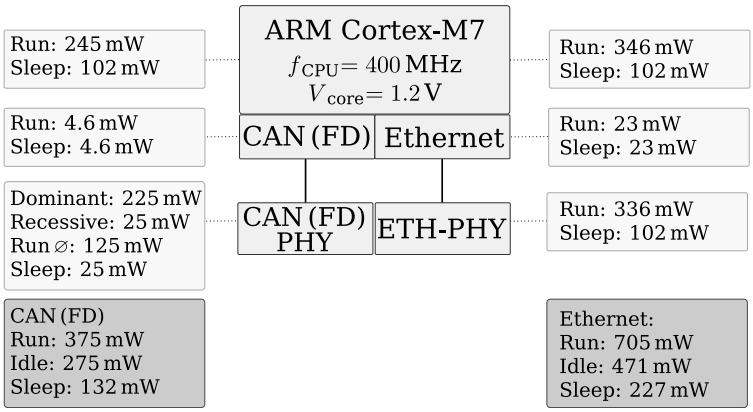


Figure 4.10: Energy consumption of the CAN (FD) and Ethernet communication divided among the peripheral units in run, sleep and idle mode [268, 271–273].

Figure 4.10 and 4.11 show the total energy consumption for CAN (FD) and Ethernet communication in run, idle and sleep mode.
CAN (FD) communication requires significantly less power than Ethernet communication in all three modes. In run mode, the power required for CAN (FD) of 375 mW is just 53.2% of the power required for Ethernet. Similarly, in sleep and idle mode, the power required for CAN (FD) is only about 58% of the power required for Ethernet. For Ethernet and CAN (FD) the sleep mode is significantly more efficient than the idle mode. Only 48% of the power required for idle mode is consumed in sleep mode.

Table 4.2: Current consumption of the single utilized peripheral units at a core supply voltage of $V_{\text{Core}} = 1.2V$.

Peripheral	Description	Current in mA
FDCAN1	Module for CAN FD	2.38
TIM5	32 bit timer for FreeRTOS	0.32
USART3	USART for Debugging	0.56
GPIOB	Status LED	0.2
GPIOD	UART and CAN	0.22
SYS	SysTick	0.1
APB1	Advanced periperhal bus (APB) for timer, UART and CAN FD	0.01
AHB4	Advanced high-performance bus (AHB) for GPIO	0.02
APB4	APB for clock generation	0.01

For energy-efficient applications, CAN (FD) communication shows clear advantages with almost 50% lower power consumption than Ethernet. For all three communication tech no lo gies, using sleep mode instead of idle mode shows a significant improvement in energy efficiency. If Ethernet is required due to its significantly higher transmission rate, the sleep mode should be considered with regard to energy efficiency.

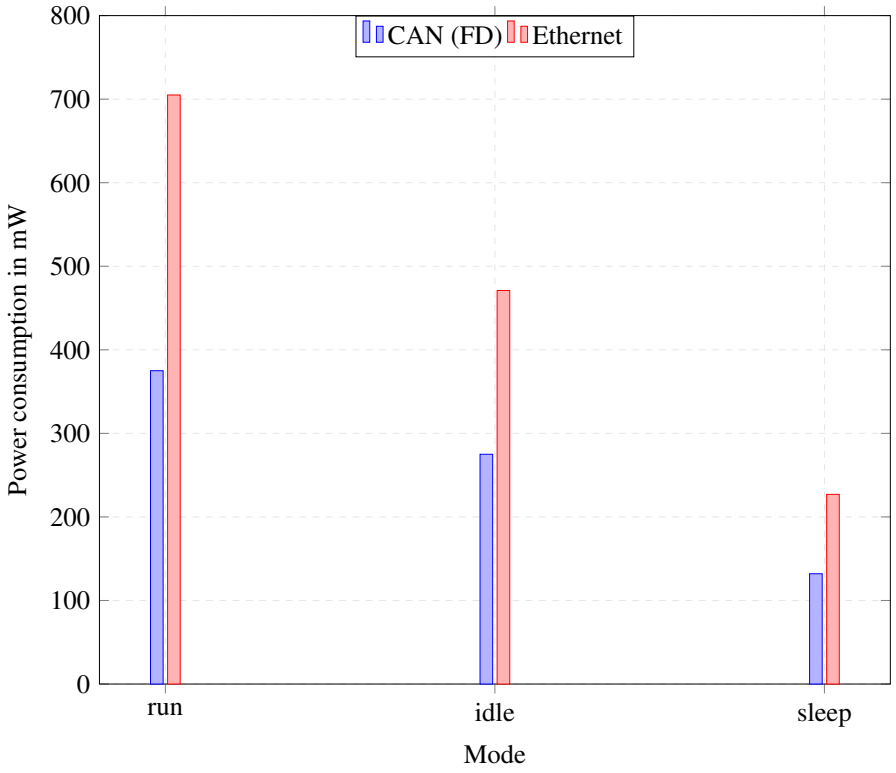


Figure 4.11: Comparison of the power consumption for CAN (FD) and Ethernet communication divided into run, idle and sleep mode [268, 271–273].

4.5.4 Error Rates

The error rates provide information about the reliability and the correctness of the data transmission. The RER of CAN (FD) communication is officially specified as $4.7 \cdot 10^{-11}$ [274, 275], whereas no official data is available for 100BaseT Ethernet. Direct Code Analysis (DCA) is used to determine the RER, which depends mainly on the polynomial of the CRC, the BER, and the frame length [276, 277]. DCA generates all possible error patterns, resulting in a sharp increase in computational effort with data length. Considering the three mentioned factors, all possible error patterns A_i are generated, which can produce an undetected error. These patterns A_i are numbered firmly afterwards. Subsequently, the upper (P_{upper}) and the lower (P_{lower}) limit of the probability of an undetected error are determined as follows:

$$P_{\text{upper}} = \sum_{i=D}^{N_{\text{Data}}} A_i \cdot {p_{\text{error}}}^i \cdot (1 - p_{\text{error}})^{N_{\text{Data}} - i} \tag{4.3}$$

$$P_{\text{lower}} = 2^{-r_{\text{CRC}}} \cdot \sum_{i=D}^{N_{\text{Data}}} A_i \cdot {p_{\text{error}}}^i \cdot (1 - p_{\text{error}})^{N_{\text{Data}} - i} \tag{4.4}$$

N_{Data} is the length of the data, D the Hamming distance, p_{error} the probability of a bit error and r_{CRC} the degree of the generator polynomial of the CRC.[277]
Figure 4.12 shows the upper and lower limits of the RER for CAN with a data frame of 8 bytes and 15 bit CRC and for Ethernet with a data frame of 42 bytes and 23 bit CRC [276].

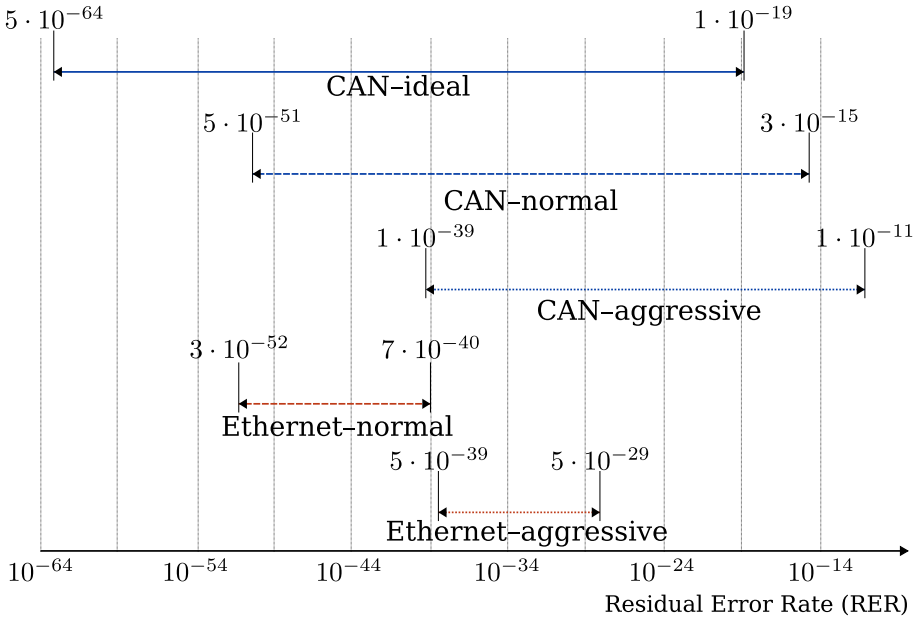


Figure 4.12: Upper and lower limits for RER for CAN [278] and Ethernet [277] in different environments determined by using DCA [276].

To determine the BER, a large number of messages are sent under different conditions and the number of bit-erroneous messages is obtained. Table 4.3 shows the BER for CAN at 8 user data bytes [278] and for Ethernet at 1468 user data bytes [277].

Comparison Regarding the Susceptibility to Errors

Ethernet has a calculated maximum RER of $7 \cdot 10^{-40}$ while CAN has a RER of up to $3 \cdot 10^{-15}$. Ethernet shows clear advantages in the RER, which has a greater impact due to non-detection, compared to the BER. All RER values are significantly below the limit value of 10^{-7} defined in ISO 61508 and ISO 26262, which has to be observed for communication technologies in safety critical applications. The BER of Ethernet is also smaller than the one of CAN by a factor of approximately 10. Ethernet therefore shows a clear advantage with regard to the error rate.

4.5.5 RX-FIFO Load

To test the RX-FIFO load, random messages were generated. For CAN, CAN FD and Ethernet no noticeable RX-FIFO load occurs. Table 4.4 shows the message processing time, which includes message generation, the transmission and the unpacking of the messages, compared to the pure message receiving and unpacking time. When comparing these times and taking into account that all communication participants share a common communication bus, it is evident that no significant RX-FIFO load occurs (Fig. 4.13). The RX-FIFO utilization increases with the message receiving

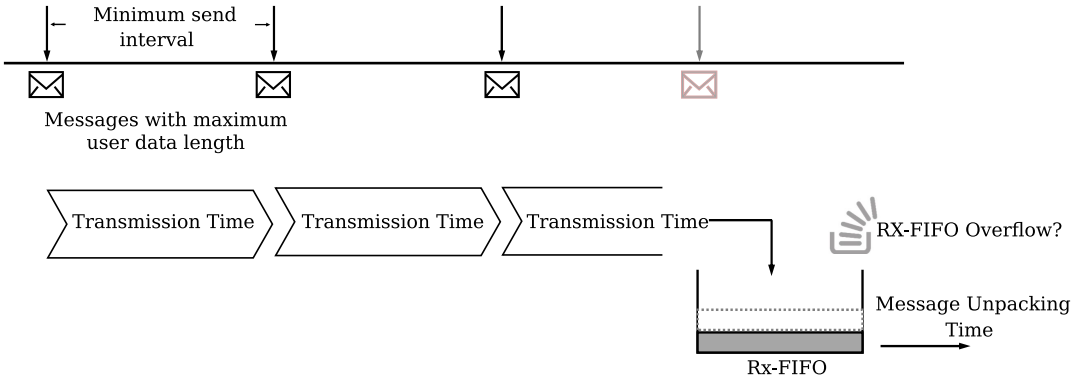


Figure 4.13: An RX-FIFO overflow results in message losses which can negatively influence the control. Therefore, the maximum number of user data bytes is sent with the highest data rate in the smallest possible interval and the utilization of the RX-FIFO is analyzed.

and unpacking time. CAN is particularly advantageous here with a receiving and unpacking time of 3.3 µs for the maximum 8 user data bytes. Ethernet takes 83.9 µs for receiving and unpacking 1500 bytes of user data, which is significantly longer in comparison to CAN (FD). The ratio of the unpacking time to the message processing

Table 4.3: BER of CAN and Ethernet for different environments [277].

Environment	BER of CAN	BER of Ethernet
Ideal	$3.0 \cdot 10^{-11}$	-
Normal	$3.1 \cdot 10^{-9}$	$3.35 \cdot 10^{-10}$
Aggressive	$2.6 \cdot 10^{-7}$	$3.0 \cdot 10^{-8}$

Table 4.4: Comparison of the message processing time and the message unpacking time.

	CAN	CAN FD	Ethernet
Transmission rate:	500 kbps	4 Mbps	100 Mbps
Send interval:	300 µs	200 µs	120 µs
User data:	8 byte	64 byte	1500 byte
Message processing time:	227.6 µs	208.3 µs	314.7 µs
Message receiving and unpacking time:	3.3 µs	7.8 µs	83.9 µs

time of 314.7 µs and the minimum possible transmission interval of 121 µs, still indicates that the RX-FIFO is not significantly loaded.

4.6 Summary

The application of the communication technologies CAN, CAN FD and Ethernet in networked control systems and especially in the DBMS was evaluated on the basis of the criteria message processing time, processor load, power consumption, energy consumption, error rate and RX-FIFO load (Tab. 4.6).

Table 4.5: Summary of the comparative analysis of CAN, CAN FD and Ethernet.

	CAN	CAN FD	Ethernet
Payload data	low	low - medium	high
Message processing time	+	++	+++
Processor workload	+++	+++	+
Energy consumption	+++	+++	+
Error rate	++	++	+++
RX-FIFO load	+++	+++	++

+++: outstanding
++: completely fulfilled
+: sufficient

In terms of message processing time, Ethernet showed significant advantages due to its high transmission rate of 100 Mbps (Tabs. 4.5, 4.6). When transmitting 8 user data bytes, Ethernet is approximately 80% faster than CAN and 50% faster than CAN FD. CAN FD already shows clear benefits over CAN. For the transmission of 8 user data bytes, CAN FD with a data rate of 4 Mbps is 60% faster than CAN.
None of the investigated communication technologies noticeably burdens the processor. With a transmission interval of 200 μs, CAN (FD) communication requires only 1.5% of the processor, while Ethernet requires 24%.
For energy-efficient applications, CAN (FD) is preferred as it consumes 50 percent less power than Ethernet.

In terms of error probability, Ethernet offers advantages with at least a 10-fold lower error occurrence, whereas all communication technologies are suitable for safety-critical systems due to their low error probability. CAN, CAN FD and Ethernet did not show any noticeable load on the RX-FIFO due to the short receive and unpacking times in relation to transmission times.
Ethernet offers excellent characteristics in the transmission of large data amounts and in the error rate, but it requires significantly more power and processor time. The long init time of Ethernet is critical for real-time systems and networked control systems. For these applications, an Ethernet implementation without lwIP has to be considered. CAN FD has significant benefits in terms of message processing time, even with few user data, and requires the same amount of power and processor time as CAN. In addition, CAN FD offers the possibility to transmit up to 64 user data bytes and to increase the data rate even further. Furthermore, microcontrollers with less powerful processors can be used for CAN (FD) communication, which reduces the costs. For these reasons, CAN FD is evaluated as the most appropriate communication technology for the DBMS (Fig. 4.14). For applications with a higher number of user data bytes, Ethernet remains the communication technology of choice. In further comparative analyses, Controller Area Network Extra Long CAN XL [279], Energy Efficient Ethernet (EEE) [280] and Ethernet Time Sensitive Networking (TSN) should be considered. CAN XL, with a maximum user data transfer of 2048 bytes and data transfer rates of up to 10 Mbps, is the successor to CAN FD. With the higher data rates and number of user data, the gap between CAN and Ethernet is steadily closing. EEE is an extension of Ethernet with the aim of reducing power requirements. Ethernet TSN is a standard extension of the IEEE with the aim of achieving real-time capability of Ethernet. Among other things, real-time capability is enhanced by time synchronization, prioritization, scheduling, traffic shaping and resource reservation [281] and is promising for networked control systems.

Table 4.6: Summary of the results of the comparative analysis of CAN, CAN FD and Ethernet.

Communication Technology	User Data Byte	Transmission Rate	Message Processing Time	Processor Workload[1]	Power[2]	Energy[3]	Rx FIFO Load[4]	BER[5]	RER[5]
CAN	≤ 8	125 kBit/s – 1 MBit/s	500kBit/s 8 byte 227.6 µs	0.03% 1.5%	375 mW 275 mW 132 mW	4.5 mWh – 4.6 mWh	low send interval: 300 µs processing: 3.3 µs	$5 \cdot 10^{-64}$ $1 \cdot 10^{-11}$	$5 \cdot 10^{-51}$ $3 \cdot 10^{-15}$
CAN FD	≤ 64	1 MBit/s – 8 MBit/s	1//4 MBit/s 64 byte 208.3 µs	0.03% 1.5%	375 mW 275 mW 132 mW	4.58 mWh – 4.59 mWh	low send interval: 200 µs processing: 7.8 µs	/	/
Ethernet UDP	≤ 1500	10 MBit/s – 40 GBit/s	100 MBit/s 64 byte 53.4 µs	1.8% 23.6%	705 mW 471 mW 227 mW	7.84 mWh – 7.85 mWh	medium send interval: 120 µs processing: 83.9 µs	$3 \cdot 10^{-52}$ $5 \cdot 10^{-29}$	$3 \cdot 10^{-52}$ $7 \cdot 10^{-40}$

1 Measured for a periodic message send interval of *i*, 10 *ms* and *ii*, 0.2 *ms*
2 Estimated power consumption in *i*, run, *ii*, idle and *iii*, sleep mode
3 Calculated energy consumption for 1 min for a message frequency of *i*, $f_m = 1$ Hz and *ii*, $f_m = 100$ Hz
4 Time analysis with maximum message frequency and maximum number of user data per message
5 RER and BER for *i*, normal and *ii*, aggressive environment

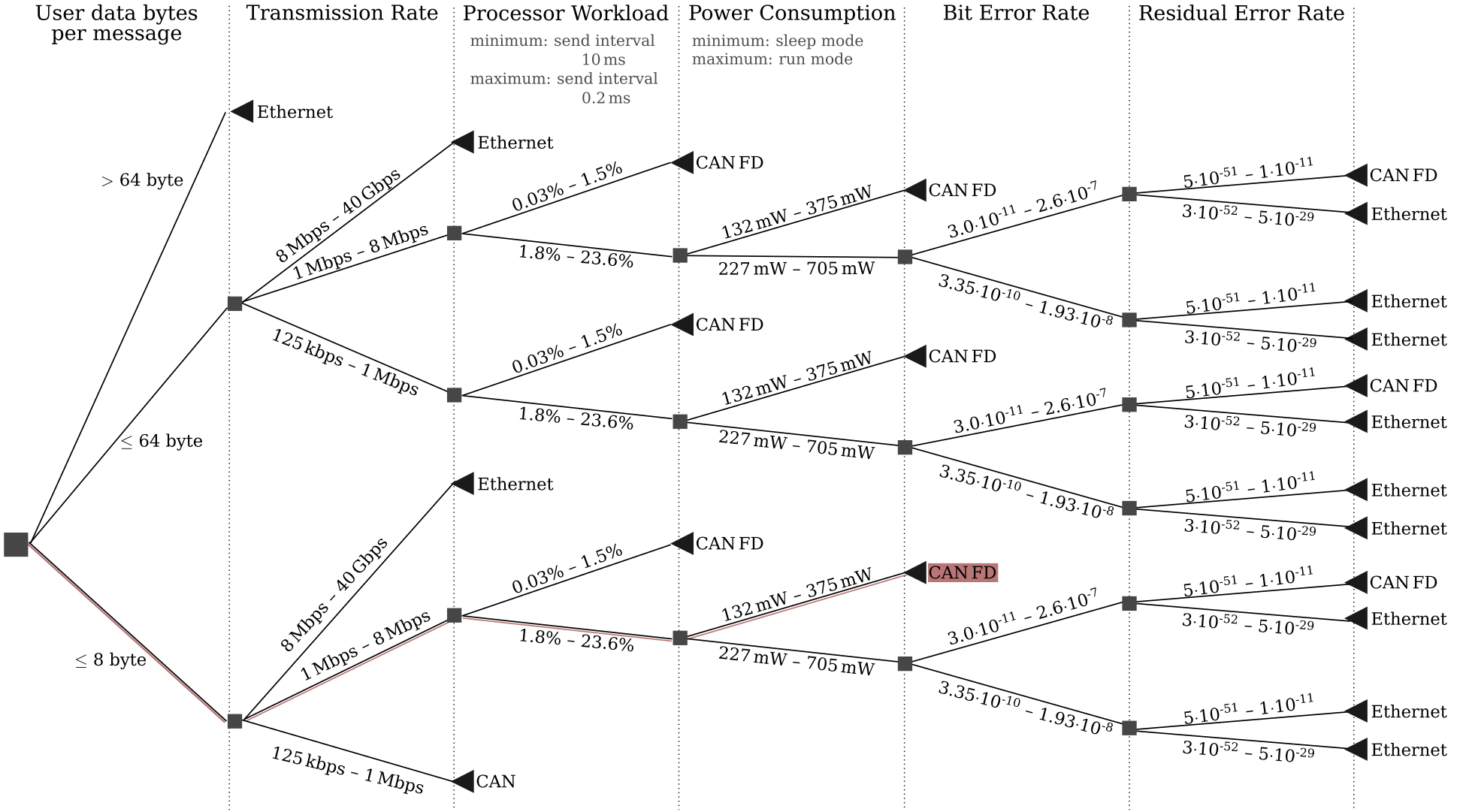


Figure 4.14: Decision matrix for the selection of the communication technology: For the selection of the communication technology in the DBMS (marked in red), the low number of user data and the significantly lower power requirement were the decisive factors.

5

Leader Election for the Coordination of the System Tasks

In the decentralized, distributed battery management system, functionally equivalent nodes work together to form a system with improved availability, reliability and fault tolerance. In this way, the common control objective of maintaining the DC link voltage in the presence of battery state-dependent load sharing and volatile generators and loads aims to be achieved. As multiple components cooperate to accomplish tasks, coordination among them is required. Electing a node as the temporary leader can be a possible solution to perform coordination. This chapter presents a self-stabilizing algorithm for the election of a leader in dynamically reconfigurable bus topology-based broadcast systems with a message and time complexity of $\mathcal{O}(1)$. The election is performed dynamically, i.e., not only when the leader node fails, and is criterion-based. The criterion used is a performance related value which evaluates the properties of the node regarding the ability to perform the tasks of the leader. The increased demands on the leader are taken into account and a re-election is started when the criterion value drops below a predefined level. The objective here is to distribute the load more evenly and to reduce the probability of failure due to overload of individual nodes. For improved system availability and reduced fault rates, a management level consisting of leader, assistant and co-assistant is introduced. This reduces the number of required messages and the duration in case of non-initial election. For further reduction of required messages to uniquely determine a leader, the CAN protocol is exploited. The proposed algorithm selects a node with an improved failure rate and a reduced message and hence time complexity while satisfying the safety, and termination constraints. The operation of the algorithm is validated using a hardware test setup consisting of five microcontroller nodes.

5.1 Motivation

In contrast to centrally structured systems, decentralized, distributed systems consist of multiple functionally equivalent peer nodes working towards a common control

objective. Such systems offer several advantages including improved reliability, system availability, scalability and flexibility. Decentralization aims to reduce possible single points of failure, such as master controllers in centralized systems, and thus enhance the robustness and fault tolerance of the system.
In order to effectively utilize the computing and control power of the individual nodes, all of them work collaboratively on the system control tasks. As they work together, they must be coordinated to build a coherent and efficient system. The coordination among these nodes is essential and significantly affects the overall system performance.
Electing one of the nodes as a temporary leader is a possible solution to reduce the complexity of the coordination without imposing a potential single points of failures. Besides coordination, the temporary leader also manages several additional activities such as task definition and assignment, aggregation of measurement results, clock synchronization, and the process of adding or removing nodes.
The election must lead to an unambiguous result in the shortest possible time, because an uncoordinated system suffers from inconsistency, inefficiency, performance degradation, and negatively affects the control.
In this chapter, a Leader Election Algorithm (LEA) is proposed for a dynamically reconfigurable bus topology-based system consisting of n peer nodes. In principle, the LEA can be used in any broadcast capable system including FlexRay or Ethernet based systems. In the following, the exemplary use case of the LEA in a CAN FD based decentralized battery management system is shown. Other possible use cases include automotive or automation applications. The main contributions of this chapter can be summarized as follows:

- The criteria of maximum system availability, low failure rate, and uniformly distributed load were considered in the development of this LEA. The proposed dynamic criterion-based election algorithm is designed for a reconfigurable, scalable bus-topology-based system. These features improve the reliability and the competence of the temporary leader.

- The concept of the management level consisting of leader, assistant and co-assistant is introduced to effectively detect faulty or inactive leader nodes and to reduce the time of re-election and the associated downtime of the system coordination.

- For the optimization of the message and time complexity of the election process, a principle is proposed that uses the CAN message format to reduce the number of required election messages. This leads to a message and time complexity of $\mathcal{O}(1)$ for a number of nodes corresponding to common bus communication systems.

- The operation of the algorithm and its termination is proven by a hardware test setup consisting of five nodes.

The rest of this chapter is organized as follows. Section 5.2 shows related work. Section 5.3 describes the system for which the LEA is designed and Section 5.4 analyses the requirements for the leader election. In Section 5.5, the LEA based on the CAN-bus (LEA-CAN) is presented, the election messages are defined, two election procedures (big LEA-CAN, small LEA-CAN) are described, the message overhead is analysed, and the error handling is presented. Finally, the hardware test setup is shown (Section 5.9) and a conclusion is drawn.

5.2 Related Work

Existing Leader Election Algorithms can be distinguished in random [282] and criterion based [283–285] ones (Fig. 5.1]).

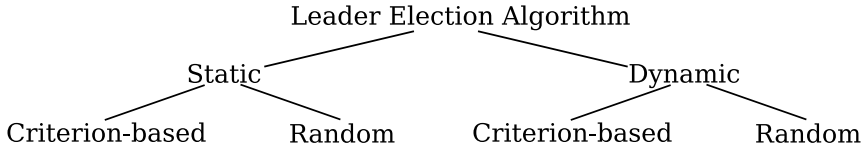


Figure 5.1: Existing leader election algorithms can be divided into static and dynamic ones based on the repetition frequency. They can further be classified into criterion-based and random.

Another differentiation is the repetition of the election. Static algorithms perform a new election only if the leader fails [286, 287]. Periodic and dynamic election algorithms perform re-election even when the leader is intact. Periodic algorithms execute time-based re-elections [288]. Dynamic algorithms perform re-election based on the change of performance-related variable parameters such as battery life [289]. The underlying architecture is another differentiating factor of existing leader election algorithms. Examples include ring based systems [290–292], 2D torus network [293] and algorithms specifically for unknown topologies [294–296]. Another characteristic is the time and message complexity [296–299].

5.3 System Description

The decentralized system for which the LEA-CAN was developed consists of n nodes, where $n \in \{4 \dots 64\}$. The distributed nodes are connected with a common CAN (FD) line (Fig. 5.2). They exchange information relevant to the execution of the system tasks including locally measured values and state parameters. The way the CAN message identifier is used limits the maximum number of participating nodes (Fig. 5.3). For a first realization the 11 bit CAN identifier is used, whereas the 29 bit identifier allows an extension of the number of participating nodes.
The message identifier is thereby split into a five bit priority ID to describe the type and urgency of the sent message and into a six bit node ID to identify the sender node.
The system is dynamically reconfigurable, which means that nodes can be added or removed even after an initial installation. The restriction of the maximum number of nodes results from the 6 bit node ID.
Each node is elective and selectable as a leading node. It is characterized by a unique node ID for identification and a Node Weight (NW).

5.3.1 Node Weight

The Node Weight (NW) evaluates the performance-related characteristics of the node in terms of its ability to perform the leader's tasks. This value also takes into account the duration of the last leadership and the passed time since that last leadership. The tasks of the management level require an increased computational effort and demand on the control power. Therefore, the duration of the last leadership is taken into account when determining the NW. The duration is recorded in terms of the

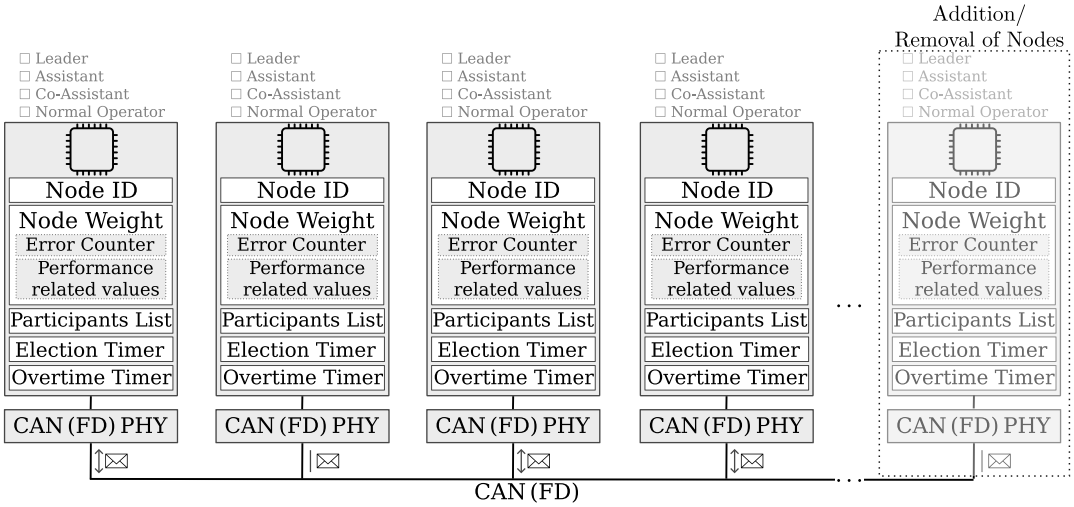


Figure 5.2: The dynamically reconfigurable system consists of n nodes, which all have a unique node identifier (ID) and a node weight (NW), i.e. a performance related value which is also used as an election criterion. The nodes are connected with a common CAN (FD) line. Each node is able to send and receive messages, is eligible to vote and can be elected as leader, assistant or co-assistant.

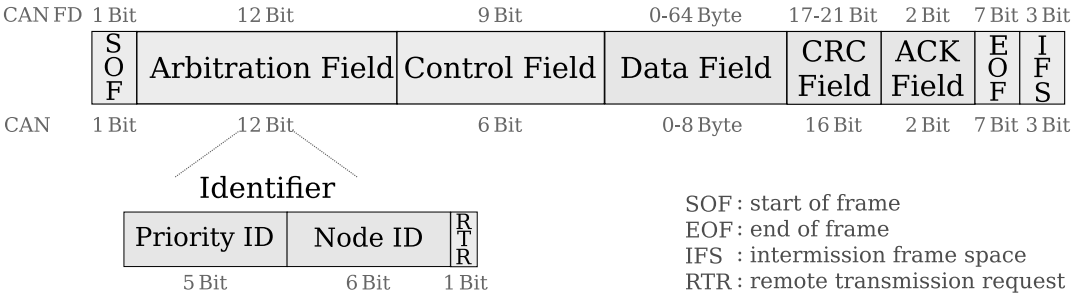


Figure 5.3: CAN or CAN FD is used for communication between the nodes. The 11 bit message identifier is split up into a 5 bit priority identifier, which shows the type and urgency of the sent message, and a 6 bit node identifier, which shows the node ID of the sender. The node ID limits the maximum number of participating nodes to $n_{\max} = 2^6 = 64$.

number of heartbeat messages sent during the leadership. Heartbeat messages are sent periodically by the leader and assistant for synchronization, management level status monitoring, and system task coordination. Participating nodes are able to detect the failure of the leader or assistant by the absence of these heartbeat messages.
In addition, an error counter is taken into account determining the NW. The error counter is incremented in case of faulty task assignment, actual value acquisition and set point setting. All nodes have internal error counters. If they send wrong actual values considering the maximum possible sensor deviation, their error counter is increased. Error messages make the faulty nodes aware of their incorrectly measured actual values and increase their error counters. If the subsequent values are again correctly recorded or specified, the error counter is reduced iteratively. Reliable, correct actual value acquisition and set point specification is essential for the leader. Therefore, the error counter, which manages measurement and calculation errors of the node, is included in the determination of the NW. Since the NW takes into account various criteria, the weighted sum approach is used to determine it [300–302].

5.3.2 Determination of the Node Weight for the Decentralized Battery Management System

Following, the determination of the node weight for nodes of a decentralized battery management system is shown as an example. The node weight takes the following functions into account:

- Battery state evaluation $f_1(T, SoC, SoP, SoH, C_N)$, with battery Temperature T, State of Charge SoC, State of Power SoP, State of Health SoH and normed Capacity C_N.
- Evaluation of the state of charge $f_2(SoC)$.
- Evaluation of the duration since the last leader election $f_3(t)$.
- Evaluation of the duration of the last leadership $f_4(t)$.
- Evaluation of the error counters (CAN, UART, Timer, Election) $f_{5,j}(x)$ where j=4.

For the calculation of the weighted sum, a weight w_i is chosen for each objective function and it follows:

$$\sum_{i=1}^{k}(w_i \cdot f_i) \text{ where } w_i > 0 \text{ for all } i \in 1,...,k \text{ and } \sum_{i=1}^{k} w_i = 1 \tag{5.1}$$

5.3.3 Participants List

The nodes maintain local participant lists (Fig. 5.2) sorted by NW, in which they manage the data of the remaining nodes. At system startup or (re-)activating individual nodes, the nodes send *Hello* messages which, in addition to the user ID and node weight, contain all other data relevant for system control, such as maximum current, capacity or permissible operating temperature range. If a node is removed, for example for maintenance purposes, it first sends a *Can I leave?* message. Upon confirmation from the leader, it sends a *Goodbye* message stating that it is going to be deactivated, and the remaining nodes remove the corresponding entry from their lists and take over its system tasks.

5.3.4 Tasks of the Management Level

The task of the management level is to coordinate the system control. For setpoint specification and synchronization of the distributed nodes, the leader and assistant periodically send heartbeat messages, which contain the individual setpoint specifications of the actuator nodes in the data field. The foundation for the definition of the setpoints is the data basis of the participant list. Furthermore, the temporary leader re-adjusts the remaining control deviation. In case of significant deviations between the specifications of the leader and the assistant, a majority decision is made with the co-assistant and the faulty management node is identified and deselected. In addition, the temporary leader gives the approval to deactivate individual nodes and coordinates additional system tasks such as pending software updates.

5.4 Requirements Analysis

In the following, the key requirements for the LEA are summarized.

Dynamic Criterion-based Election

Since the tasks of the temporary leader are different from those of the rest of the nodes, a criterion-based dynamic election algorithm is needed. The criterion is a performance-related value that evaluates the characteristics of a node in terms of its ability to perform the tasks of the leader. This value also takes into account the burden that the execution of the leader tasks entails. After the performance value of the temporary leader decreases, a new election is performed dynamically, even if the current temporary leader is still functioning.

Election of the Management Level

In addition to the leader, an assistant and a co-assistant are elected. The assistant supervises the task specification of the temporary leader. In case of conflicts between the leader and the assistant, a majority decision is made together with the co-assistant and the malicious node is deselected. The introduction of the leader level consisting of assistant and co-assistant offers besides the possibility to detect and deselect a harmful leader, the advantage of a shortened election process in case of a non-initial election. In this case, the roles of the leader level are first exchanged and subsequently a node is elected as co-assistant.

Extreme Value Search

To determine the management level, it is necessary to find the nodes with the extreme values of the election criterion. Locating extreme values can additionally be used, e.g., for control and monitoring tasks.

Dynamically Reconfigurable System

Nodes, including those from the management level, can be removed or added on the fly. The LEA has to be scalable within a certain range and has to cope with a changing number of nodes. In addition, strategies are required to keep the system stable in case a node of the management level is removed.

Reduction of the Election Time and the Required Messages

A distributed, uncoordinated system can suffer from inconsistency and performance degradation due to asynchronously operating nodes, worst case leading to the inability to complete the system tasks. Therefore, the management level and especially the temporary leader have to be elected within the shortest possible period of time. During the election process, the cooperation between the nodes is limited or even blocked. Therefore, a distinct election result within a short election period is essential. As the number of messages directly influences the required election time, it has to be reduced to a minimum.

Table 5.1: Description of the transfer conditions of the state machine (Fig. 5.4)

Transfer	Transfer Condition
T_1	*Start Big LEA-CAN message* was sent and received
T_2	Election confirmation messages of the management level received
T_3	Failure of the entire management level
T_4	Failure of single leading nodes and *Start Small LEA-CAN* message was sent and received
T_5	Election confirmation message of the co-assistant received
T_{Error}	An error has occurred

5.5 LEA-CAN: CAN-based Leader Election Algorithm for Distributed Systems

The proposed leader election strategy includes two different election states (Fig. 5.4). If the entire management level has to be elected, which occurs, normally immediately after the system start or if the NW of the entire management level drops significantly at the same time, the big election algorithm (Big LEA-CAN) is executed. If only individual leading nodes fail after the management level is initially elected, the small election algorithm (Small LEA-CAN) is performed. In the following, the two election algorithms are presented (Figs. 5.5 and 5.7).

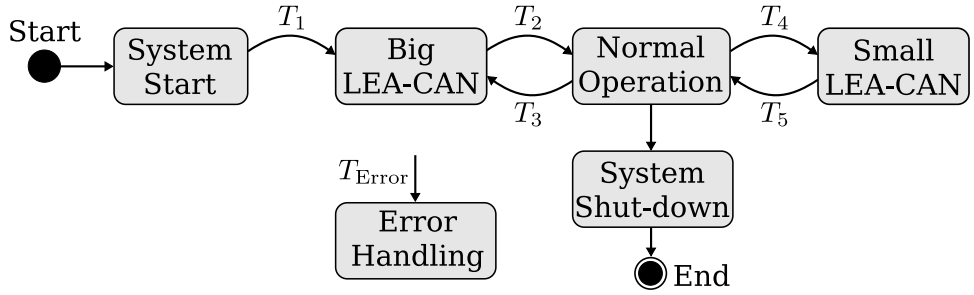


Figure 5.4: System states: After the start of the system, the entire management level is first determined in a big election process (Big LEA-CAN). Upon receipt of all election confirmation messages (one from the leader, the assistant and the co-assistant), the system switches to normal operation. If individual leading nodes fail, the shortened election process (Small LEA-CAN) is subsequently started. If an error occurs, the system switches from all operating states to the error handling state. Table 5.1 defines the transfer conditions.

5.5.1 Big LEA-CAN

Subsequently, the Big LEA-CAN algorithm is described, which (re)-elects the entire management level.

5.5.1.1 Description of the Election Process of the Big LEA-CAN

The objective of the big LEA-CAN is to elect the entire management level consisting of leader, assistant and co-assistant. All nodes of the network participate in this election and try to send their election message by receiving the *Start Election* message. The election message already contains the NW in the first 5 bits of the CAN identifier followed by the node ID. The NW value, where NW $\in \{0...10\}$, zero corresponds to the optimal state and the value ten describes the worst case value. The nodes of the management level therefore optimally all have a NW value close to zero. This value distribution has been chosen deliberately because the message identifiers are placed bit by bit on the bus when there are several CAN messages to be sent. The value zero corresponds to a dominant level and overwrites all recessive levels representing the value one. Setting the NW as part of the CAN message identifier ensures that the node with the largest NW at the time of transmission directly prevails in case of simultaneous transmission attempts. Nodes which could not prevail are then only available for assistant, co-assistant or normal operation. In case several nodes have the same NW values, the one with the smallest ID is chosen.
The structure of the big election algorithm is expressed by a state machine with eleven states (Fig. 5.5). After the election is started by the *Start Election* message, all nodes change to the *Start Election* state and generate the election messages containing their respective NW values. Each node tries to send the election message over the CAN line. Two different cases can occur:

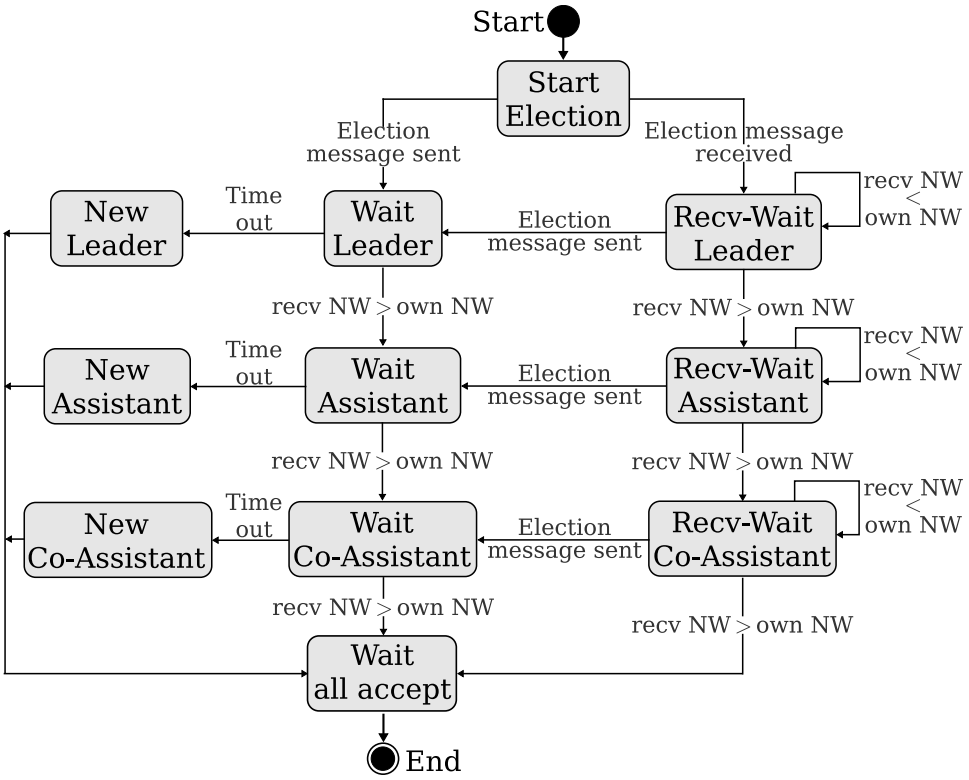


Figure 5.5: State diagram of the Big LEA-CAN to elect the entire management level consisting of leader, assistant and co-assistant.

Case 1: The election message prevails in the arbitration phase, since it has the lowest NW value at that time. The election message is sent to all participating nodes and the sender changes to the state *Wait Leader*. If the node receives messages with lower NW values, it switches to the state *Wait Assistant*. The switch can be performed

analogously up to three times. If three messages with lower NW values are received, the node switches to the state *Wait all accept* and no longer actively participates in the election.

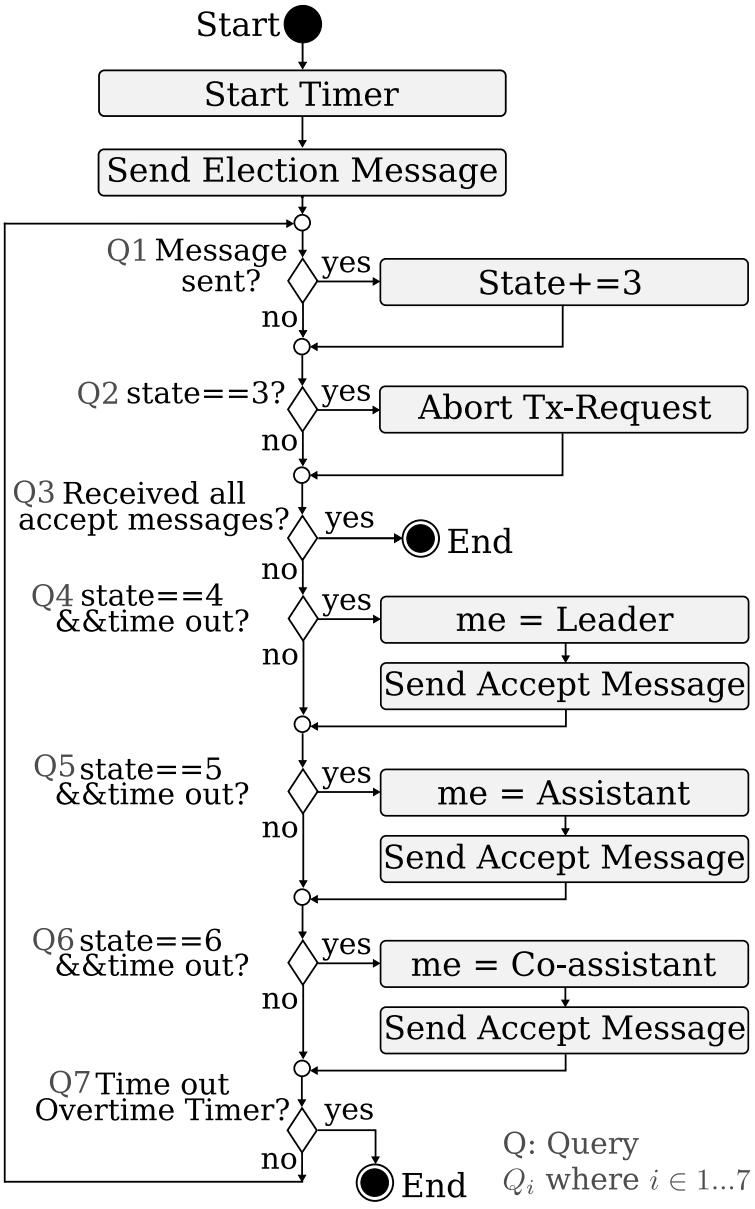


Figure 5.6: Activity Diagram of the Big LEA-CAN algorithm.

Case 2: The identifier of the node's election message is overwritten with a lower NW or node ID value during the arbitration phase and then the node switches to the receive mode. The received NW value is compared with its own. If the own NW is lower, the node remains in the current state (initially *Recv-Wait Leader*). If the own NW is larger, the node changes to the state *Recv-Wait Assistant*. The change can be performed analogously up to three times. After a node has received the third message with a better NW, it transfers to the state *Wait all accept* and it no longer actively participates in the election. It withdraws its own election message that has not yet been sent by deleting the corresponding entry in the CAN Transmit FIFO (`HAL_FDCAN_AbortTx_Request()`) and remains in receive mode.

5.5.1.2 Termination Criterion of the Big LEA-CAN

The nodes change their states according to their own and the received NW values as previously described. At the end of the election process, exactly one node each is in the *Wait Leader*, *Wait Assistant* and state *Wait Co-Assistant*. The remaining nodes are in the state *Wait all accept*.
A timer is used to terminate the election process. At the beginning of the election, the timers of each node are started and they are reset every time an election message is received. If this timer reaches a timeout, the election has been terminated for the individual node. If the election process is correct and without errors, exactly three nodes are *not* in the state *Wait all accept*. These nodes first assign themselves the status of the leader, assistant and co-assistant and then send an election acceptance message. Upon receipt of the three election acceptance messages, the big leader election is completed and the nodes switch back to the state *Normal Operation*.

5.5.1.3 Implementation of the Big LEA-CAN

For the representation of the different states a variable `state` is defined and set to the value belonging to the state. The states *Start Election* and *Recv-Wait Leader* can be combined in one state, since there is no difference between them regarding the implementation. The same applies to the states *New Leader, New Assistant, New Co-Assitant* and *Wait all accept*.

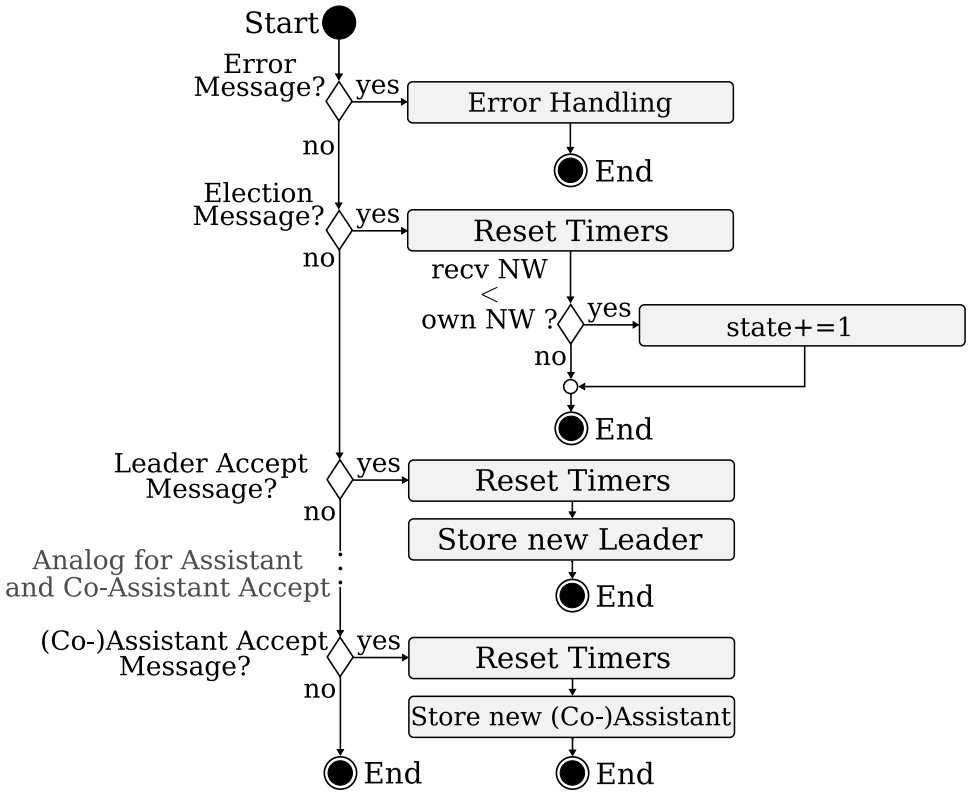


Figure 5.7: Activity Diagram of the CAN handler used for the Big LEA-CAN algorithm.

The process of the large election is shown in the activity diagrams (Figs. 5.6 and 5.7). First, the election timer is started, which, when expired, signals the end of the election process. The period time t_e must be greater than the transmission time of a

message and is defined as follows:

$$t_e = t_m \cdot (1 + 5\%) + t_p$$

where t_m is the maximum message transmission time defined in Table 5.4 and t_p is the time required to receive and process a message. The maximum processing times were determined in a previous work [303]. For CAN messages, it is 3.3 µs and 7.8 µs for CAN FD messages, each using the maximum number of user data bytes.
In addition to this, a second timer, the *Overtime* timer, is activated in all participating nodes. This timer specifies the maximum time within the election is allowed to be in standstill. If no new relevant election messages are sent and still no new management level is determined, the timeout of the *Overtime* timer ends the election prematurely. In this case, the affected node signals this with an *Abort* message.
After the start of these two timers the election message is generated and put into the transmission FIFO of the CAN transceiver. The start of the election process is completed and the states of the election are queried cyclically in an infinite loop.

Description of the Queries (Q)

Query 1 (Q1) checks whether the election message has already been sent. If this is the case, the state variable is incremented by three and the query checking whether the message has been sent is disabled. Incrementing the state variable skips the states in which the node is waiting to send its message and jumps directly to the appropriate management level wait state. For example, if a node is in the *Recv-Wait Assistant* state when its message is sent, it switches directly to the *Wait Assistant* state.
In *Query 2 (Q2)* the state variable is checked for equality with the value three. If it is equal and the message has not yet been sent, a position in the management level for the node is excluded and the election message is removed from the transmit FIFO.
Query 3 (Q3) implements the completion criterion. Once a node has received all three *Accept* messages, the management level is fully determined and the election is successfully completed. Consequently, the node exits the infinite loop and returns to the normal operation state.
The *Queries 4-6 (Q4-6)* are necessary for the assignment of the leading roles. If a node itself belongs to the new management level, it recognizes this by the fact that it is still in state four, five or six even after the election timer has expired. In this case it assigns itself the appropriate role and sends an *Accept* message.
When receiving election relevant messages the CAN handler first resets the timers and then checks if the state variable has to be changed. This is the case if the received NW is lower than the own one. When receiving an election acceptance message, for example the *Leader Accept* message, both timers are reset. The node ID of the sender is searched in the subscriber list. If a list element exists, the leader pointer is set to the corresponding address. The same process is performed for an *Assistant Accept* and a *Co-Assistant Accept* message.

5.5.2 Small LEA-CAN

In the following, the Small LEA-CAN algorithm is described, which is used in case of failure or deactivation of individual managing nodes.

5.5.2.1 Description of the Election Process of the Small LEA-CAN

If one of the leading nodes fails or if the NW value falls below the threshold value during operation, the objective is to quickly replace the gap in the management level by executing the abbreviated Small LEA-CAN election algorithm. Here, in case of failure of the leader (i) in Fig. 5.8) or the assistant (ii) in Fig. 5.8), the positions are quickly filled by moving up the management positions of the corresponding nodes (Fig. 5.8). Only the co-assistant is re-elected.
At the start of the shortened election process a *Start Election* message is sent (Fig. 5.9) and all nodes change to the Small LEA-CAN state. The special feature here is that the node, which sends the *Start Election* message makes directly a candidate proposal by writing the node ID of the proposed co-assistant in the data field.
The remaining nodes receive the message and evaluate the election proposal. The prerequisite for using the Small LEA-CAN algorithm is that all nodes have a complete and updated list of the participants and their parameters. Therefore, the abbreviated election algorithm is not used after system startup.
Upon receiving the *Start Election* message containing the candidate's ID, two cases can occur:
Case 1: The node accepts the proposal. The prerequisite for this is that it would either propose the same candidate or that the NW value of the candidate is lower than the one of its own proposal. If all nodes agree with the candidate, they send no further message and wait for the end of the election process in the *Finished and Ready* state.
Case 2: The proposal is rejected and the node sends a reject message proposing a new candidate. It then switches to the *Wait Reject* state. As soon as three or more nodes vote against the current candidate, it is rejected and the next candidate is elected. This process is repeated until a candidate is elected that is approved by the majority.

5.5.2.2 Termination Criterion of the Small LEA-CAN

Analogous to the Big LEA-CAN, the election and overtime timer are also used here, which are restarted with the receipt of election-relevant messages. The election process is considered to be finished as soon as the timer has expired. The nodes switch to the *Wait accept* state and wait for the election acceptance message from the candidate. When this is received, the election process is finished and all nodes switch back to the normal operation state.

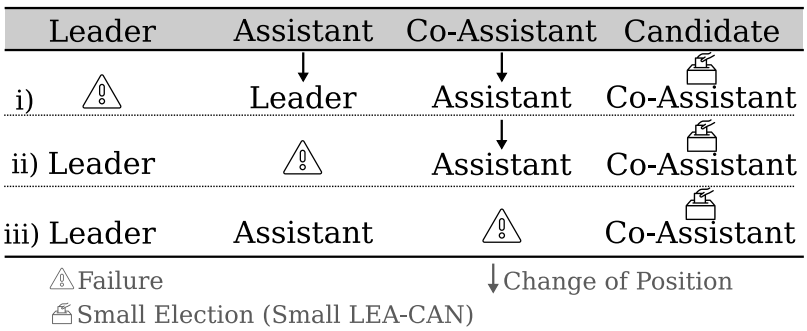


Figure 5.8: In case of the failure of single leading nodes, the management level is quickly reoccupied by position changes, i.e. by moving up, and the abbreviated election process.

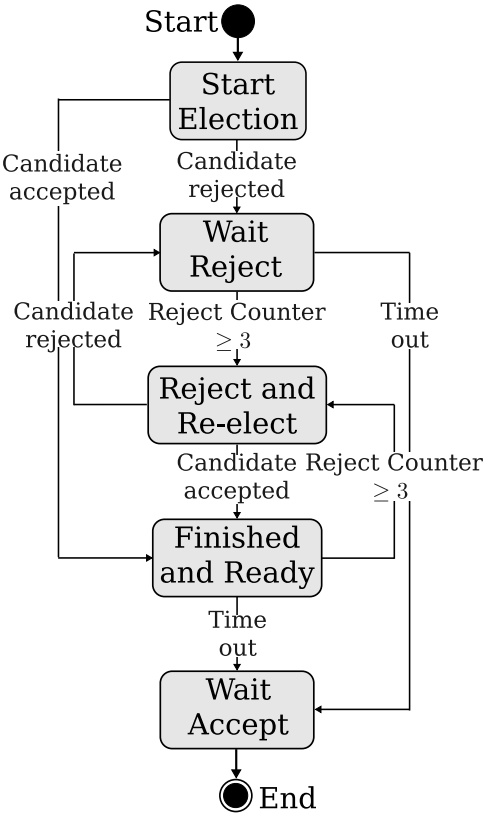


Figure 5.9: State diagram of the Small LEA-CAN to elect the co-assistant.

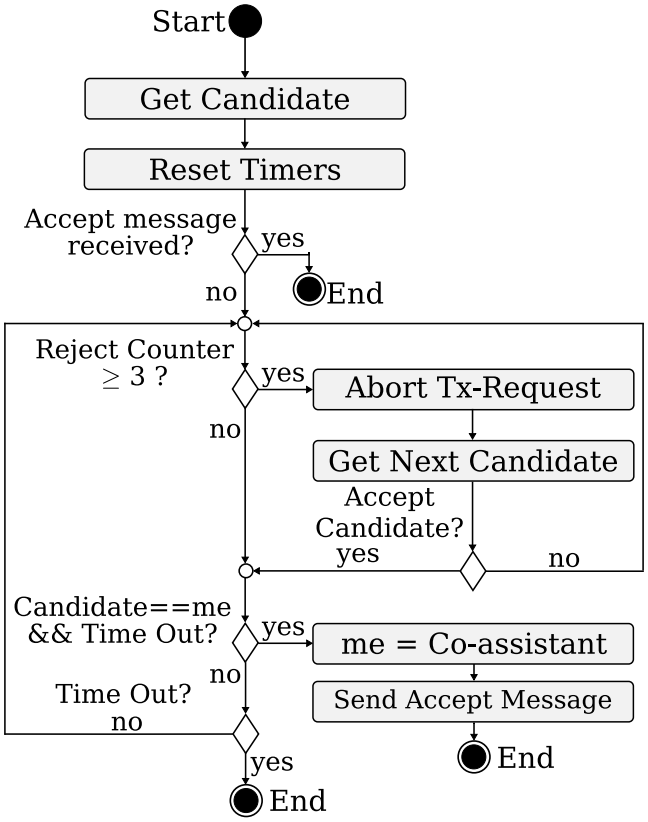


Figure 5.10: Activity diagram of the small LEA-CAN algorithm.

5.5.2.3 Implementation

Upon the receipt of the *Start Election* message is received, the two timers are started and the candidate proposal is evaluated in the CAN handler. The acceptance criterion

is that the proposed candidate is equal to the own proposal or the NW of the proposed candidate is lower than the one of the own proposal. Comparing the NW values, a tolerance of $\pm 5\%$ is included. This avoids multiple selections due to measurement tolerances and prevents delaying or avoiding the main functionality of the election of the co-assistant as fast as possible to restore the normal operation.

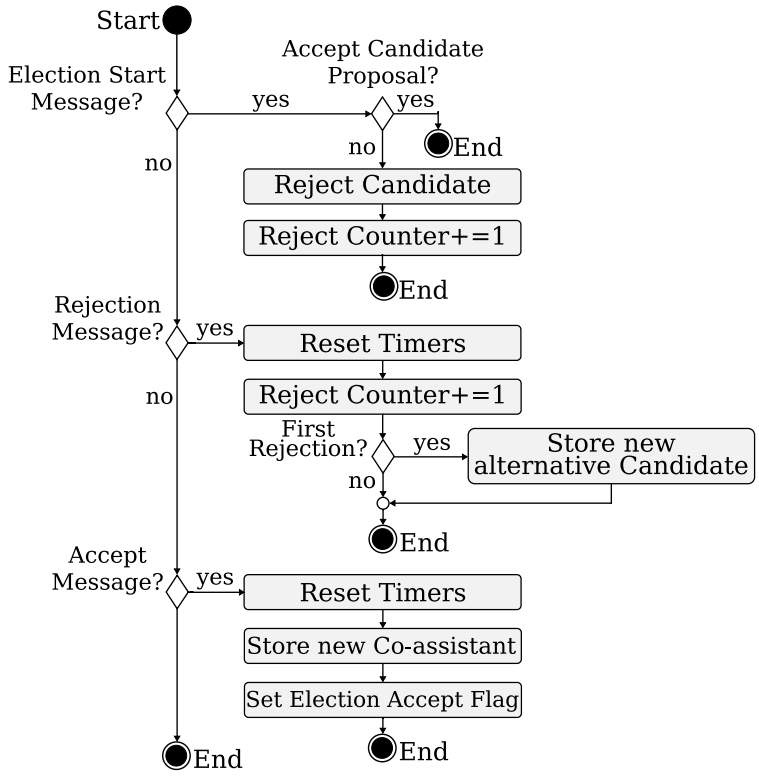


Figure 5.11: Activity diagram of the CAN handler used for the small LEA-CAN algorithm.

If the candidate is rejected, the *reject candidate* flag is set and the reject counter is incremented in the CAN interrupt handler. Furthermore, the timers are reset and the node ID and NW of the potential new candidate specified in the data field of the rejection message is stored. Back in thread mode, the first check is whether an accept message has arrived. If this is the case, the small algorithm is considered as successfully completed and it is switched back to the normal operation state. Otherwise, the next step is to check whether at least three nodes have already rejected the current candidate and the reject counter has at least the value three. If this is the case, the next candidate whose node ID is in the data field of the first received reject message is evaluated. This process is repeated until one of the candidates receives less than three rejections. This candidate is then considered to be generally accepted and the election process is finished. Finally, the nodes wait for the *Accept* message from the candidate. The candidate assigns itself the co-assistant status after the first timer expires and sends an *Accept* message. The remaining nodes search for the candidate's node ID in their participant list and assign the pointer to the list element according the node ID of the newly elected co-assistant. The small election algorithm is successfully completed and all nodes switch back to the normal operation mode.

5.6 Election Messages

To achieve the lowest possible number of required messages and thus a minimum required election time, the arbitration of the CAN (FD) communication is employed reasonably. In addition, the election messages only contain the CAN identifier.

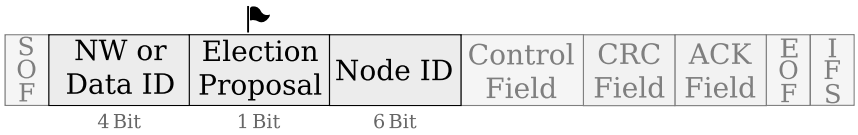


Figure 5.12: Structure and format of the election messages using the 11 bit identifier of the CAN (FD) message protocol. Further detailing of the message format shown in figure 5.3.

The data field remains empty and the transmission time of the messages is reduced. The priority ID (Fi. 5.3) is further subdivided into a 4 bit field for the description of the content or the indication of the node weight and into an Election Proposal (EP) flag, which is set if the corresponding message contains an election proposal (Fig. 5.12). Separate messages are defined for each of the system states *Normal Operation, Big LEA-CAN* and *Small LEA-CAN*. The election messages are defined for an 11 bit identifier in Tab. 5.2, whereas the use of the message format containing a 29 bit identifier is analogous and increases the number of usable nodes.

Table 5.2: Composition of the priority identifiers of the election messages for the Big and Small LEA-CAN

LEA		Message	Data ID or NW	EP Flag
Big LEA-CAN	Small LEA-CAN	Election Message	NW	1
		Error	0x0	0
		Abort	0x1	0
		Co-Assistant Accept	0x4	0
		Co-Assistant Reject	0xC	0
		Leader Accept	0x2	0
		Assistant Accept	0x3	0
		Leader Reject	0xA	0
		Assistant Reject	0xB	0

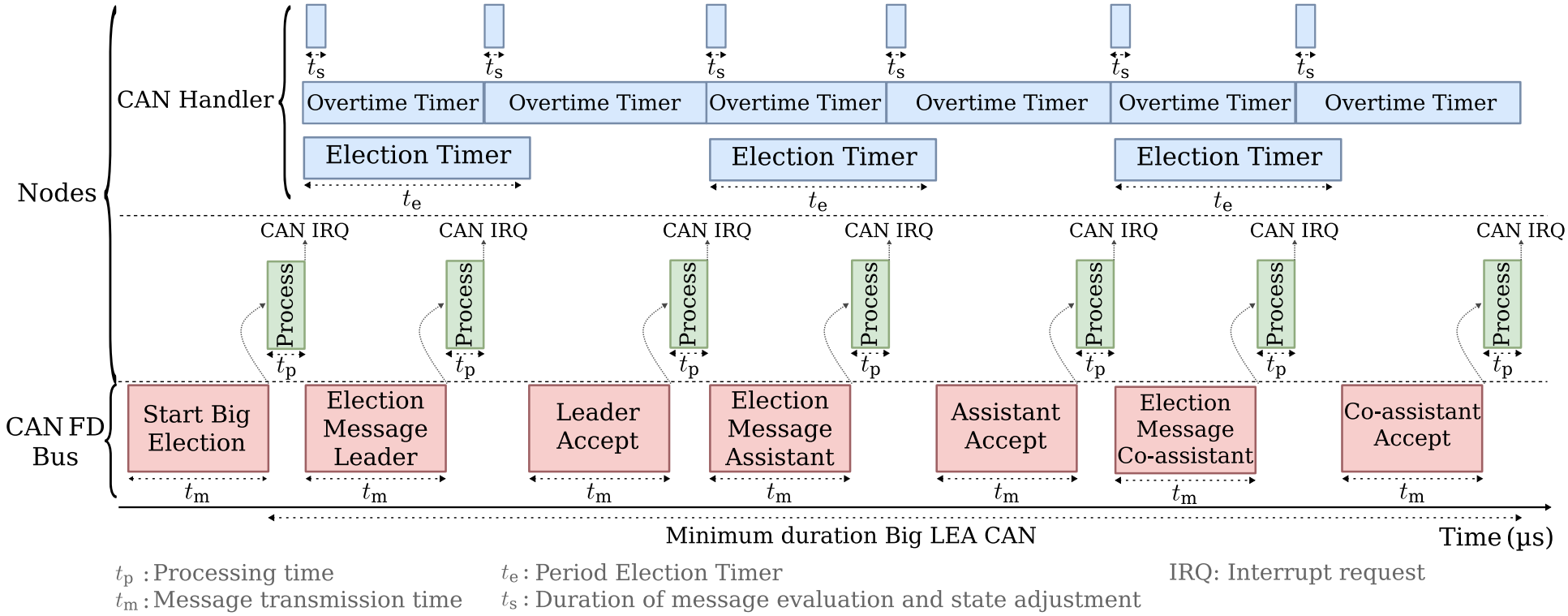


Figure 5.13: Minimal message effort and duration of the Big LEA-CAN. Details regarding the process steps of the nodes in the CAN handler are given in the figures 5.7 and 5.14.

5.7 Time Complexity and Scalability Analysis

The time complexity of the LEAs in the proposed system depends on the number of exchanged messages needed to elect the management level or the co-assistant.
In the best case, two messages are exchanged within the Small LEA-CAN algorithm (Fig. 5.15) and a total of 7 messages are exchanged within the Big LEA-CAN (Fig. 5.13). The message transmission time depends on the number of stuffing bits (Tab. 5.3), the applied CAN message format and the selected transmission rate (Tab. 5.4). Furthermore, the election duration is influenced by the processing times and the reload value of the election timer, which is required to ensure that the nodes can use their veto right if an unsuitable node has prevailed in the arbitration.
For the minimum duration of the Big LEA-CAN t_{BLmin} the following results:

$$t_{\mathrm{BLmin}} = (2 \cdot t_{\mathrm{p}} + t_{\mathrm{m}} + t_{\mathrm{e}}) \cdot n \tag{5.2}$$

The following applies for the duration of the Small LEA-CAN t_{SLmin}:

$$t_{\mathrm{SLmin}} = t_{\mathrm{m}} + t_{\mathrm{p}} + t_{\mathrm{e}}, \tag{5.3}$$

where t_{m} is the message transmission time (Tab. 5.4), t_{p} is the processing time, t_{e} is the period of the election timer and n is the number of leading nodes to be elected.

Exemplary Calculation for the Minimum Duration of the Leader Election

In the following, the minimum durations of the two election processes are calculated exemplarily. The processing time for packing the CAN FD messages refers to an ARM Cortex-M4 processor [304]. For the communication CAN FD is used with a normal transmission rate of 1 Mbps and an increased rate of 4 Mbps. Furthermore, the following consideration takes into account the maximum possible number of stuffing bits.
The minimum duration of to the Big LEA-CAN process t_{BLmin} under specified conditions without considering the *Start Big LEA-CAN message* is:

$$\begin{aligned} t_{\mathrm{p}} &= 7.8\,\mu s \\ t_{\mathrm{m}} &= 40\,\mu s \\ t_{\mathrm{e}} &= t_{\mathrm{m}} \cdot (+5\%) + t_{\mathrm{p}} = 49.8\,\mu s \approx 50\,\mu s \\ t_{\mathrm{BLmin}} &= (2 \cdot 7.8\,\mu s + 50\,\mu s + 40\,\mu s) \cdot 3 = 316.8\,\mu s \approx 320\,\mu s \end{aligned} \tag{5.4}$$

Thereby the entire management level was elected.
The minimum duration of to the Small LEA-CAN process t_{SLmin} follows as:

$$\begin{aligned} t_{\mathrm{p}} &= 7.8\,\mu s \\ t_{\mathrm{m}} &= 40\,\mu s \\ t_{\mathrm{e}} &= t_{\mathrm{m}} \cdot (+5\%) + t_{\mathrm{p}} = 49.8\,\mu s \approx 50\,\mu s \\ t_{\mathrm{SLmin}} &= (7.8\,\mu s + 40\,\mu s + 50\,\mu s) = 97.6\,\mu s \approx 100\,\mu s \end{aligned} \tag{5.5}$$

The duration of the Small LEA-CAN process t_{SLmin} takes less than one third of the time required for the Big LEA-CAN process t_{BLmin} . This clearly shows that the

deployment of the Small LEA-CAN process significantly improves system availability by reducing downtimes associated with an ongoing election process.

Table 5.3: Minimal and maximal message length of an election message with zero user data bytes in bit considering the maximum number of stuff bits

Length in Bit	CAN 11 Bit ID	CAN 29 Bit ID	CAN FD 11 Bit ID	CAN FD 29 Bit ID
Minimal	47	67	60	79
Maximal	55	80	64	88

Table 5.4: Transmission duration of CAN and CAN FD messages with 11 or 29 bit identifier at different transmission rates

Transmission Rate	CAN 11 Bit ID	CAN 29 Bit ID	CAN FD 11 Bit ID	CAN 29 Bit ID
in MBps	Transmission duration in µs			
0.5	94 - 110	134 - 160	120 - 128	158 - 176
1	47 - 55	67 - 80	60 - 64	79 - 88
1 BRS: 4	/	/	36.75 - 40	55.75 - 64
1 BRS: 8	/	/	32.875 - 36	51.875 - 60

BRS: Bit rate switching

The election duration of both algorithms is *independent* of the number of nodes and remains constant as the number of nodes increases. However, with an increasing number of nodes, the probability increases that the election message of an inappropriate node erroneously prevails during the arbitration phase.

5.8 Error Handling

In order to safeguard the program execution in the error case, error handling is implemented as a reaction to 17 different error types. Furthermore, three different error counters are defined in addition to the error counter of the CAN controllers. One error counter for the UART communication, one for the timers and one for the election algorithms. If an error occurs, first the severity is evaluated and depending on this the error counter is increased. The UART error counter follows the procedure of the CAN error counter: If the UART error counter reaches the value 100, the corresponding node can only receive messages. If reception errors occur repeatedly and the error counter value reaches 255, the UART is deactivated. While the error counters for the timers and the UART communication are administered only locally, the election error counter is part of the participant list. Each node thus has information about its own election error counter and the ones of the remaining nodes. This allows the leader to precisely monitor the error behaviour of individual nodes and to react to it. For example, it can exclude a participant from the election process if the error counter reaches a certain threshold value.

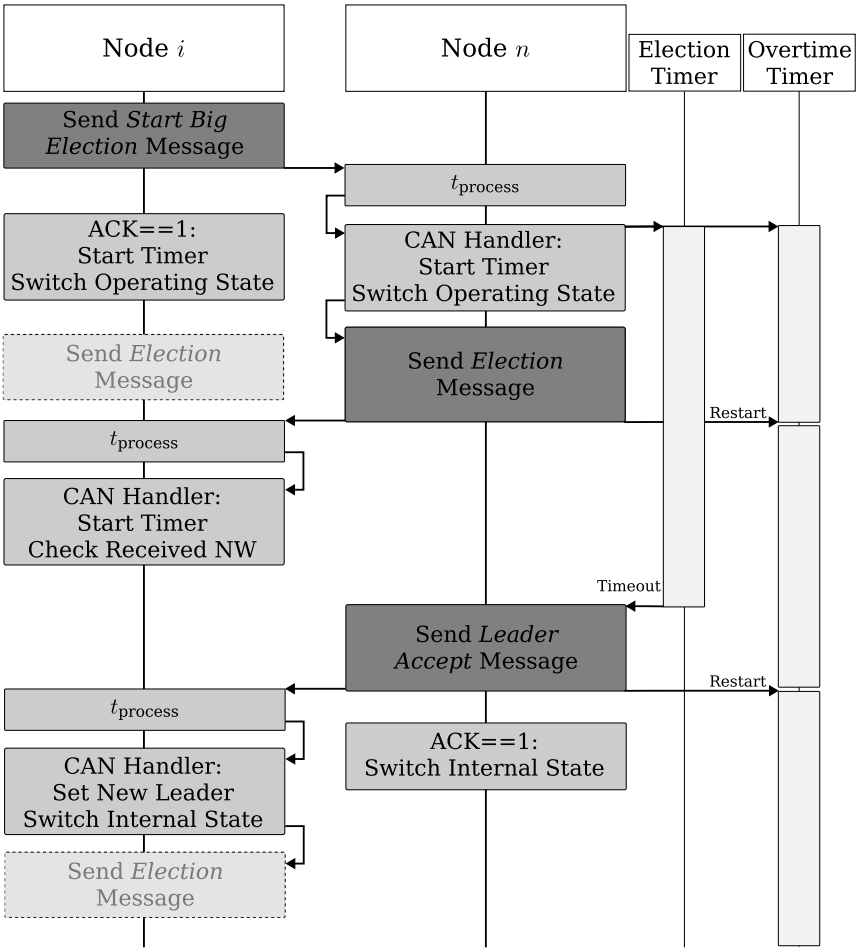


Figure 5.14: Sequence diagram for a simplified description of the leader election in the Big LEA-CAN between two nodes. Note: Each node has election and overtime timers, though they are shown here only for Node *n*.

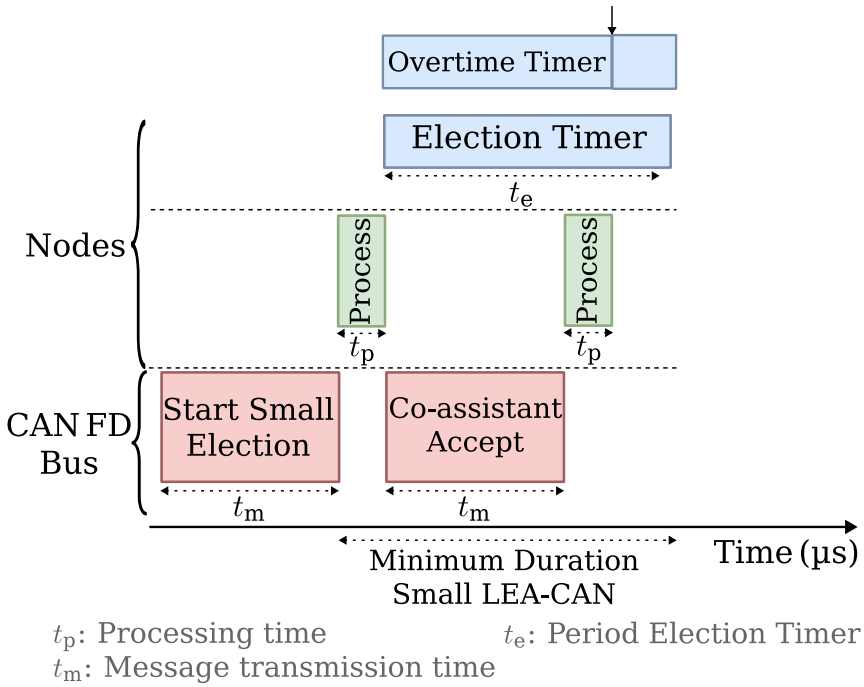


Figure 5.15: Minimal message effort and duration of the Small LEA-CAN.

Table 5.5: Selection of the defined errors: Description of their occurrence and handling

Error	Occurrence	Error Handling
mainFSM error	undefined state in main state machine	reset of main state machine
system clock error	erroneous initialization of the system clock	node remains in error state
malloc error	erroneous memory reservation using malloc	node remains in error state
UART transmit/receive error	erroneous UART communication, e.g. bitflips or varying parity bits	increase UART error counter
timer error	incorrect initialization or faulty start of (one of) the two election timers	increase timer error counter and cancel election process
election error message	reception of an error message via CAN	increase of the election error counter of the node specified in the error message
election status error	call of the Big LEA-CAN election function using a state variable unequal to the value zero	increase of the election error counter, send an error message and remove respective node from the election process
big election out of bound	invalid value of the state variable	increase of the election error counter, send an error message and remove respective node from the election process
election accept error	incorrect *Accept* message	increase the election error counter of the sending node, send an error message, abort the election process (Big LEA-CAN) or election reattempt (Small LEA-CAN)

5.9 Hardware Test Setup

Both election algorithms were tested in a hardware test setup consisting of five microcontrollers (Fig. 5.16, Fig. 5.17). The microcontrollers have a CAN FD plug-on board with a terminating resistor that can be switched via the microcontroller for a reconfigurable, expandable CAN system. Furthermore all microcontrollers are connected to a PC via USB for test purposes. For message monitoring a USB2CAN

adapter is used, which can also be connected to the PC via USB and allows messages to be sent to and received from the CAN FD bus.
For the communication between the participants the CAN 2.0 A was used and a transmission rate of 500 kbps was chosen.

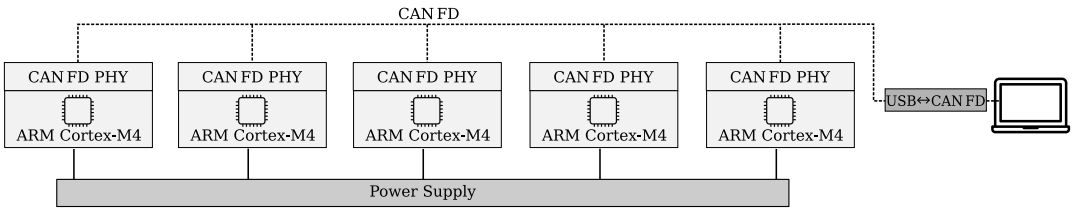


Figure 5.16: The hardware test setup consists of five ARM Cortex M4-based microcontrollers [304], with customized CAN FD interface, a USB-to-CAN adapter [305] and a test PC. All messages are logged on the test PC and it is also possible to start election processes by sending respective messages from the PC. Figure 5.17 shows the hardware implementation

Figure 5.17: Hardware test setup consisting of five nodes, which consist of a custom CAN-FD-PHY-board and an ARM-Cortex-M4 based microcontroller [304]

Message Logging

In order to log the messages of an election process and thus determine the message overhead, a logging functionality was included. For this, priority ID, node ID and the data of a message are stored in a list. Each time a message associated with the election arrives, a list element is added in the CAN interrupt handler. At the end of the election process, the list is cleared again to prevent memory overflow. This functionality can be switched on or off via a definition and is switched off by default.

Implementation of a Serial Connection to the Test PC

For test purposes a serial connection between a node (UART) and the test PC (USB) was implemented. With the help of a terminal program that supports a serial interface (e.g. HTerm), new test data can be transmitted to the node. This extension can be activated or deactivated by a definition.

5.10 Summary

This chapter presented a method for selecting a leader for a scalable, reconfigurable CAN bus-based system. The concept of management levels was introduced to reduce

the error rate and improve system availability. An election algorithm based on dynamic criteria is used to ensure the performance and adequacy of the temporary leader. In addition, the CAN message format used exploits arbitration to reduce the message and hence time requirements of the election algorithm. The presented leader election algorithm has a message and time complexity of $\mathcal{O}(1)$ in the range of the number of participants supported by common bus systems (CAN, CAN FD). Both algorithms were tested in a hardware test setup. In future work, error management will be further extended and cases such as erroneous leader appointment, deselection and deactivation rights will be added. Furthermore, the task and rights assignment of the management level will be further detailed.

6 Operation and Control Strategies

Battery systems are used in a wide range of safety-relevant applications, such as electric vehicles, unmanned aerial vehicles and home storage systems. Safety, reliability and avail ability of the battery system therefore play a key role. In addition, the useful service lifetime of the batteries determines the environmental impact and economic efficiency of the overall system. One possible solution is to give batteries a second life in applications with lower requirements in terms of dynamic behavior or capacity. Heterogeneous battery systems consist of batteries with differences in cell technology, age, capacity, and optimal operating range. To meet the safety, reliability, and availability requirements a scalable, Decentralized Battery Management System (DBMS) based on a distributed control system is proposed. Batteries, generators, and loads have Local Control Units (LCUs) consisting of a microcontroller, a measurement unit, and a DC-DC converter with adjustable voltage and current limits. These LCUs are the basis for the communication-based, cooperative system control and enhance the reliability and scalability of the battery system compared to conventional centralized structures. They record and manage the operating parameters and provide the basis for predictive energy management and battery residual value estimation. As a fallback strategy, a droop-based control of the DC-DC converters is used in addition to the communication-based one. Transition conditions between the control modes are defined and the control methods are compared and differentiated. The performance and the resulting benefits of batteries are determined by the control strategies. In this chapter, the requirements for the control strategies for different operating modes, including startup, severe fluctuations of the DC power line voltage, and safe shutdown, are analyzed.

6.1 Motivation

The reduction of fossil energy sources and the integration of renewable energy sources is indispensable in order to reduce the emissions and thus to limit the consequences of the climate crisis in the face of a globally increasing energy demand. The intermittent nature of renewable energy sources and the time difference between energy supply

and demand poses a significant challenge. Battery systems offer the possibility to compensate fluctuations and to supply new load types, such as electric vehicles or unmanned aerial vehicles (Fig. 6.1).

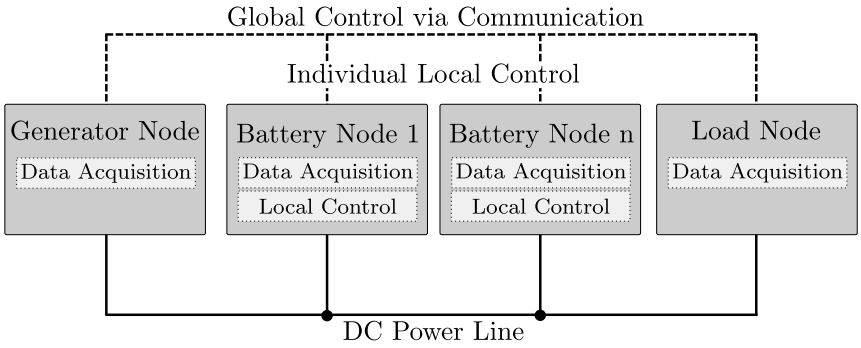


Figure 6.1: Decentralized Battery Management (DBMS) system architecture consisting of battery, generator and load nodes. The control is distributed in a local and global level.

Thereby, the service life of the battery system is a key factor regarding the environmental impact and the economic efficiency. Optimal operation of batteries and resource-efficient use of second-life batteries extend the life cycle and thus improve the sustainability [306]. While recycling of raw materials or remanufacturing have been considered as solutions, simply reuse of the battery packs offers tremendous cost benefits [307, 308]. Heterogeneous battery systems combine batteries with differences in cell chemistry, nominal capacity, State of Health (SoH), State of Charge (SoC) and age. Integrating new batteries in combination with used batteries, that have been only slightly modified to avoid further development costs, is a challenge [309, 310]. A battery state dependent load distribution is necessary for the safe operation of a heterogeneous battery system [311–313].
Furthermore, battery systems are installed in an increasing number of safety-relevant applications such as in electric vehicles, backup power or home energy storage systems. Therefore, the availability and the reliability of the battery system are relevant factors. Availability describes the ontime and usability of the battery system in different operating states such as start-up or maintenance. Reliability is defined in this context as ensuring availability of the battery system and fault-free operation even in the case of failure of single components.
Another challenge is to ensure robustness, which is defined as stability in the presence of disturbances, i.e. correct operation in the event of transients, sensor drifts or abrupt load changes.
Flexibility and scalability are further requirements to ensure that the battery system can be used for a variety of different applications. Scalability refers to a variable number of components that can change even after initial implementation. Flexibility describes the possibility to combine any battery types and to integrate different loads and energy generators.
Appropriate control strategies are required to meet the above objectives in a heterogeneous battery system [314]. The main objectives of the control include maintaining the DC power line voltage V_{DC} at a predefined target value and the energy sharing between the parallel connected components (Figs. 6.1, 6.4). The use of several components and thus multiple DC-DC converters increases the difficulty of observability and controllability.

In the following sections, a theoretical analysis of a multi-level collaborative control strategies for a decentralized, heterogeneous battery system is presented (Fig. 6.1). First, existing control strategies in battery systems are considered. Next, the system for which the control strategies are observed, is proposed. The tasks and objectives of the control are described and the control of the overall system is divided into different levels. Different control strategies for the individual levels as well as their advantages and limitations are discussed. Subsequently, transition conditions between the individual control strategies are defined. Finally, the presented control strategies are compared with existing ones and an outlook on future research is given.

6.2 Related Work

The integration of different renewable energy sources such as photovoltaic or wind in combination with variable loads and different energy storage devices like super capacitors, fuel cells and batteries complicates the control of the common DC power line voltage (Fig. 6.1) as well as the energy sharing between the components. Various control techniques, such as centralized, decentralized, distributed, and hierarchical ones (Fig. 6.2), are proposed to ensure safe and reliable operation (Fig. 6.3) [315].

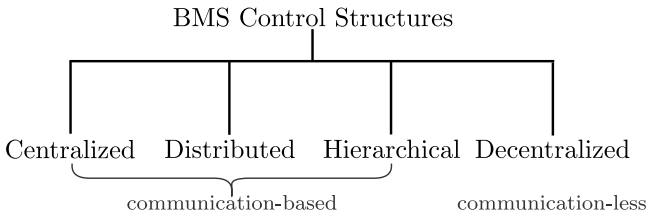


Figure 6.2: Centralized, distributed, and hierarchical control strategies require global communication between nodes, while decentralized control operates communication-less.

6.2.1 Centralized Control Strategies

In centralized control strategies, data are sent from multiple, distributed, subordinate units to the central controller over the communication links. The total generation, loads and other operational information such as (SoC) of the batteries are processed in the central control unit and corresponding signals are sent back. The central unit is functionally different from the subordinate ones [316]. This technique has better observability and controllability. Nevertheless it has lower reliability due to the single point of failure and the fixed defined number of inputs to the central control unit is associated with lower flexibility and scalability.

6.2.2 Decentralized Control Strategies

Decentralized control strategies are introduced to avoid the single-point failure. The DC-DC converters are adjusted by local controllers, where locally measured signals are the inputs [317]. Droop control is often used, where a virtual droop resistance is used for the battery and a virtual droop capacitance for the supercapacitor [318].
The determination of the droop settings is a challenging task, since current sharing, accuracy and system stability are strongly dependent on the droop settings. Deviations resulting from variations in the measurement resistors are a challenge for the

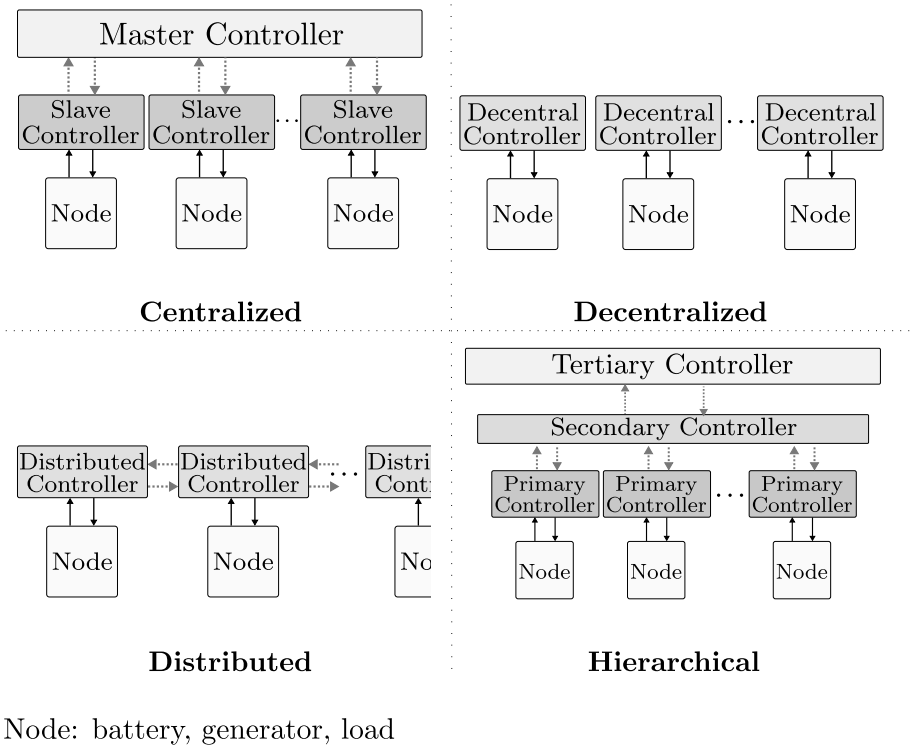


Figure 6.3: Existing control strategies can be categorized in centralized, decentralized, distributed and hierarchical ones. Common strategies mainly consider battery nodes in the control, while it is also possible to consider load and generation nodes.

determination of the controller output values [319]. Furthermore, the conventional droop control is problematic at low DC power line voltages in the case of increased output current. For instance, higher droop settings result in a more damped system and improved current sharing accuracy. However, the higher value of droop parameter leads to increased permanent DC voltage deviation on the DC power line. [320, 321]

6.2.3 Distributed Control Strategies

The advantages of centralized and decentralized control are combined in distributed control, where only neighboring units communicate [229, 322]. Each DC-DC converter is still steered by a local controller, but the local units additionally exchange information, e.g., the locally measured DC power line voltage, with neighbouring units. The DC power line voltage can be measured differently (Fig. 3.7), but should be equal in terms of magnitude, taking into account small, permissible measurement errors. The communication between the nodes is helpful to detect defective sensors and deviations.

6.2.4 Hierarchical Control Strategies

In hierarchical strategies, the control is divided into three levels consisting of primary, secondary and tertiary control [323–326]. The primary controller operates locally and has the shortest response time. It uses locally measured signals to influence the DC power line voltage and is also responsible for energy sharing at the lower level. The secondary controller has higher response times compared to the primary controller and compensates for the voltage deviation caused or left by the primary controller. Furthermore, it attempts to achieve power balance between the primary

controllers with a suitable energy sharing strategy. The secondary controller is needed to compensate for the limits of the primary controller. In particular, the performance of the primary controller is not satisfactory when the line resistance is large. Furthermore, in the case of droop control at the primary level, for example, the permanent control deviation can be compensated. The tertiary controller is the top level controller with the slowest response. It is responsible for maintaining optimal operation, for example, in terms of efficiency with multiple units.

6.2.5 Comparison of Existing BMS Control Architectures in Terms of Reliability, Scalability and Control Quality

In master-slave architecture, the defect of the master board leads to the complete failure of the battery system. The absence of individual slave boards can also lead to safety-critical states, depending on the state of the battery (cell) and whether it can be disconnected from the rest of the system. The control tasks are clearly assigned and the unambiguous specifications of the master based on a uniform database promote control stability.
The decentralized architecture also ensures operation of the battery system in the event of single or multiple failed controller boards, but the communicationless concept based on local measurements has drawbacks in terms of control accuracy.
Using distributed control strategies, the failure of single or multiple controllers also does not endanger operation, but the point-to-point communication is interrupted. This can lead to limitations in control accuracy and stability.
With hierarchical control strategies, it depends on which controller type fails. A functioning battery system is possible even if several primary controllers fail. If a failure of the secondary or tertiary controller occurs, the primary controllers do not receive system information and load sharing specifications. The primary controllers can still be used for a short term, e.g., for an emergency stop. The communication between the controllers in the distributed and hierarchical control strategy enhances the data basis for the control decisions and improves the control stability.

6.2.6 Adaptation Capabilities of Control Architectures

The selection of a control strategies leads to a trade-off between reliability and control quality.
Existing systems use a single control strategy throughout the entire operation. In the following, control strategies for the DBMS are presented. In contrast to existing systems, the DBMS provides the ability to switch between different control strategies depending on the operating state. With the chosen hardware setup, it is possible to implement centralized, decentralized, distributed, and hierarchical control strategies (Fig. 6.3), as well as mixed forms thereof. Switching between control strategies is software-based and does not require any hardware changes.
In the following, different global and local control strategies are designed. Their advantages and limitations are discussed and they are assigned to operating states. Transfer conditions are defined and the advantages of mixed control strategies are analyzed.

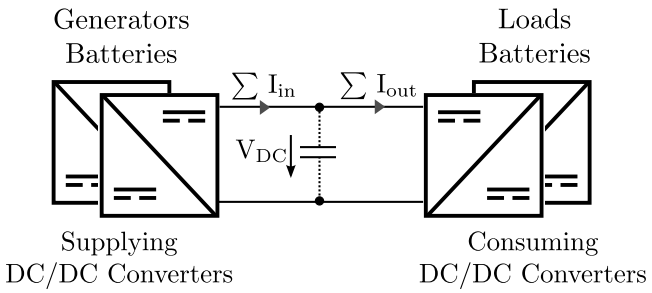


Figure 6.4: Simplified representation of the main control objective. The main control objective is to maintain the DC power line voltage at a certain predefined setpoint for a given load and generation by controlling the battery currents. Batteries can supply missing energy (discharging, positive currents) or absorb excessive one (charging, negative currents).

6.3 Control Objectives, Optimizations and Distribution to Separate Control Levels

The main control objective of the DBMS is to maintain the DC power line voltage V_{DC} at a fixed defined setpoint (Fig. 6.4).
An additional constraint is, that the batteries must be operated within their safe operating areas (SOA). The maximum permissible charging or discharging power depends, among other things, on the SoC, the operating temperature, the Open Collector Voltage (OCV) and the internal resistance of the battery. DC-DC converters connected to the batteries limit the output and input power according to the specifications. If there is enough charging and discharging capacity, various optimizations are taken into account in the control strategies of the DBMS in addition to the control objective under the aforementioned constraints (Fig. 6.5).

6.3.1 Optimization Scenarios

In the following, possible optimization scenarios are described.

6.3.1.1 Optimal Battery Operation

Optimal battery operation and the resulting improved safety and service life time is one optimization goal. Various battery technologies result in different optimal operating ranges. For parallel connected batteries, the load current is distributed depending on SoC, remaining nominal capacity, operating temperature and optimal operating range. Furthermore, regarding the battery type and the operating condition, low (dis)charge currents, recovery time, i.e. rest periods between charge and discharge processes, or pulsed (dis)charge can have positive effects on battery aging and safe operation [327–331]. The issue of battery-optimal load current sharing is a separate one and is not considered in more detail in this chapter. Only the control strategy optimal battery operation is considered. It has priority even at the expense of system efficiency and also partial shutdowns of the loads can be considered.

6.3.1.2 Maximum Efficiency

Alternatively, the system can be optimized for maximum efficiency. The focus here is primarily on the optimum efficiency range of the DC-DC converters. At low power ranges, switching losses lead to an overall low efficiency of the DC-DC converter [332]. As a result, when pursuing the optimization goal of maximum efficiency at low consumption powers, individual battery nodes can be completely deactivated. Consequently, the remaining battery nodes deliver higher output powers and their DC-DC converters operate in a higher efficiency range. In addition, supercapacitors can be integrated for balancing low load and generation peaks. They exhibit high efficiencies at low energy density.

6.3.1.3 Long Operation Duration

Another optimization goal is system availability over the longest possible operating time, e.g. range optimization, supply of mobile applications or stand-alone grids. The intention in this case is to maximize the operating time and to safely supply the consumer at least partially for as long as possible. The approach is that in such scenarios, the batteries also operate outside their optimal operating range. System efficiency with temporary deactivation of individual battery nodes to optimize overall efficiency remains a focus, as does partial shutdown of loads.

6.3.1.4 Ensured Supply of the Loads

Ensuring the load supply even when the batteries leave their optimal range or the DC-DC converters operate outside their maximum system efficiency ranges is a further optimization goal. Use cases include emergency stop in vehicles, safe landing of an unmanned aerial vehicle or placing an emergency call on a mobile phone.

6.3.1.5 High System Availability

Besides the control objective and the optimization strategies, the higher-level system objectives of robustness, reliability, scalability, flexibility and availability also have to be considered (Fig. 6.5).
In order to meet the requirements, different distributed and hierarchical control strategies are presented, among which switching takes place depending on the operating state. For a defined separation of tasks and a specified assignment of responsibilities, the system control is divided into two levels: a global and a local control level.

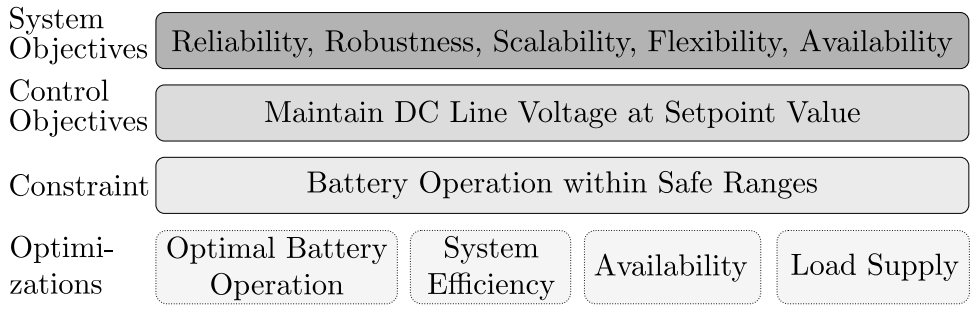


Figure 6.5: The system objectives, the control objective, and the constraints mandatorily affect each control strategy, while the optimizations are optionally considered.

6.4 Global Control Level Strategies

The global control layer is responsible for system-level control decisions. Its tasks include the decision on the applied global and local control states as well as the verification of the transition conditions between them and the implementation of the optimization strategies. At the global level, there are two control states.

6.4.1 Decentralized, Droop-based Control Strategy

The fully decentralized, droop-based control takes into account local measurements of the nodes and operates without a global communication between the components. In this case, stored droop characteristics determine the virtual droop resistance and thus realize the load sharing between the components and the voltage control of the DC power line (Fig. 6.6).

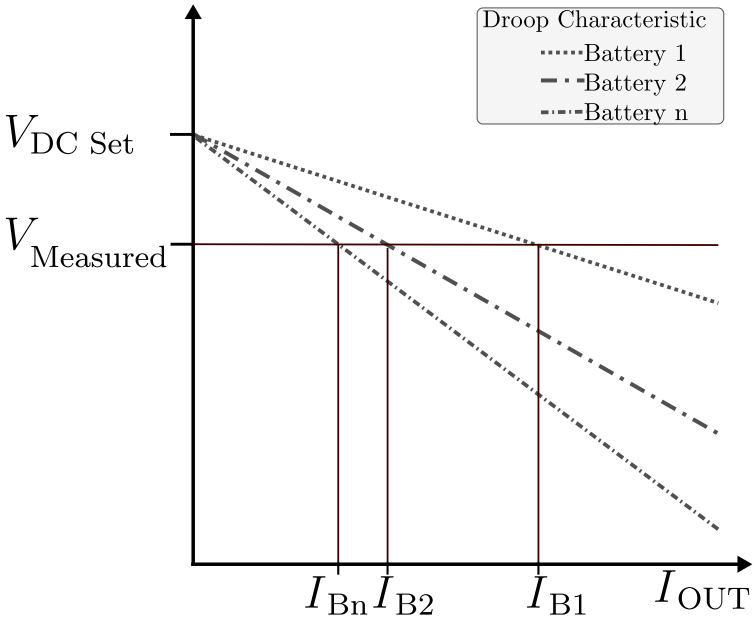


Figure 6.6: The slope of the droop curves of the local droop based controllers for the battery nodes and thus the value of the virtual internal resistances determine the discharge current and are adjusted according to the battery state. In local measurements, the actual DC power line voltage is acquired and compared with the stored droop characteristic to specify the output current. In this scenario, Battery 1 supplies the majority of the required power.

The DC line voltage is measured by each battery node and the respective droop characteristic is used to determine the output current accordingly. For battery state dependent load sharing, the slope of the droop characteristic can be changed depending on e.g., the battery fitness.

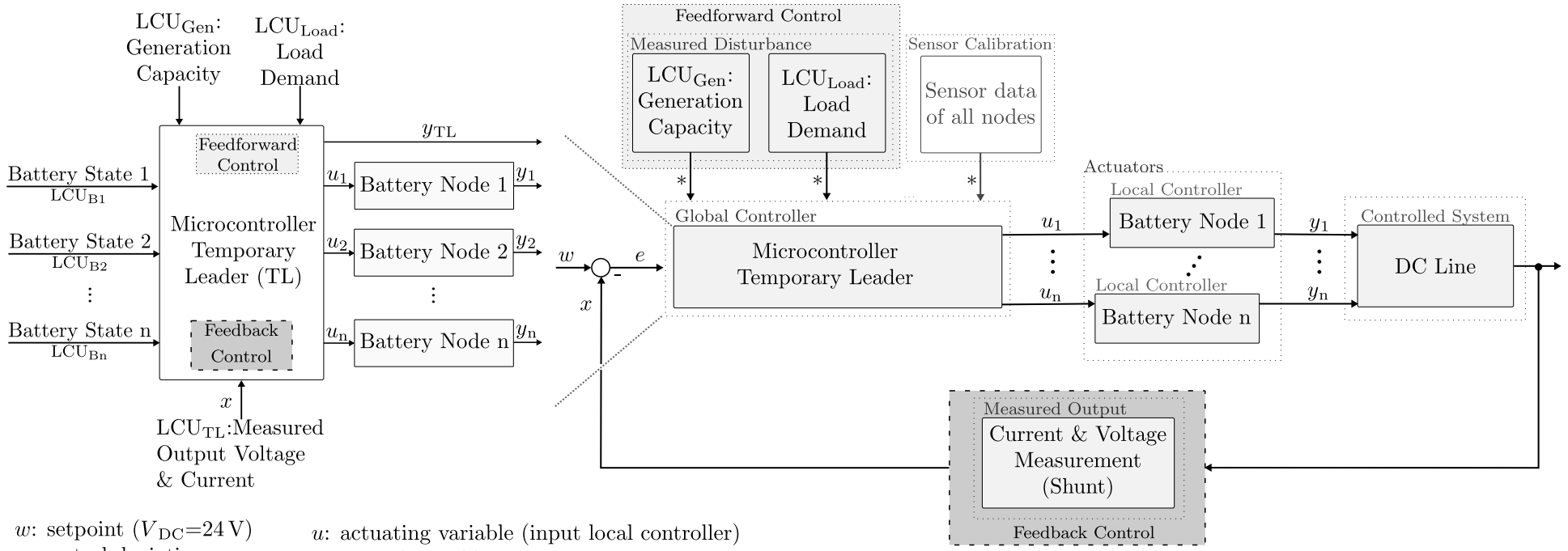


Figure 6.7: The cascaded control of the DBMS consists of an outer, global control loop and several inner, local control loops (Fig. 6.1). The microcontroller of the temporary leader is the global controller and it takes into account the battery states, the measured generation and power consumption as measured disturbances (feedforward control) and the measured actual values (feedback control) for the specification of the actuating variables. Furthermore the temporary leader steers its own DC-DC converter to adjust the remaining control deviation.

Droop control offers increased robustness, fail-safety and reliability due to its communication-less operation based on local measurements. Determining the droop characteristics and subsequently the droop settings is critical for safe battery operation, accurate DC power line voltage control and fair energy sharing. In this context, the selection of the droop characteristics represents a compromise between optimal energy sharing and optimal voltage regulation. In addition, the selection of inappropriate droop settings in nodes may lead to voltage fluctuations at the DC power line and a mismatch in current sharing. The droop parameter is the gain factor of a P-controller, i.e. the overall system is a parallel connection of several P-controllers with different gain factors. [333, 334]
As a result, a permanent control deviation remains. In summary, droop control offers improved robustness and reliability with limited control accuracy and a permanent control deviation.

6.4.2 Hierarchical, Communication-based Control Strategy

A further control strategy on the global level is the communication-based hierarchical control, where a functioning communication between all nodes is a prerequisite. All components, including the generators and loads, send their operating parameters via a global bus line (CAN FD) and manage the received operating data of all remaining participants. Consequently, each microcontroller has available all the data required for system control.

6.4.2.1 Challenges of Decentralized Systems Consisting of Autonomously Operating Nodes

In principle, all battery nodes are able to autonomously control the system by consuming or supplying surplus power according to the DC power line voltage measurement. This leads to a system of distributed autonomous nodes. The clocks of the distributed nodes cannot be perfectly synchronized, resulting in nodes operating to local clocks with small drifts and offsets. The clock drifts can be reduced, but not fully eliminated. To design the control for a system consisting of asynchronous operating nodes, all possible state transitions between the different nodes must be defined, which is a non-trivial task.

6.4.2.2 Introduction of Control Layers

Therefore, a hierarchical control consisting of two domains, the regulating domain and the actuating domain, is proposed, which still fulfills the system goals reliability, robustness, scalability, flexibility.
The tasks of the regulating domain include the specification of the control parameters of all batteries and thus a battery state-dependent adaptive load sharing to balance the battery states, the synchronization of the nodes, the management of the (de)activation of participating nodes and the implementation of the selected optimization strategy. One of the battery nodes is elected as the temporary leader, performing strategic and regulatory tasks. The temporary leader takes into account the battery states and the current load and generation data (Fig. 6.7). In addition to this, the temporary leader compensates for the permanent control deviation. For this reason, only a battery node can be elected. The remaining battery nodes operate as actuators according to the specifications of the temporary leader and form the actuating domain.

For the hierarchical, communication-based control, error-free communication between all participating nodes is a prerequisite. Compared to droop-based control, this strategy is more costly in terms of computing power and energy consumption of the microcontrollers. Communication between components, data management and monitoring as well as repeated calculation of the actuating variables depending on the operating parameters is required. The message exchange allows the generation and load values to be directly included in the feedforward control loop as measured disturbance. This improves control dynamics by eliminating the wait for effects of current generation and consumption on the DC power line voltage and its measurement and processing in the feedback control.
In summary, the battery state dependent load sharing and optimization strategies can be realized more precisely by direct specifications via the temporary leader compared to the adjustment of the droop characteristics. Furthermore, no permanent control deviation is required to determine the output values, which improves the control accuracy.
The droop-based and communication-based control strategies at the global control level exhibit different characteristics (Fig. 6.9) and requirements and, accordingly, are suitable for different operating states. Figure 6.8 shows the state diagram of the control at global level.
The state-transitions are defined by the equations (6.1) and (6.2).

A_1: *The temporary leader is elected and operational.*

A_2: *The global communication between all participating nodes and the leader is error-free.*

A_3: *The deviation of the measured DC power line voltage from the setpoint voltage is less than* $\pm 20\%$

A_4: *A software update is performed.*

A_5: *Components are added, removed or temporarily deactivated.*

A_6: *System start-up is performed.*

A_7: *System shut-down is performed.*

$$T_1 = A_1 \wedge A_2 \wedge A_3 \wedge \overline{A_4} \wedge \overline{A_5} \wedge \overline{A_6} \wedge \overline{A_7} \tag{6.1}$$

$$T_2 = \overline{T_1} = \overline{A_1} \vee \overline{A_2} \vee \overline{A_3} \vee A_4 \vee A_5 \vee A_6 \vee A_7 \tag{6.2}$$

6.5 Local Control Level Strategies

The global control level specifies the setpoints for the local control loops of each battery node (Fig. 6.10). In droop-based control, characteristics for the virtual internal resistance are determined for every battery node. These characteristics are compared to locally acquired measurement values and the intersection defines the current setpoint.

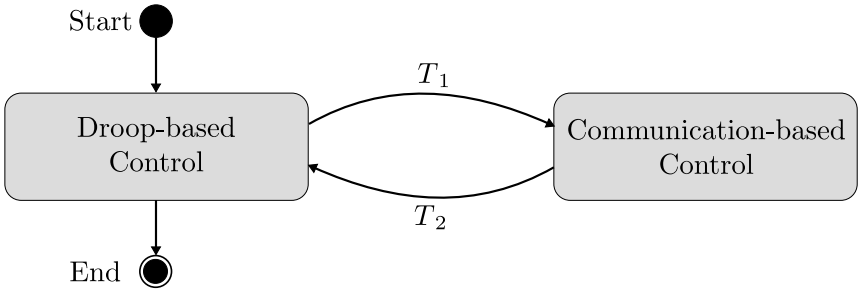


Figure 6.8: State diagram of the global control level with state transitions T_1 and T_2 (Equations 6.1, 6.2.)

In communication-based control, the temporary leader directly specifies and sends the setpoints via the communication line. The local control loop is a feedback control. The current and voltage sensors record the actual values and are part of the feedback control. The actual values are sent to the microcontroller, which monitors them and considers them in the control to the setpoints.
The LCUs of the loads and generators also capture the actual current values and send them to all participating nodes via the global communication line. This information is taken into account as a measured disturbance in the feedforward control section. Control stability and control dynamics are improved since the manipulated variables are adjusted directly instead of reacting to a change of the DC power line voltage due to excess or missing power.
The processing of the setpoints, i.e. the control according to those setpoints, is the task of the local control level. The actuator of the local control loop is the DC-DC

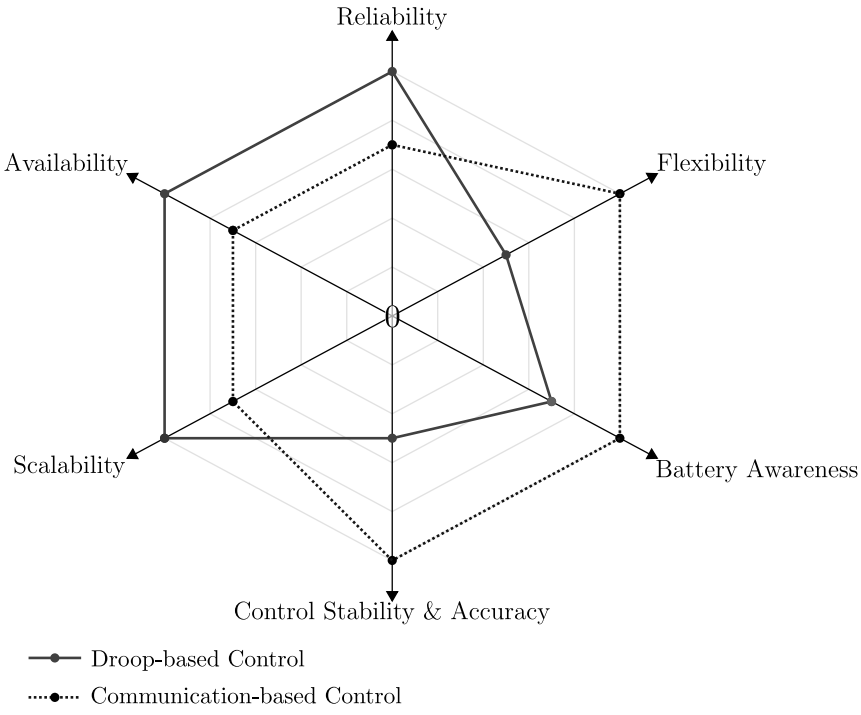
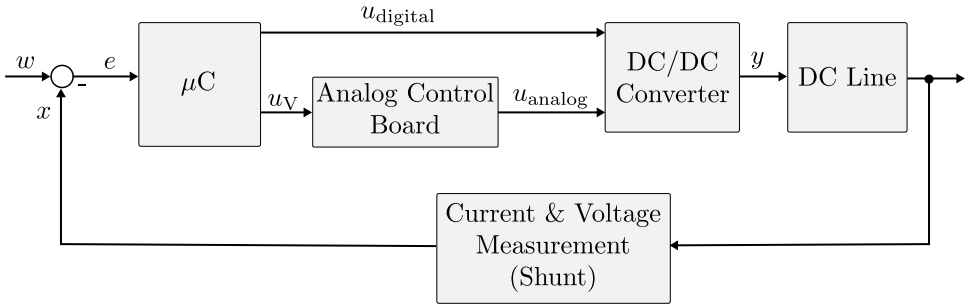


Figure 6.9: Estimation of the characteristics of the control strategies at the global control level: The droop-based control is characterized mainly by robustness and lower system requirements, while the communication-based control strategy provides more precise setpoint specifications and takes battery conditions into account more effectively.



w: setpoint (specification of global control level)
e: control deviation
x: measured output
u: actuating variable
y: control variable

Figure 6.10: The task of the local control loop is to control to the setpoint *w* specified by the global control level (Fig. 6.7). The actuator is the DC-DC converter whose control variable *y* is specified using either a digital or analog controller.

converter. For the DBMS, multiphase DC-DC converters combining a buck and a boost converter with a current controller are used [335]. Two separate half bridges are connected and controlled by a phase shifted signal. The use of two half-bridges divides the current by two and thus leads to lower current ripples, reduced losses and increased efficiency. The current controller is either analog or digital controllable (Figs. 6.10, 6.11). According to the setpoint current, the MOSFETs are controlled in such a way that the current measured via the shunt resistor corresponds to half of the setpoint current. In this chapter, the control methods and their implementation are considered in a superficial, conceptual way. Further detailed description of the DC-DC converter, the control methods and their implementation is given in the chapters 7, 8 and 9.

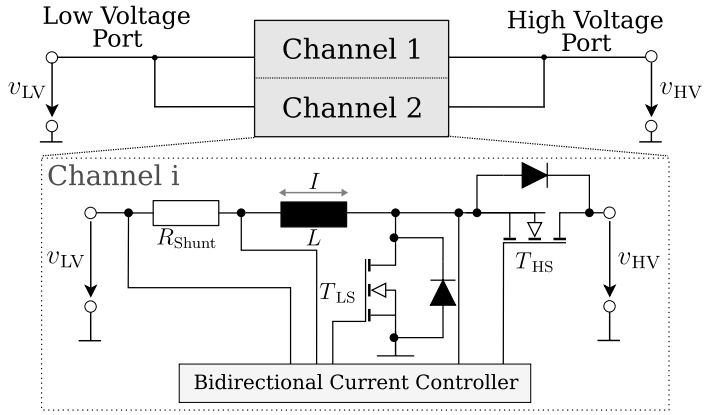


Figure 6.11: The bidirectional DC-DC converter used in the DBMS consists of two phase-shifted channels which in turn are based on half bridges. [336].

It is possible to switch between an analog, hardware-based control and a digital, software-based control at the local control level (Fig. 6.10).

6.5.1 Hardware-based Control

For analog control, an additional hardware-based control circuit is implemented (Fig. 6.12). Both the droop- and the communication-based control can be imple-

mented as analog controllers at the local control level. Details about the controller design follow in the further chapters 8 and 9.

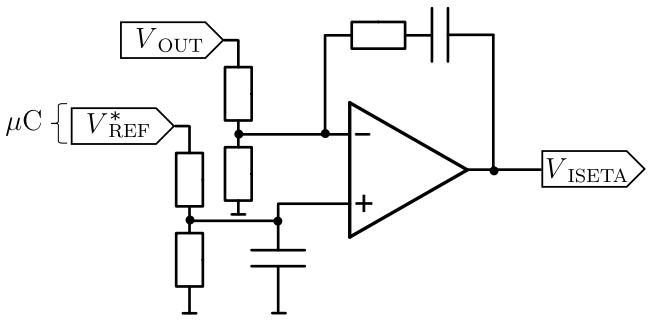


Figure 6.12: In the analog, hardware-based control, a voltage reference V_{ISETA} is specified for the subsequent current controller. Input signals are once the feedback output voltage, downscaled via a voltage divider, and a reference voltage specified via the DAC of the microcontroller. Both droop- and communication-based control can be implemented in analog mode.

The output voltage of the analog control circuit is the feedback reference voltage V_{ISETA} for the current controller [335]. Analog control at the local control level offers increased robustness with higher losses and thus lower efficiency. It exhibits less computational effort. Furthermore, it offers only limited control possibilities, since the circuit is fixed and corresponds to a P-controller with a variable gain factor.

6.5.2 Software-based Adaptive Control

In digital control, a Pulse Width Modulated (PWM) signal is directly generated by the microcontroller and functions as a reference signal (PWM_{ISETD}) for the current controller (Fig. 6.10). In this case the controller is not realized analogue with operational amplifier and the respective hardware components but it is fully digital implemented on the microcontroller. This provides more flexibility and the ability to use adaptive control.
Adaptive controllers can change their behavior in response to changes in the dynamics of the system and the type of control disturbances (Fig. 6.13). In contrast to the ordinary feedback control with constant gain, adaptive controllers change the gain or even the controller type according to the operating conditions [337].
Ordinary linear feedback with constant gain can work properly under a certain operating condition, i.e. within a predefined load range. However, difficulties may arise when the operating conditions change. A more sophisticated, adaptive controller offers the possibility to offer high control stability and accuracy in a variety of operating conditions.
In addition, it is possible to change the controller type of some or all of the battery nodes, e.g. to a PD controller or PI controller for specific operating conditions such as system startup, severe fluctuations, or for predictable or previously announced load/generation changes. In this case it is also possible to vary the values of the corresponding controller parameters.
In summary, digital adaptive control offers more flexibility and the possibility to improve control dynamics and stability over a variety of different operating conditions. The selection of the type of the adaptive controller, the determination of the controller types as well as the controller coefficients and the assignment to

the operating conditions with definition of the transition conditions are challenging tasks. Compared to the droop control, the computational effort is higher, but the losses caused by the hardware components are eliminated, positively affecting the efficiency of the system.

6.6 Assignment of the Control Strategies to the Operating States

The different operating states pursue various control goals and therefore it can be helpful to change the chosen control strategy. Figure 6.14 shows the different operating states that can occur in the DBMS.
In the operating states with high requirements for robustness and at the same time lower requirements for battery-optimal operation and control stability, the droop-based control strategy is used (Tab. 6.1). Advantageous in this case is that less system requirements have to be fulfilled, i.e. no communication between the nodes is necessary and no leader has to be selected. If possible, i.e. if there is enough battery capacity, if the communication works and if the leader is elected, the communication based control is enabled and more sophisticated and system oriented modes of operation become available (Tab. 6.1).

6.7 Summary

In this chapter, the control concepts of a decentralized battery management system were discussed. A battery management system was presented which can implement centralized, decentralized, distributed and hierarchical control strategies without hardware changes. The characteristics of different control strategies were evaluated considering the reliability and the control accuracy. Instead of using a single control strategy throughout the operation of the DBMS, the system is able to switch between different control strategies as various operating states also exhibit deviating properties. The control was divided into a global and local control level and two different strategies per each level were presented. The operating states were defined and a

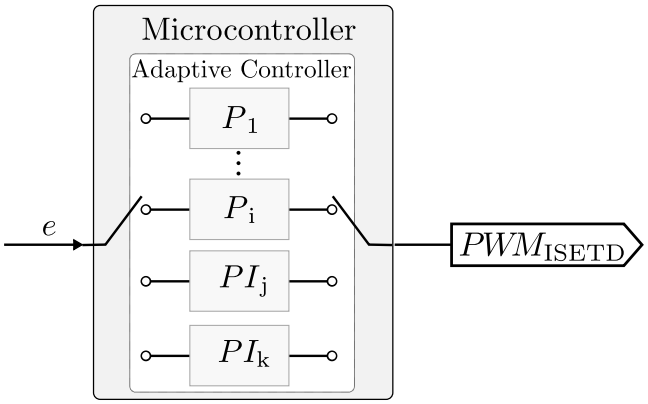


Figure 6.13: The digital adaptive controller offers increased flexibility. Depending on the type of control disturbances, the controller parameters and types can be changed during active operation. Several controller implementations can be realized by software. The microcontroller directly generates a PWM signal for the subsequent current controller.

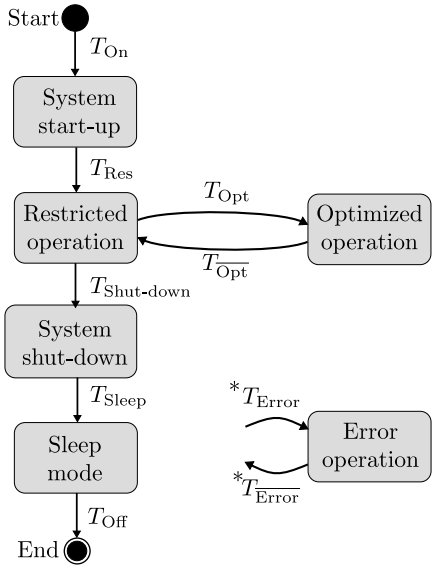


Figure 6.14: Operating states of the DBMS and the respective transfer conditions, which are defined in Tab. 5.1.
*Transfer to the state error operation is possible from all operating states.

Table 6.1: Description of the transfer conditions and assignment of the control strategies to the different operating states.

Operating State	Transfer	Transfer Condition	Global Control	Local Control
System start-up	T_{On}	Activation signal	droop-based	analog
Restricted operation	T_{Res}	Leader is elected and the deviation of the DC power line voltage from the setpoint is $\leq 20\%$	communication-based	analog in combination with digital
Optimized operation	T_{Opt}	Sufficient (dis)charge capacity available	communication-based	analog in combination with digital
Error operation	T_{Error}	Error occurrence such as interruption of communication or failure of leader	droop-based	analog
System shut-down	T_{Shut}	Deactivation signal	droop-based	analog
Sleep mode	T_{Sleep}	DC power line is potential-free	communication-based*	digital*

* Inactive - except for recharging processes.

first assignment of the control strategies was made. This assignment is the basis for the future implementation and further investigations regarding the scalability and robustness of the system. Furthermore, a method for switching between the control

strategies based on the bumpless transfer [338, 339] is planned be developed in further work, so that the change of the control strategies only minimally influences the control stability. Related future investigations include analyzing the control stability of the system depending on the number of nodes and comparing the control strategies in terms of energy efficiency.

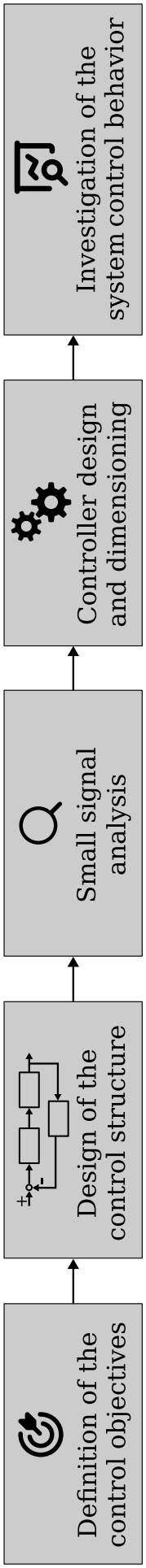


Figure 6.15: Overview of the entire controller design process and assignment of the individual chapters.

7

Control Oriented Mathematical Modeling and Stability Analysis of the Bidirectional DC-DC Converter

Bidirectional DC-DC converters combine buck and boost converters and allow power transfer in both directions. They are used in numerous applications, including uninterruptible power supplies, grid-connected or home storage battery systems. Parallel connection of different batteries equipped with bidirectional DC-DC converters offers an increase in total storage capacity, providing higher currents and improving the reliability and the system availability. To share the load current among the DC-DC converters while maintaining the safe operating range of the batteries, appropriate control approaches are needed. As a basis for the controller design, analysis of the small-signal model, knowledge of both the static and dynamic characteristics of the DC-DC converter and derivation of the transfer functions are required. In this chapter, the small-signal behavior of a DC-DC converter in buck and boost modes for both Continuous Conduction Mode (CCM) and Discontinuous Conduction mode (DCM) is analyzed using the circuit averaging technique. The control and line to output transfer functions relevant for the average current mode control and voltage control are derived using the averaged equivalent circuits. In addition, the poles and zeros are determined. The transfer functions, together with their poles and zeros, form the basis for the control analysis and the stability considerations. In summary, the equations for the poles and zeros are given for buck, boost and for CCM and DCM, respectively.

7.1 Motivation

To reduce CO_2 emissions and air pollution with ever-increasing global energy consumption, the integration of renewable energy sources and the electrification

of the transportation is crucial. The use of intermittent energy sources such as solar and wind power requires energy storage systems to further ensure grid stability and the reliability of energy supply. Battery systems are one of the most important options for energy storage given the rapid cost decline and additional benefits such as geographically independent deployability, mobile use, and availability. In recent years, numerous new battery technologies have been developed with the goal of further improving their electrochemical performance [26]. In addition, the number of retired batteries is expected to increase along with the market share and production volume of electric vehicles [340–342]. Used batteries, which no longer meet the requirements of electric vehicles in terms of dynamics and capacity due to increased internal resistance, find a second use, such as in home storage or in uninterruptible power supply systems. Second-life applications hold the potential to increase the lifetime and to optimize the costs and the resource exploitation of battery systems. In the sight of resource scarcity with ever-increasing energy storage demand, the integration of these batteries can contribute in balancing peak loads and stabilizing the grid.

Heterogeneous battery systems combine batteries with differences in cell chemistry, nominal capacity, State of Charge (SoC), State of Health (SoH), and in Safe Operating Areas (SOAs) in terms of SoC, temperature, and maximum (dis)charge current in one system. They enable synergy effects by exploiting different properties of various cell chemistries, such as low-temperature capability or resistance to high charging currents. They also offer the possibility of combining different second life batteries of varying types in conjunction with new ones.

Due to variations in output voltages and SOAs, the control of heterogeneous battery systems is challenging. Direct parallel connection of batteries with slightly varying output voltages results in high equalizing and circulating currents [343, 344]. This leads to specific requirements for the control and the power electronics, i.e. for the DC-DC converters (Fig. 7.1). A wide input voltage range on the low volt side is required to support various batteries. Variable SOAs demand a battery state dependent current limitation which has to be adjusted during operation. A bidirectional DC-DC converter combining a buck and a boost converter is required for power flow in the charge and discharge direction. [345, 346]

Parallel connection of multiple DC-DC converter modules offers benefits such as increased output power, expandability and improved reliability. An explicit current sharing mechanism is required to distribute the current and load between the nodes. Without this, even small imbalances in the output voltage will result in significantly different output current changes which may damage the SOAs of the batteries.

Appropriate control approaches are mandatory for precise current sharing while maintaining a stable DC link voltage. Further demands on the controllers of the DC-DC converters include coping with the nonlinear behavior of batteries, compensating fluctuations of the load, ensuring stability under all operating conditions, and providing a fast transient response.

The dimensioning of such control systems demands a fundamental understanding of the static and dynamic characteristics of the DC-DC converter. Therefore, the small-signal models using circuit averaging techniques and the derived transfer functions required for cascaded voltage and current control of a bidirectional DC-DC converter in all modes of operation must be defined and analyzed.

First, an overview of related work is given. Existing modeling approaches are described and the selection of the circuit averaging technique is explained. The DC-DC converter under investigation is described and the transfer functions relevant

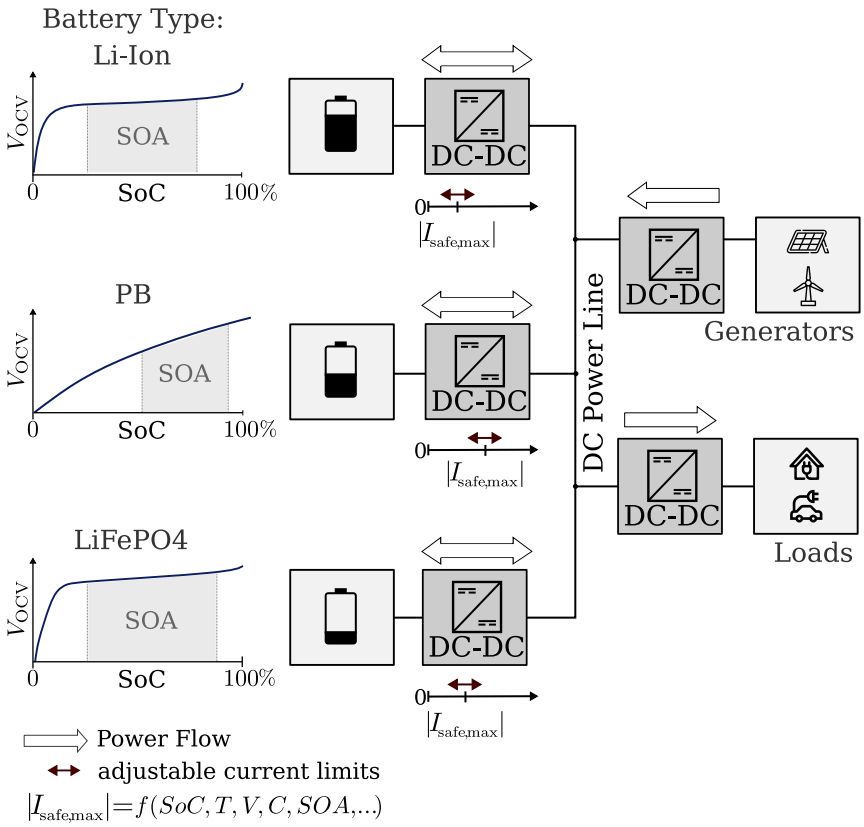


Figure 7.1: In the decentralized battery management system, bidirectional DC-DC converters with wide input voltage ranges and adjustable current limits ($|I_{Safe}|$) realize the power flow between different batteries with varying safe operating areas (SOA) and SoC dependent output voltages. Appropriate controllers are mandatory for precise current sharing between the parallel connected converters.

for voltage and average current mode control are presented. The small-signal models are introduced and subdivided into buck and boost modes depending on the operation mode of the DC-DC converter, and further into CCM and DCM. The transfer functions are comprehensibly derived from the averaging equivalent circuits and the poles and zeros of the defined transfer functions are determined. Summarizing, the poles and zeros are shown in all operating modes including buck, boost and respectively CCM and DCM.

Nomenclature for the Equations

In the following, capital letters are used for the description of average values. Complex values are not underlined. Alternating components are marked by the prefix ∂ and time-dependent quantities are described by lower case letters.

7.2 Related Work

Existing small-signal modeling approaches include the state space averaging [347–352], the switched inductor modeling [353–355] and the circuit averaging technique [356–359]. The operation of pulse width modulated (PWM) DC-DC converters is based on the alternate detour of the inductor current by a periodically controlled switch and a diode, whereby the latter two components are the time-varying part of

the circuit. The basic principle of all the aforementioned modeling approaches is the averaging of these individual switching states.
Using the state space averaging method, the state equations and associated state vectors for each state of the switch are defined. In each subinterval, one position of the switch (open or closed) is considered and the DC-DC converter is represented by a corresponding linear circuit. The equations are then averaged according to the dwell times and used as a basis for determining the transfer functions. The switched inductor modeling and the circuit averaging technique are based on the derivation of linear equivalent circuits replacing the active switch and the diode of the actual circuit. Consequently, the derived transfer functions describe only the change in magnitudes as an average over a switching period.
The equivalent circuit generated by the switched inductor modeling is based on the principle that by applying an average voltage to an inductor, the average current flowing through it, is obtained. This current is then included as a dependent current sources to emulate the average currents. [353]
In the averaged switching modeling approach, the low-frequency components of the DC-DC converter are determined while the high-frequency switching harmonics are discarded through a procedure referred to as averaging. The result is a time-invariant equivalent circuit that models the DC and low-frequency AC components. It replaces the semiconductor switches and is well suited for simulation. [357]

Explanation of the Model Selection

In the following, the circuit averaging technique is used and separate linear equivalent circuits are generated for the different operating modes (Figs. 7.15, 7.18, 7.19). Advantages of this approach include the efficient consideration of parasitic effects and the possibility to simulate the averaged models, e.g. to analyze the small-signal transfer functions. This technique can also be applied to PWM converters operating in DCM, which in this case is significant for the design of appropriate control approaches used within the DBMS. A detailed explanation of the choice of this method as well as the corresponding derivations are described in more detail in [356, pp. 547-674].
Existing papers address the modeling of bidirectional DC-DC converters focus on single operating modes [360–364], for example DC-DC converters in CCM [365] or in boost mode and DCM [366]. They provide models in all operating modes, but use different approaches, e.g. state space [367–371]. Further attempts specialize in DC-DC converters based on full bridges or specializations thereof [372–377]. They show improvements of existing modeling approaches, e.g., in terms of accuracy and computational effort [359, 378] or they focus on large signal models [379, 380].
Complementing existing work, this chapter presents the models corresponding to the circuit averaging technique of a bidirectional DC-DC converter based on two half-bridges in all operating modes, including CCM and DCM. Furthermore, the transfer functions relevant for current control are comprehensibly derived and all the required equations are summarized.

7.3 Description of the Bidirectional DC-DC Converter

A multiphase, Pulse Width Modulated (PWM) bidirectional DC-DC converter consisting of two phase-shifted half-bridges is used in the heterogeneous battery system and investigated. Figure 7.2 shows the circuit of one of the two channels. For

current control, the LM5170 controller is used, which offers the possibility to provide an analog reference voltage (ISETA, V_{ISETA}) or a pulse width modulated digital signal (ISETD, PWM_{ISETD}) to specify the current set point. Depending on the two operating modes buck and boost, one of the two MOSFETs works as *main* and the other one as *sync* MOSFET. During boost mode the *main* MOSFET is T_{HS}, in buck mode the *main* MOSFET is the T_{LS}. In each case the other MOSFET works as *sync* MOSFET.
Diode emulation mode is used for the switching of the MOSFETs, i.e. the MOSFETs are switched complementary: If the *main* MOSFET is on, the *sync* MOSFET is off, and vice versa. While the *main* MOSFET is driven, the current across the inductor increases and while the *sync* MOSFET is driven, the current across the inductor decreases. When the current reaches 0 A, the diode emulation mode is activated and the *sync* MOSFET is switched off. This leads to improved efficiency at low load power.

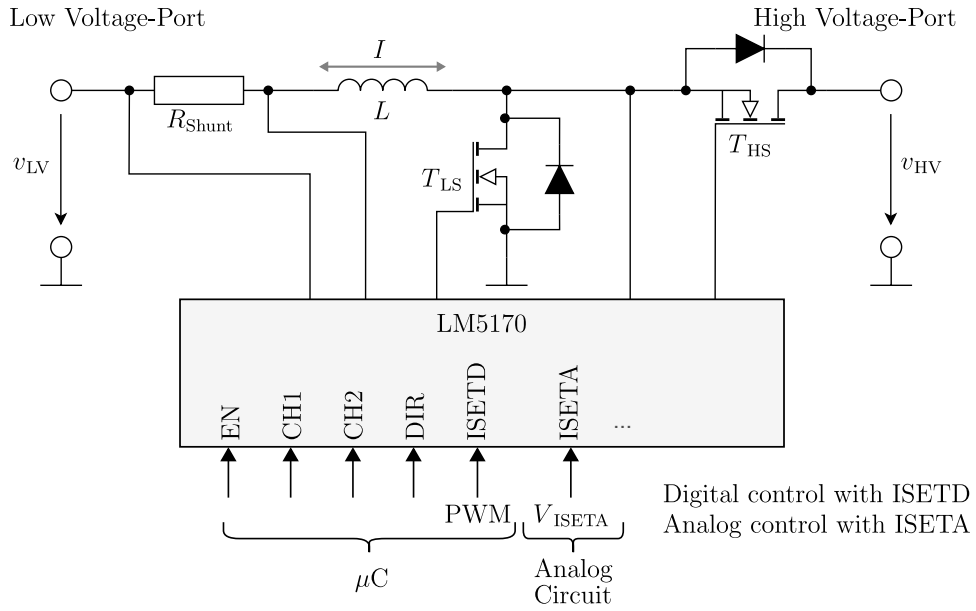


Figure 7.2: Circuit of one of the two half bridges of the bidirectional DC-DC converter together with the current controller LM5170.

7.4 Theoretical Background

The different operating modes that occur with DC-DC converters are described below. Furthermore, a selection of transfer functions is specified, which are relevant for the average current and voltage control.

7.4.1 Operating Modes of the DC-DC Converter

Bidirectional DC-DC converters, including those based on a half-bridge topology, have three different modes of operation: CCM, Boundary Conduction Mode (BCM) and DCM (Fig. 7.3). The operating mode of a DC-DC converter is primarily determined by the ratio between the value of the inductance, the load current and by the duty cycle. The duty cycle hereby describes the ratio between the on-time of the switch and the total switching cycle duration. The inductance stores energy during the on-time (switch is closed) and releases it during the off-time (switch is open).
When the switch is closed in CCM, the current in the inductor increases, and when the switch is opened, the current decreases but does not reach the value zero. This

means that during the switching cycle, there is always energy stored in the inductor that can be transferred to the output capacitor and the load. The BCM is the boundary operation between the CCM and DCM. Here, the inductor current just reaches zero at the end of the switching period. The DCM is a mode of operation where the inductor current drops to zero before the end of the switching cycle time and remains at zero until the end of it. This occurs when the load current is relatively low and the value of the inductance is small enough to allow the current to drop to zero before the next switching cycle.
The different modes of operation affect the control strategy and the behavior of the DC-DC converter, for instance the output voltage ripple, the stability of the feedback loop and the efficiency. In terms of control, the CCM exhibits better output voltage control and lower output voltage ripple due to the continuous inductor current. Despite that, higher switching losses and lower efficiency can occur compared to the DCM, especially at low load. The DCM, in contrast, offers improved transient response and faster load control due to the faster current decay in the inductor. Challenging aspects regarding the control are the discontinuous current waveform and the higher output voltage ripple in the DCM. [356]

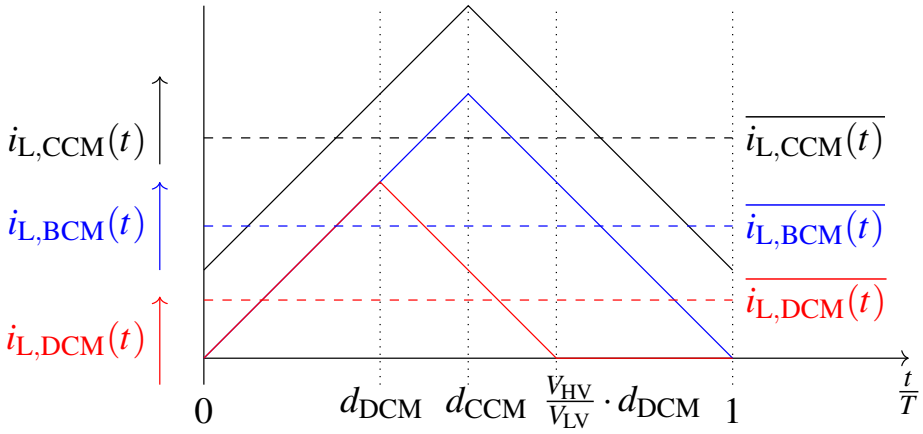


Figure 7.3: Waveforms of the inductor currents in continuous conduction mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM), where d_{CCM} and dDCM are the duty cycles which determine the on-times of the switches.

7.4.2 Small-Signal Transfer Functions

Transfer functions are the basis for the development of control strategies, the stability evaluation and the performance analysis. The transfer functions differ according to the topology, the control mechanism utilized, and the mode of operation, which depends on buck, boost, CCM and DCM.
Small-signal transfer functions refer to the quantitative behavior in response to small changes at the input or output. They are expressed in terms of small-signal models, which are linearized models that represent the behavior of the converter around a steady-state operating point.
Generally, considering voltage and current control, there are four basic transfer functions (Fig. 7.4). A distinction is made between the Control to Output Transfer Function (COTF) ($\partial V_{in} = 0$) and the Line to Output Transfer Function (LOTF) ($\partial d = 0$). The COTF specifies the influence of the controlled variable and the duty cycle d on the DC-DC converter output. The relation between the duty cycle and

the output voltage $G_{\mathrm{vd}}(s)$ is relevant for the description of the voltage loop. The transfer function from output current to duty cycle $G_{\mathrm{id}}(s)$ is essential for the current mode control (CMC). The LOTF describes the behavior of the output voltage $G_{\mathrm{vg}}(s)$ or current $G_{\mathrm{ig}}(s)$ in case of input disturbances, e.g., input voltage fluctuations or drops. [381]

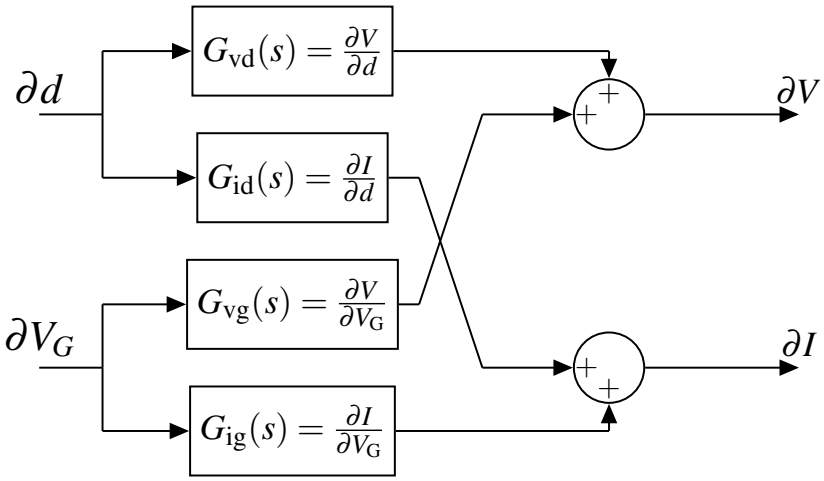


Figure 7.4: Selection of the basic transfer functions of a DC-DC converter for voltage and average current mode control, where ∂V is the output voltage, ∂I is the output current, ∂d is the duty cycle and $\partial V_{\mathrm{g}}(t)$ is the small-signal disturbance input. [356]

The transfer function $G_{\mathrm{vi}}(s)$ of output current ∂I to output voltage ∂V is essential for current and voltage control, as well as for determining the closed-loop output impedance.
In the following, only the Average Current Mode Control (ACMC) is considered and the Peak Current Mode Control (PCMC) is excluded, since it is not relevant for the control of the DC-DC converter under investigation. The current to output transfer function $G_{\mathrm{vi}}(s)$ for the ACMC can be derived from the two known transfer functions $G_{\mathrm{vd}}(s)$ and $G_{\mathrm{id}}(s)$:

$$G_{\mathrm{vd}}(s) = G_{\mathrm{id}}(s) \cdot G_{\mathrm{vi}}(s) = \frac{\cancel{\partial I}}{\partial d} \cdot \frac{\partial V}{\cancel{\partial I}} \tag{7.1}$$

$$G_{\mathrm{vi}}(s) = \frac{G_{\mathrm{vd}}(s)}{G_{\mathrm{id}}(s)} \tag{7.2}$$

7.5 Buck Mode of the Bidirectional DC-DC Converter

When charging the batteries or supplying a load with lower supply voltage, the bidirectional DC-DC converter operates in buck mode. In this section, the equivalent circuit diagrams and equations of the DC-DC converter operating in buck mode are presented for determining the small-signal models and deriving the transfer functions of CCM and DCM.
In the equivalent circuit of an ideal buck converter (Fig. 7.5), a diode replaces the MOSFET and replicates the undercurrent shutdown and the switching behavior. In this case, the transistor is driven by a PWM signal $v_{\mathrm{G}}(t)$ with period T_{s} and duty cycle d.

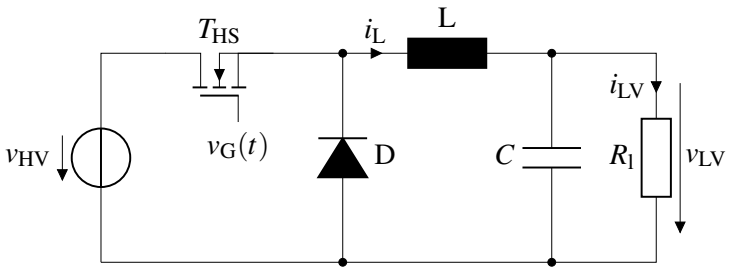


Figure 7.5: Equivalent circuit diagram of an ideal buck converter. The input capacitor is assumed to be free of losses and is replaced by an ideal voltage source. [356]

In CCM the transformer ratio is given by:

$$\frac{V_{HV}}{V_{LV}} = d \tag{7.3}$$

Thereby V_{HV} is the static voltage at the high side and V_{LV} is the static voltage at the low side of the DC-DC converter. The equation (7.3) is valid up to the Boundary Conduction Mode (BCM). The current through the output capacitor is by definition free of any mean value and the current through the inductance i_L is equal to the load current i_{LV} (Fig. 7.5). The BCM occurs when the following is fulfilled:

$$\begin{aligned} I_{BCM} = I_{LV} = \frac{\Delta I_L}{2} \cdot \frac{(V_{HV} - V_{LV}) \cdot d \cdot T_s}{2 \cdot L} = \\ = \frac{V_{LV} \cdot (1-d) \cdot T_s}{2 \cdot L} \end{aligned} \tag{7.4}$$

where ΔI_L describes the change of the current through the inductance during one period. At this operating point, the following applies:

$$i_L(0) = i_L(T_s) = 0, \ otherwise \ i_L(t) > 0 \tag{7.5}$$

7.5.1 Small-Signal Model and Derivations of the Transfer Functions for Buck Mode and CCM

Figure 7.6 shows the equivalent circuit according the circuit averaging method for the DC-DC converter in buck mode in CCM. Since the output voltage does not influence the current control, only the current transfer functions are considered in the following.

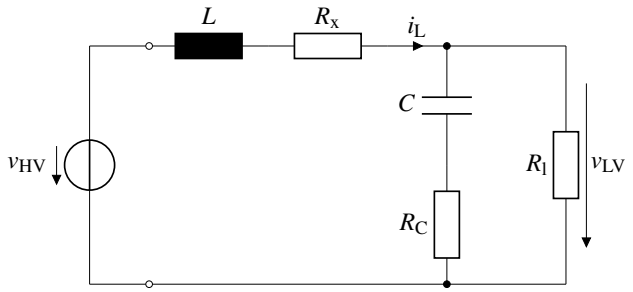


Figure 7.6: Equivalent circuit diagram of the output low-pass of the DC-DC converter in buck mode and in CCM. [356]

7.5.1.1 Duty Cycle to Current Transfer Function $G_{\mathrm{id}}(s)$

The resulting current at an applied input voltage is determined by the RLC network, where R_{x} describes the equivalent resistance, which results from the shunt and parasitic resistance of the inductor. The input voltage v_{in} at the RLC-network corresponds to the mean value of the voltage at the high voltage side v_{HV}. For CCM operation, the following applies regarding the input voltage:

$$v_{\mathrm{in}} = d \cdot v_{\mathrm{HV}} \tag{7.6}$$

Describing the duty cycle d and the voltage on the high voltage side with large signal and small-signal components results in:

$$\begin{aligned} v_{\mathrm{in}} &= (d + \partial d) \cdot (V_{\mathrm{HV}} + \partial V_{\mathrm{HV}}) \\ &= d \cdot V_{\mathrm{HV}} + \partial d \cdot V_{\mathrm{HV}} + \partial V_{\mathrm{HV}} \cdot d + \underbrace{\partial d \cdot \partial V_{\mathrm{HV}}}_{\ll} \end{aligned} \tag{7.7}$$

where $\ll$ is used to indicate very low values compared to the remaining ones. The last element can be neglected due to its low value compared to the other ones. The first element describes the large signal part and is neglected for the small-signal considerations. Consequently, two transfer functions can be derived from this consideration (Fig. 7.4).
The relation between the input voltage and the current through the inductor are determined by the complex alternating current calculation:

$$G_{\mathrm{id}}(s) = \frac{\partial I_{\mathrm{L}}}{\partial d} = \frac{V_{\mathrm{HV}}}{R_{\mathrm{x}} + sL + \frac{R_{\mathrm{l}} \cdot (R_{\mathrm{C}} + \frac{1}{sC})}{R_{\mathrm{l}} + R_{\mathrm{C}} + \frac{1}{sC}}} \tag{7.8}$$

Under the realistic assumption $R_{\mathrm{x}}, R_{\mathrm{C}} \ll R_{\mathrm{l}}$ follows:

$$G_{\mathrm{id}}(s) = \frac{1}{R_{\mathrm{l}}} \cdot \frac{1 + C \cdot R_{\mathrm{l}} \cdot s}{1 + \frac{L}{R_{\mathrm{l}}} \cdot s + L \cdot C \cdot s^2} \cdot V_{\mathrm{HV}} \tag{7.9}$$

Equation (7.9) shows that the gain depends on the input voltage. The transfer function has a zero point

$$|s_0| = \left| \frac{1}{R_{\mathrm{l}} \cdot C} \right| \tag{7.10}$$

and a conjugate complex pole pair:

$$\begin{aligned} |s_{\infty,1,2}| &= \left| \frac{\pm\sqrt{1 - 4 \cdot \frac{C}{L} \cdot {R_{\mathrm{l}}}^2} - 1}{2 \cdot R_{\mathrm{l}} \cdot C} \right| \\ &= \left| \frac{\pm\sqrt{1 - 4 \cdot \frac{C \cdot R_{\mathrm{l}}}{\frac{L}{R_{\mathrm{l}}}}} - 1}{2 \cdot R_{\mathrm{l}} \cdot C} \right| \end{aligned} \tag{7.11}$$

Thereby $\frac{L}{R_{\mathrm{l}}}$ corresponds to the time constant of the LR-filter, which is relevant for the behavior of the current. Respectively, $R_{\mathrm{l}} \cdot C = \tau$ corresponds to the time constant of the RC-filter. To obtain and maintain a constant output voltage also in the DCM, the

following applies for the design of the output capacitance:

$$R_\mathrm{l} \cdot C \gg \frac{L}{R_\mathrm{l}} \tag{7.12}$$

For high frequencies, the zero- and first-order terms in the denominator and zero-order terms in the numerator in equation (7.9) can be neglected and for the current transfer function at high frequencies $G_{\mathrm{id,hf}}(s)$ follows:

$$G_{\mathrm{id,hf}}(s) \approx \frac{V_\mathrm{HV}}{R_\mathrm{l}} \cdot \frac{C \cdot R_\mathrm{l} \cdot s}{L \cdot C \cdot s^2} = \frac{V_\mathrm{HV}}{R_\mathrm{l}} \cdot \frac{R_\mathrm{l}}{L \cdot s} \tag{7.13}$$

At high frequencies the phase response decreases continuously with $20\frac{db}{dec}$ and the transfer function is approximately $G_{\mathrm{id,hf}}(s) = \frac{1}{s}$ (I-behavior) (Fig. 7.7).
At low frequencies, the following gain $G_{\mathrm{id,lf}}(s)$ is obtained:

$$G_{\mathrm{id,lf}}(s) \approx \frac{V_\mathrm{HV}}{R_\mathrm{l}} \tag{7.14}$$

Neglecting the resonance overshoot and approximating using the common-mode gain and high-frequency response, the following approximation of the transfer function $G_{\mathrm{id,A}}(s)$ is obtained:

$$\begin{aligned} G_{\mathrm{id,A}}(s) &= \frac{V_\mathrm{HV}}{(R_\mathrm{x} + R_\mathrm{l})} \cdot \frac{1}{1 + \frac{L}{R_\mathrm{x}+R_\mathrm{l}} \cdot s} \\ &\approx \frac{V_\mathrm{HV}}{R_\mathrm{l}} \cdot \frac{1}{1 + \frac{L}{R_\mathrm{l}} \cdot s} \end{aligned} \tag{7.15}$$

Bode plots of both transfer functions, the exact (Equ. (7.8)) and the approximated (Equ. (7.15)) are shown in Fig. 7.7. In the approximation, the resonance overshoot and the resulting phase changes are completely neglected.

7.5.1.2 Current to Voltage Transfer Function $G_{\mathrm{vi}}(s)$

In order to determine the voltage transfer function, the current transfer function is used and the output filter is taken into account. The equivalent circuit is used to derive the transfer function of the output filter (Fig. 7.8).
For the voltage transfer function $G_{\mathrm{vi}}(s)$, the following results:

$$\begin{aligned} G_{\mathrm{vi}}(s) &= \frac{\partial V_\mathrm{LV}(s)}{\partial I_\mathrm{L}(s)} = R_\mathrm{l} \cdot \frac{1 + s \cdot R_\mathrm{C} \cdot C}{1 + s \cdot (R_\mathrm{l} + R_\mathrm{C}) \cdot C} \\ &\approx R_\mathrm{l} \cdot \frac{1 + s \cdot R_\mathrm{C} \cdot C}{1 + s \cdot R_\mathrm{l} \cdot C} \end{aligned} \tag{7.16}$$

The parasitic resistance R_C creates a zero point with the following frequency:

$$|s_{0,1}| = \left| \frac{1}{R_\mathrm{C} \cdot C} \right| \tag{7.17}$$

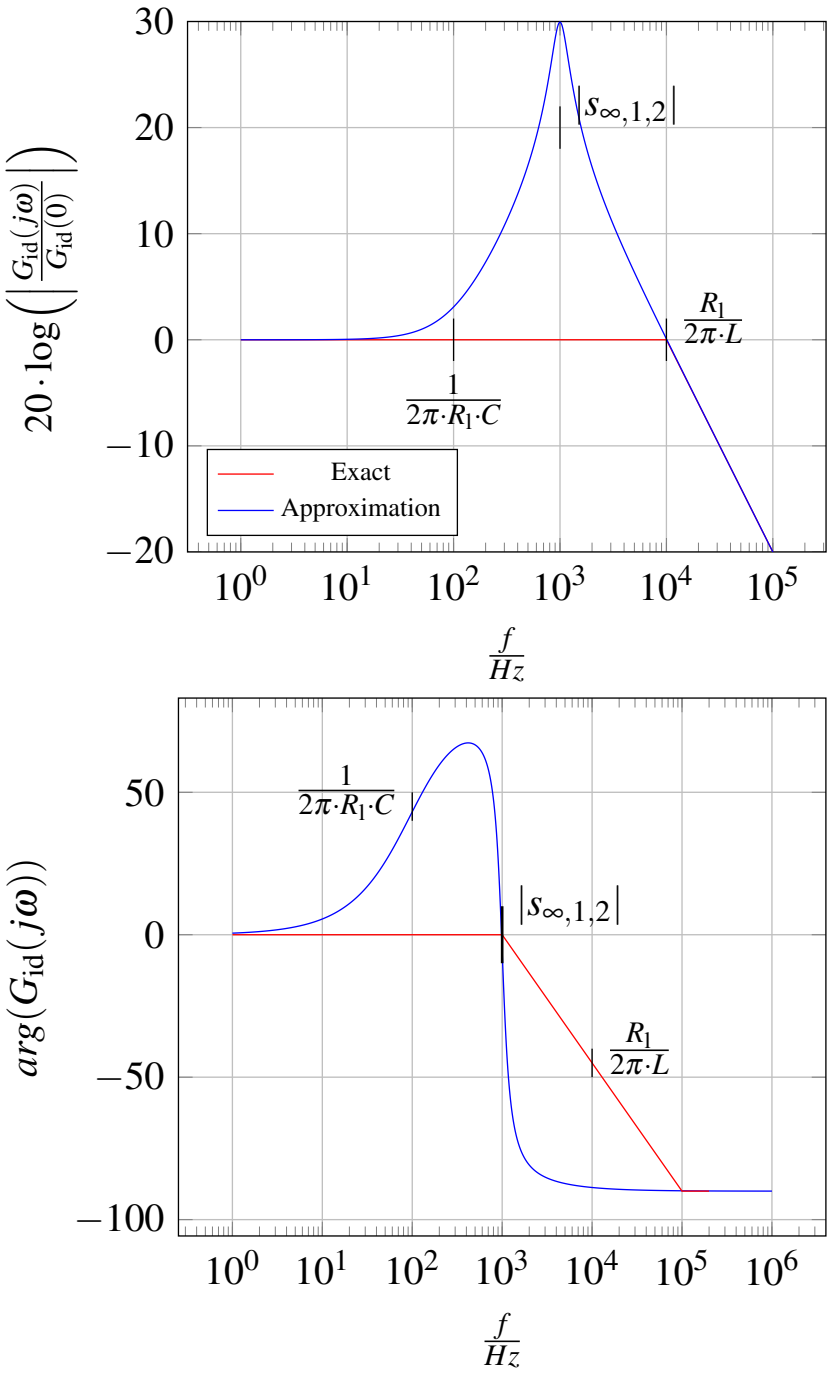


Figure 7.7: Bode plots of the derived, calculated transfer function $G_{id}(s)$ (exact Equ. (7.8) and approximated Equ. (7.15)), whereby the resonant behavior is neglected in the approximation. The straight lines are approximations. The largest part of a phase shift caused by a complex pole is limited to a frequency range whose width depends on the pole damping [382]. Here, the pole damping is 0.16. Equation (7.11) defines the pole positions.

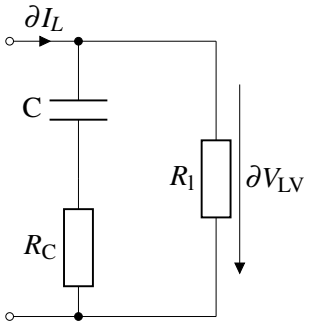


Figure 7.8: Equivalent circuit diagram of the output low-pass filter forming the basis for deriving the voltage transfer function. [356]

The pole, in contrast, generally shows very low frequencies:

$$|s_{\infty,1}| = \left|\frac{1}{R_\mathrm{l} \cdot C}\right| \tag{7.18}$$

7.5.1.3 Duty Cycle to Voltage Transfer Function $G_\mathrm{vd}(s)$

Multiplying equation (7.9) with equation (7.16) results in the duty cycle to voltage transfer function:

$$G_\mathrm{vd}(s) = V_\mathrm{HV} \cdot \frac{1 + s \cdot R_\mathrm{C} \cdot C}{1 + s \cdot \frac{L}{R_\mathrm{l}} + s^2 \cdot L \cdot C} \tag{7.19}$$

7.5.2 Small-Signal Model and Derivations of the Transfer Functions for Buck Mode in DCM

For the derivations of the transfer functions in DCM mode, the circuit averaging method is likewise used and corresponding equivalent circuits (Fig. 7.10) are defined [356, pp. 586-608]. For the control behavior and further consideration, the influence of the input voltage change ($\partial V_{HV} = 0$) is not taken into account and the simplified equivalent circuit in Fig. 7.11 results. In the following, R_x is neglected for simplification, since it does not make a significant difference.

Table 7.1: Specification of the equivalent circuit elements. d is the duty cycle, T_s is the period, and $V = V_\mathrm{HV}$ is the small-signal voltage change [356].

g_1	j_1	r_1	g_2	j_2	r_2	$M = \frac{V_\mathrm{HV}}{V_\mathrm{LV}}$	R_e
$-\frac{1}{R_\mathrm{e}}$	$\frac{2\cdot(1-M)\cdot V_\mathrm{HV}}{d\cdot R_\mathrm{e}}$	R_e	$\frac{2-M}{M\cdot R_\mathrm{e}}$	$\frac{2\cdot(1-M)\cdot V_\mathrm{HV}}{d\cdot M\cdot R_\mathrm{e}}$	$M^2 \cdot R_\mathrm{e}$	$\frac{2}{1+\sqrt{1+4\frac{R_\mathrm{e}}{R_\mathrm{l}}}}$	$\frac{2\cdot L}{d^2\cdot T_\mathrm{s}}$

7.5.2.1 Duty Cycle to Current Transfer Function $G_\mathrm{id}(s)$

From the averaging equivalent circuit (Fig. 7.11), the current transfer function $G_\mathrm{id}(s)$ (Fig. 7.4) is derived. With insertion of the values of the equivalent circuit elements r_2

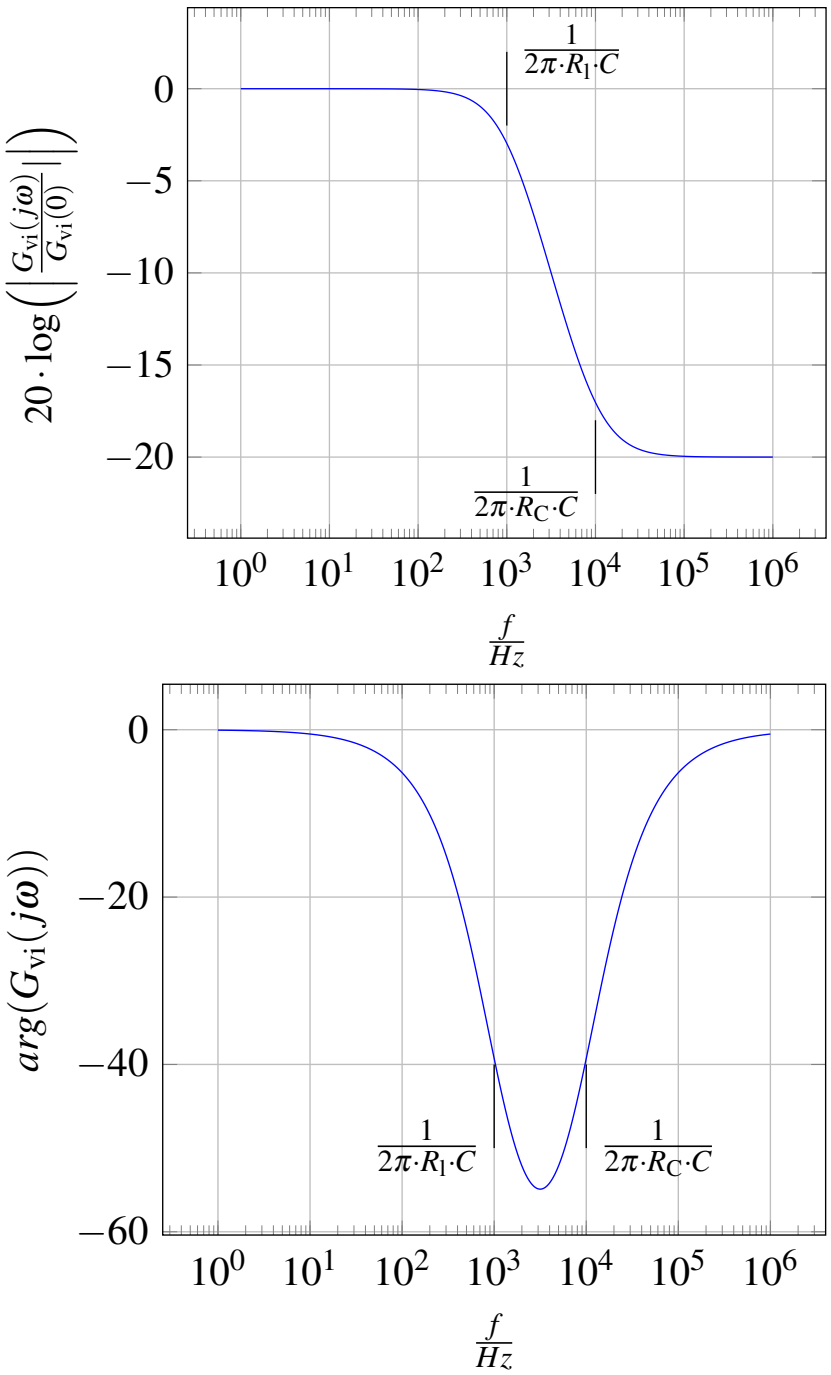


Figure 7.9: Bode plots of the calculated transfer function of the output current to the output voltage $G_{vi}(s)$ (Equ. (7.16)).

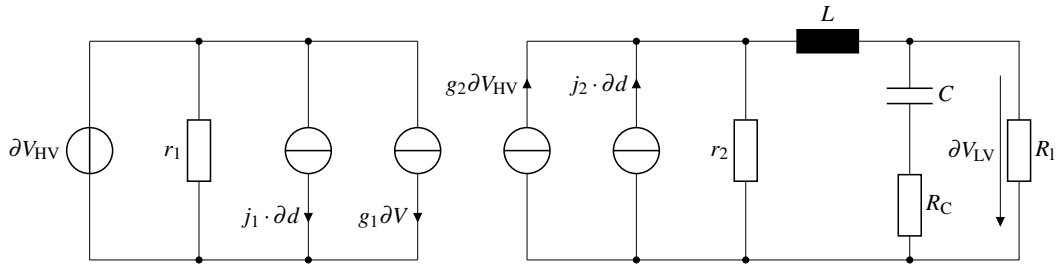


Figure 7.10: Equivalent circuit diagram of the DC-DC converter in buck mode and in DCM. The values of the equivalent circuit elements are defined in Table 7.1. [356]

and j_2 (Tab. 7.1) it follows:

$$G_{id}(s) = \left.\frac{\partial I}{\partial d}\right|_{\partial V_{HV}=0} = \frac{1}{1+\frac{sL+(R_C+\frac{1}{sC})||R_l}{r_2}} \cdot j_2 \tag{7.20}$$
$$= \frac{1+s\cdot(R_l+R_C)\cdot C}{(1+\frac{R_l}{r_2})+s\cdot\left(\frac{L}{r_2}+(R_l+R_C)\cdot\cdot C+\frac{R_l R_C C}{r_2}\right)+s^2\cdot\left(LC\cdot(\frac{R_C+R_l}{r_2})\right)} \cdot j_2$$

According to Table 7.1 the following results for r_2:

$$r_2 = (1-M)\cdot R_l \tag{7.21}$$

As $(R_C \ll R_l) \cap (R_C \ll 1) \cap (R_C \ll r_2)$ applies, the equation (7.20) can be simplified without significant deviation to:

$$G_{id}(s) = \frac{1+R_l C s}{\left(1+\frac{R_l}{r_2}\right)+s\cdot(\frac{L}{r_2}+R_l C)+s^2\cdot(LC\frac{R_l}{r_2})} \cdot j_2 \tag{7.22}$$
$$= \frac{1+R_l C s}{(r_2+R_l)+s\cdot(L+r_2 R_l C)+s^2\cdot(L\cdot C\cdot R_l)} \cdot r_2 j_2$$

Considering the sum $(L+r_2\cdot R_l\cdot C)$, the element L can be neglected compared to $r_2\cdot R_l\cdot C$ due to the relation of the time constants in the reasonable operating range. The zero point is identical with the one in CCM. There is a significant difference for the poles. They can be determined using the solution formula for quadratic equations.

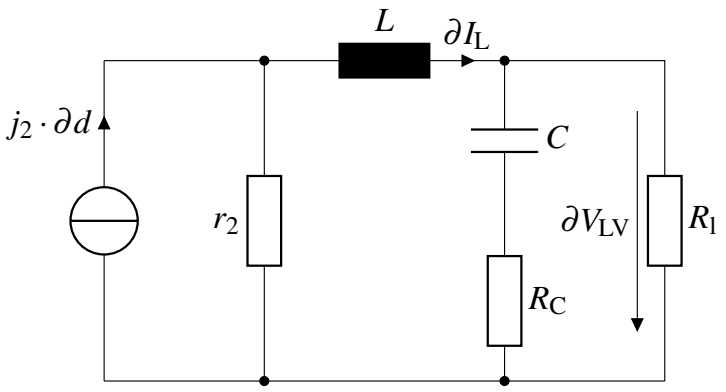


Figure 7.11: Simplified small-signal equivalent circuit in buck mode and in DCM neglecting the influence of the input voltage change $\partial V_{HV} = 0$. [356]

The discriminant D results to:

$$\begin{aligned} D &= (r_2 \cdot C \cdot R_\mathrm{l})^2 - 4 \cdot L \cdot C \cdot {R_\mathrm{l}}^2 \cdot \left(\frac{r_2}{R_\mathrm{l}} + 1\right) \\ &= (r_2 \cdot C \cdot R_\mathrm{l})^2 \cdot \left(1 - \frac{4 \cdot L}{r_2} \cdot \frac{1}{R_\mathrm{l} \cdot C} - \frac{4 \cdot L}{C \cdot r_2^2}\right) \end{aligned} \tag{7.23}$$

The magnitude of the subtrahend reaches maximum value at minimum output resistance. After inserting equation (7.21) and equation (7.4) the following results for the discriminant D:

$$D = (r_2 \cdot C \cdot R_\mathrm{l})^2 \cdot (1 - 2 \cdot T_s \frac{1}{R_\mathrm{l} \cdot C} - \frac{T_s^2}{L \cdot C}) \tag{7.24}$$

In the reasonable operating range, it is a prerequisite that the time constants of the filters are considerably larger than those of the switching period. Therefore, the poles in DCM operation are expected to be real (Fig. 7.12):

$$|s_{\infty,1,2}| = \left| \frac{-(\frac{L}{r_2} + R_\mathrm{l} C) \pm \sqrt{(\frac{L}{r_2} + R_\mathrm{l} C)^2 - 4LC \cdot \frac{R_\mathrm{l}}{r_2} \cdot (1 + \frac{R_\mathrm{l}}{r_2})}}{2 \cdot L \cdot C \cdot \frac{R_\mathrm{l}}{r_2}} \right| \tag{7.25}$$

This results in a low frequency and a high frequency pole. To estimate the minimum frequency of the high-frequency pole, the discriminant D is set equal to zero ($D = 0$).

$$|s_{\infty,\mathrm{min}}| = \left| \frac{r_2}{L} = \frac{R_\mathrm{BCM} \cdot (1 - M)}{L} = \frac{2}{T_\mathrm{s}} \right| \tag{7.26}$$

Consequently, this is a non-resonant system. The low-frequency pole is caused by the capacitance and the high-frequency pole by the inductance. The zero point and the pole caused by the capacitance compensate each other. The result is a slight curvature of the amplitude and phase response (Fig. 7.9).

7.5.2.2 Current to Voltage Transfer Function $G_\mathrm{vi}(s)$

According to the equivalent circuit (Fig. 7.11) the output voltage is determined analogously:

$$\partial V_\mathrm{LV} = G_\mathrm{id}(s) \cdot \partial d \cdot \underbrace{\left((R_\mathrm{C} + \frac{1}{s \cdot C}) || R_\mathrm{l}\right)}_{= G_\mathrm{vi}(s)} \tag{7.27}$$

Equation (7.27) shows that the ratio of the output voltage to the output current $G_\mathrm{vi}(s)$ is identical for CCM and DCM, when the DC-DC converter operates in the buck mode.

7.5.2.3 Duty Cycle to Voltage Transfer Function $G_\mathrm{vd}(s)$

Multiplying the equations (7.27) and (7.20) results in the duty cycle to voltage transfer function relevant for voltage control:

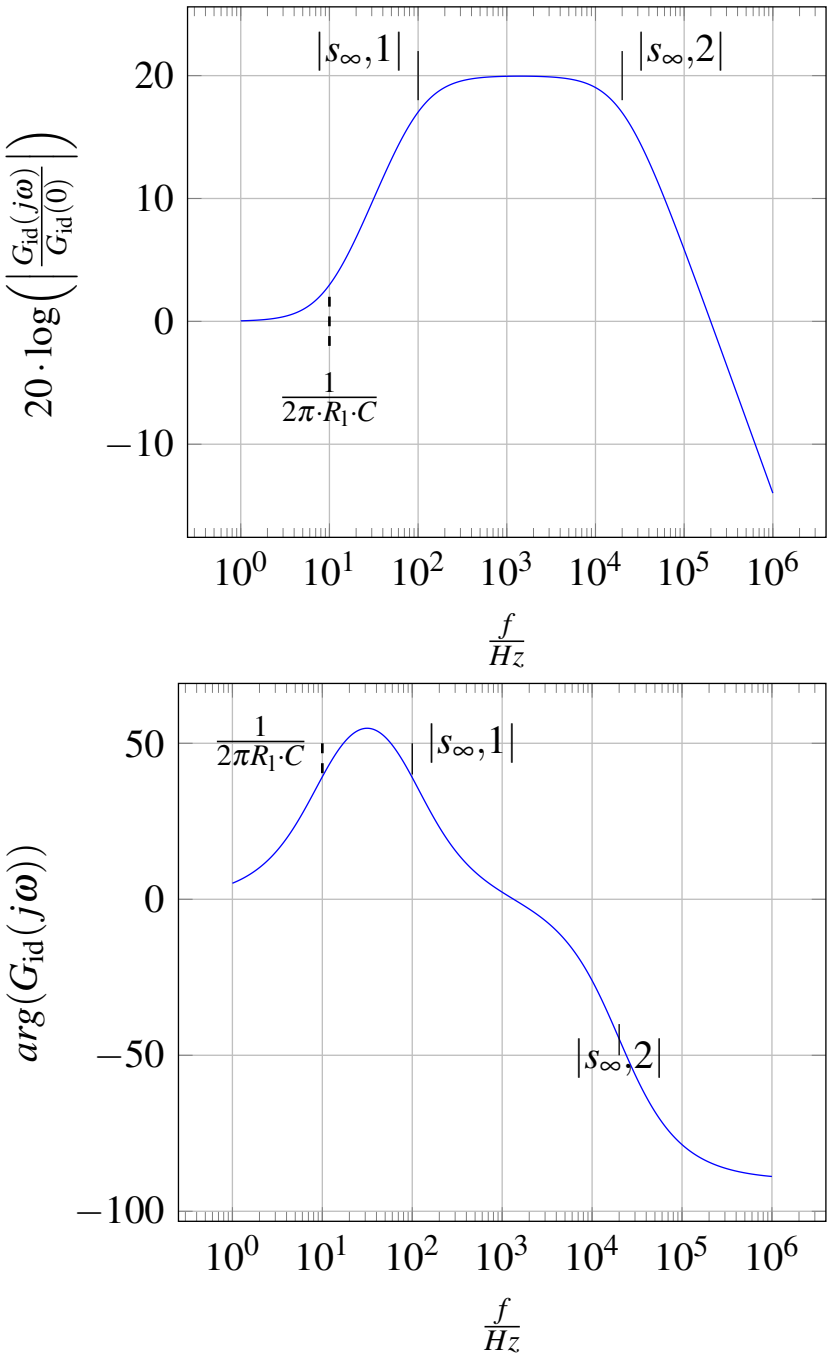


Figure 7.12: Bode plots of the derived, calculated duty cycle to current transfer function $G_{id}(s)$ (Equ. (7.22)) in DCM. Equation (7.25) gives the definition of the poles.

$$G_{\mathrm{vd}}(s) = \frac{1 + s \cdot R_{\mathrm{C}} \cdot C}{(1 + \frac{R_{\mathrm{l}}}{r_2}) + s \cdot \left(\frac{L}{r_2} + (R_{\mathrm{l}} + R_{\mathrm{C}}) \cdot C + \frac{R_{\mathrm{l}} \cdot R_{\mathrm{C}} \cdot C}{r_2} \right) + s^2 \cdot LC \cdot \left(\frac{R_{\mathrm{C}} + R_{\mathrm{l}}}{r_2} \right)} \cdot j_2 \tag{7.28}$$

$$\approx \frac{1 + s \cdot R_{\mathrm{C}} \cdot C}{\left(1 + \frac{R_{\mathrm{l}}}{r_2}\right) + s \cdot (\frac{L}{r_2} + R_{\mathrm{l}} C) + s^2 \cdot \left(LC \cdot \frac{R_{\mathrm{l}}}{r_2} \right)} \cdot j_2$$

7.6 Boost Mode of the Bidirectional DC-DC Converter

When the batteries are discharged, it is necessary to convert the lower terminal voltage to the higher DC power line voltage V_{HV}. For this purpose, the bidirectional DC-DC converter operates in boost mode (Fig. 7.13).

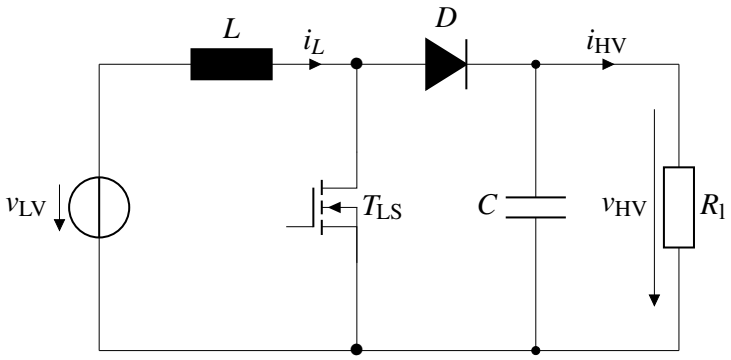


Figure 7.13: Ideal boost converter, where the input capacitor is assumed to be lossfree and is replaced by an ideal voltage source. [356]

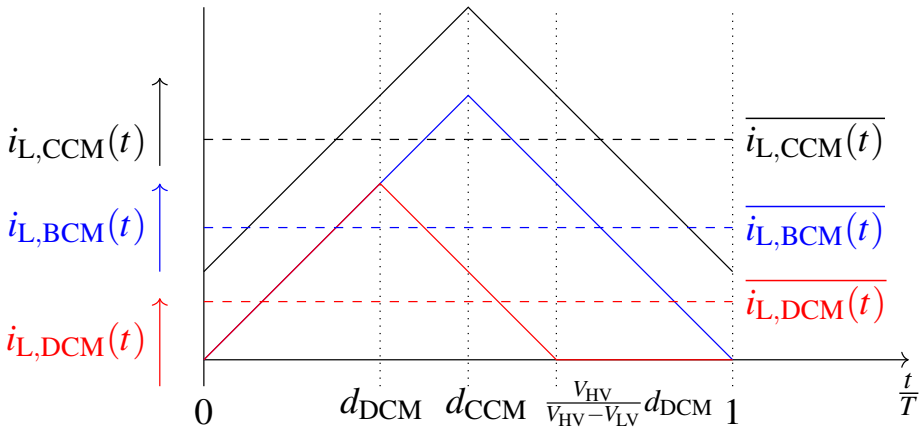


Figure 7.14: Waveforms of the inductor currents in continuous conduction mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM), where d_{CCM} and d_{DCM} are the duty cycles which determine the on-times of the switches.

The static transmission behavior of the boost converter in CCM (Fig 7.14) is defined as:

$$\frac{V_{\mathrm{HV}}}{V_{\mathrm{LV}}} = \frac{1}{1 - d} \tag{7.29}$$

The tranistor T_{LV} is driven by a PWM signal with the period T_{s} and the duty cycle d. The average value of the current through the inductor I_{L} is:

$$I_{\mathrm{L}} = \frac{I_{\mathrm{HV}}}{(1-d)} \tag{7.30}$$

For the current at the boundary to DCM operation I_{BCM} the following applies:

$$\begin{aligned} I_{\mathrm{BCM}} &= \frac{\Delta I_{\mathrm{L}} \cdot (1-d)}{2} = \frac{(1-d)\cdot(V_{\mathrm{LV}})\cdot d \cdot T_s}{2\cdot L} \\ &= -\frac{(V_{\mathrm{LV}} - V_{\mathrm{HV}})\cdot(1-d)^2 \cdot T_s}{2\cdot L} \end{aligned} \tag{7.31}$$

7.6.1 Small-Signal Model and Transfer Function for Boost Mode in CCM

The small-signal model and the derived transfer functions are determined according to the circuit averaging method for the boost mode in CCM [356, pp. 547-585], [382, pp. 1414-1419]. The equivalent circuit of the bidirectional DC-DC converter in boost mode and in CCM is the basis for the analysis (Fig. 7.15).

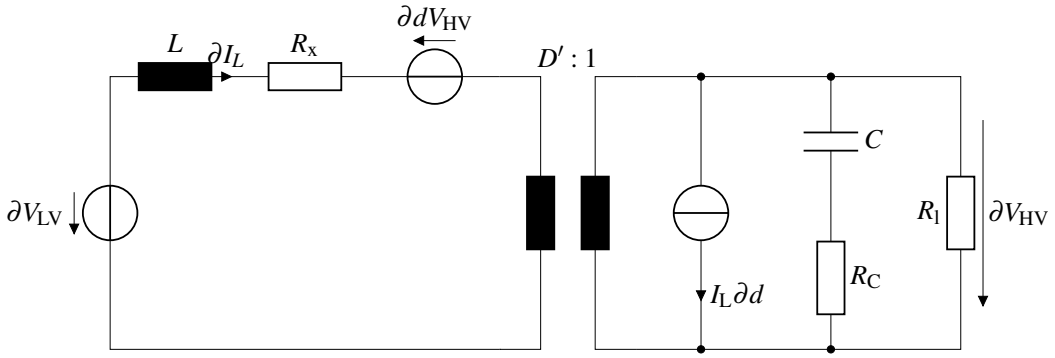


Figure 7.15: Small-signal equivalent circuit of the DC-DC converter in boost mode and in CCM, whereby $D' = (1-d)$. [356]

7.6.1.1 Current to Output Transfer Function $G_{\mathrm{id}}(s)$

The current transfer function is determined according to common methods of network analysis and after further conversions results in:

$$\begin{aligned} G_{\mathrm{id}}(s) &= \frac{\partial I_L(s)}{\partial d} = \frac{(\frac{1}{R_{\mathrm{l}}} + s\cdot C)\cdot V_{\mathrm{HV}} + (1-d)\cdot I_{\mathrm{LV}}}{(\frac{1}{R_{\mathrm{l}}} + s\cdot C)\cdot(s\cdot L + R_{\mathrm{x}}) + (1-d)^2} \\ &= \frac{2V_{\mathrm{HV}}}{R_{\mathrm{l}}} \cdot \frac{s\cdot C\cdot\frac{R_{\mathrm{l}}}{2} + 1}{\left(\frac{R_{\mathrm{x}}}{R_{\mathrm{l}}} + (1-d)^2\right) + s\cdot\left(C\cdot R_{\mathrm{x}} + \frac{L}{R_{\mathrm{l}}}\right) + s^2\cdot L\cdot C} \end{aligned} \tag{7.32}$$

The transfer function has a zero point

$$|s_{0,1}| = \left|\frac{2}{R_{\mathrm{l}}\cdot C}\right| \tag{7.33}$$

and a conjugate complex pole point:

$$|s_{\infty,1,2}| = \left| \frac{1}{2 \cdot R_\mathrm{l} \cdot C} \pm \frac{\sqrt{\left(\frac{L}{R_\mathrm{l}}\right)^2 - 4 \cdot LC \cdot (1-d)^2}}{2 \cdot L \cdot C} \right| \tag{7.34}$$
$$= \left| \frac{1}{2 \cdot R_\mathrm{l} \cdot C} \pm \frac{\sqrt{1 - \frac{4 \cdot C \cdot {R_\mathrm{l}}^2 \cdot (1-d)^2}{L}}}{2 \cdot L \cdot C} \right|$$

For very high frequencies, the lower order terms in the numerator and denominator in equation (7.32) are negligible and the following applies to the current transfer function:

$$G_{\mathrm{id,hf}}(s) = \frac{1}{sL} \tag{7.35}$$

At low frequencies, the current transfer function yields the following steady-state gain:

$$G_{\mathrm{id,lf}}(s) \approx \frac{2 \cdot V_\mathrm{HV}^2}{R_\mathrm{l} \cdot V_\mathrm{LV}^2} \tag{7.36}$$

If the current transfer function G_{id} is Approximated (A) ($G_{\mathrm{id,A}}(s)$) by the steady-state gain and the high-frequency response, the current duty cycle transfer function is:

$$G_{\mathrm{id,A}}(s) = \frac{2 \cdot V_\mathrm{HV}^2}{R_\mathrm{l} \cdot V_\mathrm{LV}^2} \cdot \frac{1}{1 + s \cdot L \cdot \frac{2 \cdot V_\mathrm{HV}^2}{R_\mathrm{l} \cdot V_\mathrm{LV}^2}} \tag{7.37}$$

Figure 7.16 shows the bode plots of the exact$G_{\mathrm{id}}(s)$ and approximated $G_{\mathrm{id,A}}(s)$ duty cycle to current transfer function.

7.6.1.2 Duty Cycle to Voltage Transfer Function $G_{\mathrm{vd}}(s)$

The determination of the duty cycle to voltage transfer function is obtained according to the circuit averaging technique with the equivalent circuit shown in Fig. 7.15. The network analysis provides the transfer function:

$$G_{\mathrm{vd}}(s) = \frac{V_\mathrm{HV}}{R_\mathrm{l}} \cdot \tag{7.38}$$
$$\cdot \frac{\left(1 - \frac{s \cdot L - R_\mathrm{x}}{(1-d)^2 \cdot R_\mathrm{l}}\right) \cdot (1 + s \cdot C \cdot R_\mathrm{C})}{R_\mathrm{x} + (1-d)^2 \cdot R_\mathrm{l} + s(L + C \cdot R_\mathrm{x} \cdot R_\mathrm{C} + C \cdot R_\mathrm{C} \cdot R_\mathrm{l} \cdot (1-d)^2) + s^2 \cdot L \cdot C \cdot R_\mathrm{l}}$$

Due to the small contribution of R_x, it can be neglected without a significant deviation and the transfer function is reduced to the following equation:

$$G_{\mathrm{vd}}(s) \approx \frac{V_\mathrm{HV}}{(1-d)^2} \cdot \frac{\left(1 - \frac{s \cdot L}{(1-d)^2 \cdot R_\mathrm{l}}\right) \cdot (1 + s \cdot C \cdot R_\mathrm{C})}{1 + s \cdot \left(\frac{L}{R_\mathrm{l} \cdot (1-d)^2} + R_\mathrm{C} \cdot C\right) + s^2 \cdot \frac{L \cdot C}{(1-d)^2}} \tag{7.39}$$

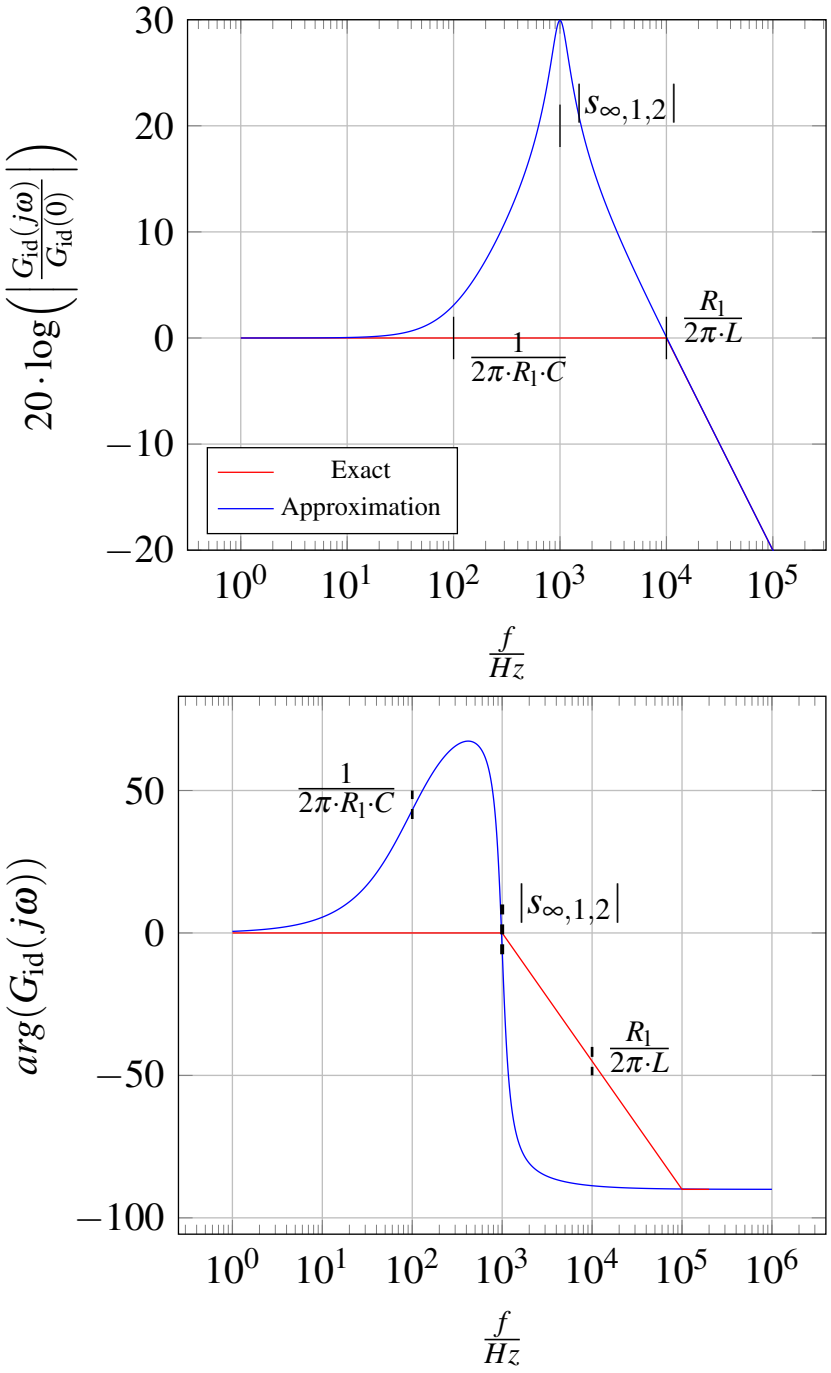


Figure 7.16: Bode plots of the exact (Equ. 7.32) and approximated (Equ. 7.37) calculated current transfer functions $G_{id}(s)$. The exact one considers high frequency behavior. The straight lines are approximations.

Table 7.2: Specification of the equivalent circuit elements. d is the duty cycle of the transistor, T_s is the period, and V is the small-signal voltage change [356].

g_1	j_1	r_1	g_2	j_2	r_2	$M = \frac{V_{HV}}{V_{LV}}$	R_e
$-\frac{1}{(M-1)^2 \cdot R_e}$	$\frac{2 \cdot M \cdot V}{d \cdot (M-1) \cdot R_e}$	$\frac{(M-1)^2}{M^2} \cdot R_e$	$\frac{2 \cdot M - 1}{(M-1)^2 \cdot R_e}$	$\frac{2 \cdot V}{d \cdot (M-1) \cdot R_e}$	$(M-1)^2 R_e$	$\frac{1+\sqrt{1+4 \cdot \frac{R_e}{R}}}{2}$	$\frac{2 \cdot L}{d^2 \cdot T_s}$

7.6.1.3 Current to Voltage Transfer Function $G_{vi}(s)$

From the equations (7.32) and (7.39), the current to voltage transfer function (Fig. 7.17) relevant for the current control can be derived:

$$G_{vi}(s) = \frac{R_l}{2} \cdot \frac{V_{LV}}{V_{HV}} \cdot \left(1 - s \cdot \frac{L}{R_l \cdot (1-D)^2}\right) \cdot \frac{1 + s \cdot R_C \cdot C}{1 + s \cdot \frac{R_l \cdot C}{2}} \tag{7.40}$$

7.6.2 Small-Signal Model and Transfer Function for Boost Mode in DCM

The observation of the bidirectional DC-DC converter in boost mode and DCM and the derivation of the transfer functions is based on the corresponding averaging equivalent circuit (Fig. 7.18).

7.6.2.1 Current to Output Transfer Function $G_{id}(s)$

To determine the current to output transfer function $G_{id}(s)$ ($\partial V_{LV} = 0$), the equivalent circuit is further simplified (Fig. 7.19).
According the averaging equivalent circuit and network analysis, the current to output transfer function (Fig. 7.20) results in:

$$G_{id}(s) = \frac{1}{1 + s \cdot \frac{L}{r_1}} \cdot j_1 \tag{7.41}$$

From a control perspective, this is a PT1 element with the following pole position:

$$s_\infty = \frac{r_1}{L} \tag{7.42}$$

7.6.2.2 Duty Cycle to Voltage Transfer Function $G_{vd}(s)$

In order to determine the current to voltage transfer function relevant for the current control, the duty cycle to voltage transfer function $G_{vd}(s)$ is required. The output voltage ∂V_{HV} can be determined by the following equation:

$$\partial V_{HV} = \left(r_2 || (R_C + \frac{1}{s \cdot C}) || R_l\right) \cdot (g_2 \cdot \partial V + j_2 \cdot \partial d) \tag{7.43}$$

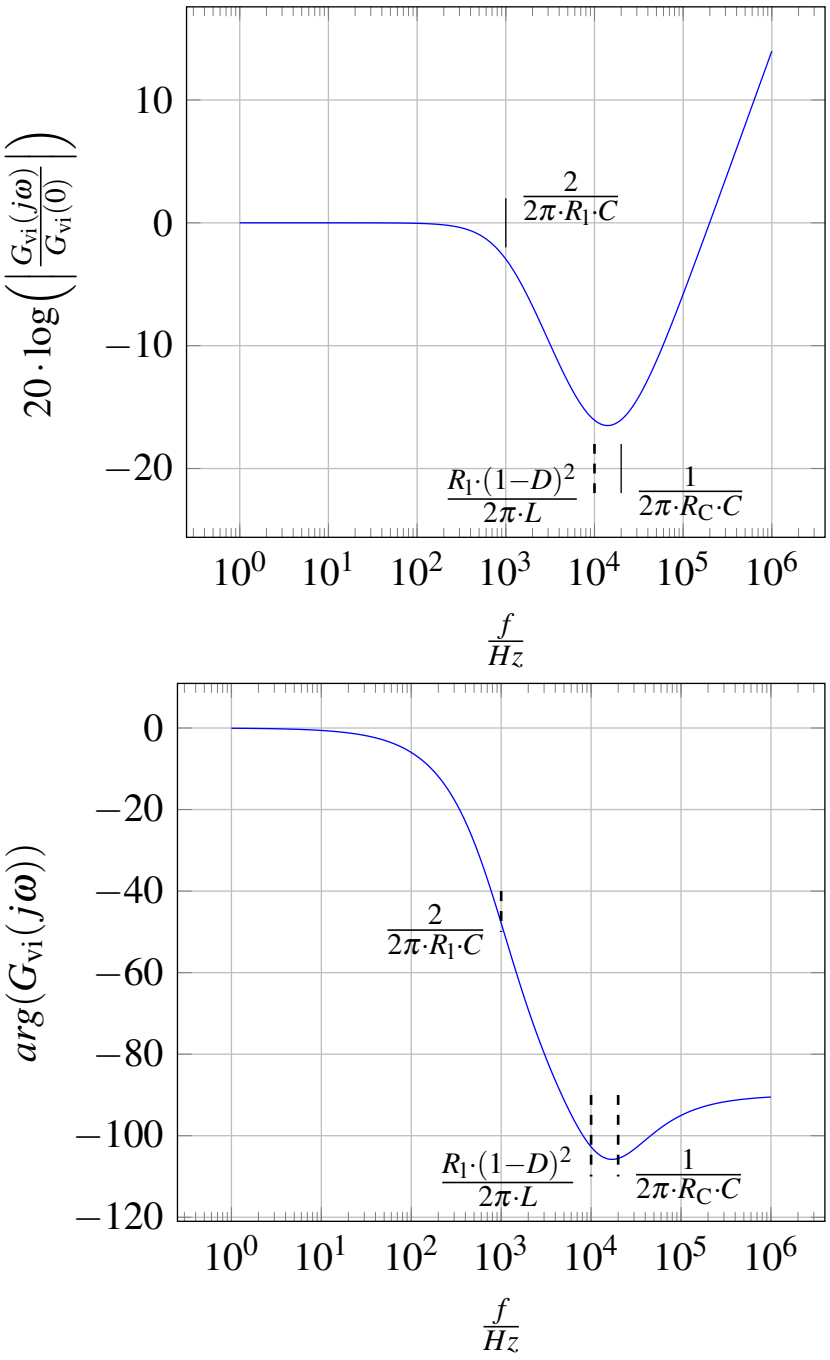


Figure 7.17: Bode plots of the current to voltage transfer function $G_{vi}(s)$ (Equ. (7.40)). The straight lines are approximations.

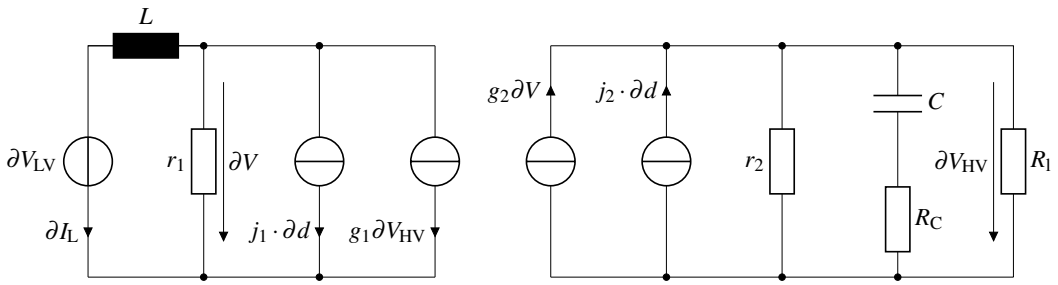


Figure 7.18: Small-signal equivalent circuit of the bidirectional DC-DC converter in boost mode and DCM. The values of the equivalent circuit elements are defined in Table 7.2. [356]

where ∂V can be represented as a function of ∂d:

$$\partial V = -\frac{s \cdot r_1 \cdot L}{r_1 + s \cdot L} \cdot j_1 \cdot \partial d \tag{7.44}$$

Substituting the equation (7.44) into equation (7.43) and replacing j_1 and j_2 with the equations specified in Table 7.2 results in the duty cycle to voltage transfer function:

$$\begin{aligned} G_{\mathrm{vd}}(s) = \frac{\partial V_{\mathrm{HV}}}{\partial d} &= \left(r_2 || (R_{\mathrm{C}} + \frac{1}{s \cdot C}) || R_{\mathrm{l}}\right) \cdot \frac{2V}{d \cdot (M-1) \cdot R_e} \cdot \left(M - \frac{s \cdot r_1 \cdot g_2 \cdot L}{r_1 + s \cdot L}\right) \\ &= \frac{2 \cdot V \cdot r_2 \cdot R_{\mathrm{l}}}{d \cdot (M-1) \cdot R_{\mathrm{e}}} \cdot \left(M - \frac{s \cdot g_2 \cdot L}{1 + s \cdot \frac{L}{r_1}}\right) \cdot \frac{1 + s \cdot R_{\mathrm{C}} \cdot C}{(r_2 + R_{\mathrm{l}}) + s \cdot C \cdot (r_2 \cdot R_{\mathrm{l}} + r_2 \cdot R_{\mathrm{C}} + R_{\mathrm{l}} \cdot R_{\mathrm{C}})} \end{aligned} \tag{7.45}$$

Inserting the equivalent circuit elements g_2, r_1 and R_e (Tab. 7.2) and further transformations gives the following:

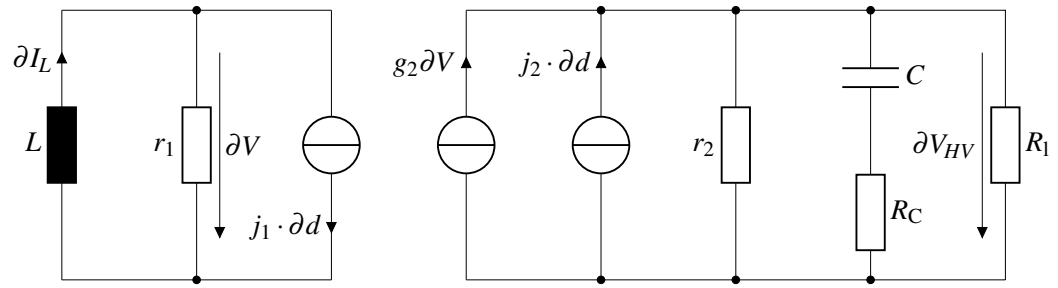


Figure 7.19: Simplified small-signal equivalent circuit for the analysis of the current to output behavior in boost mode and DCM. [356]

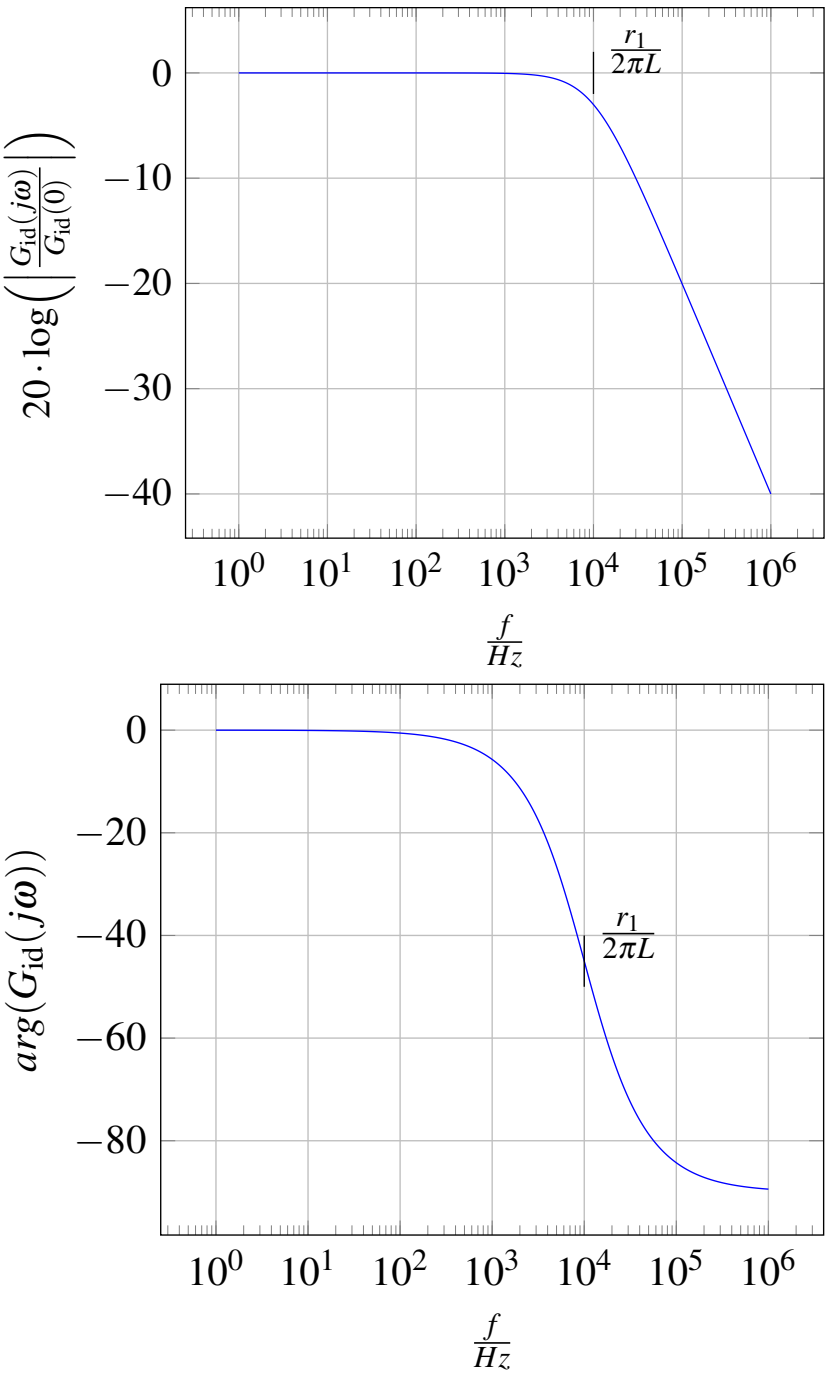


Figure 7.20: Bode plots of the duty cycle to current transfer function $G_{id}(s)$ (Equ. (7.41)) in DCM. The straight lines are approximations.

$$
\begin{aligned}
G_{\mathrm{vd}}(s) &= \frac{2\cdot V\cdot r_2\cdot R_\mathrm{l}}{d\cdot(M-1)\cdot R_\mathrm{e}}\cdot\frac{1+s\cdot L\cdot(\frac{1}{r_1}-M\cdot g_2)}{1+s\frac{L}{r_1}}\cdot \\
&\cdot\frac{1+s\cdot R_\mathrm{C}\cdot C}{(r_2+R_\mathrm{l})+s\cdot C\cdot(r_2\cdot R_\mathrm{l}+r_2\cdot R_\mathrm{C}+R_\mathrm{l}\cdot R_\mathrm{C})} \\
&= \frac{2\cdot V\cdot r_2\cdot R_\mathrm{l}}{d\cdot(M-1)\cdot R_\mathrm{e}}\cdot\frac{1-s\cdot\frac{M\cdot d^2\cdot T_\mathrm{s}}{2\cdot(M-1)}}{1+s\cdot\frac{L}{r_1}}\cdot \\
&\cdot\frac{1+s\cdot R_\mathrm{C}\cdot C}{(r_2+R_\mathrm{l})+sC\cdot(r_2\cdot R_\mathrm{l}+r_2\cdot R_\mathrm{C}+R_\mathrm{l}\cdot R_\mathrm{C})}
\end{aligned}
\tag{7.46}
$$

The transfer function has a Right Half Plane Zero (RHPZ) with the following time constant T_{RHPZ}.

$$
T_{\mathrm{RHPZ}} = \frac{M\cdot d^2\cdot T_\mathrm{s}}{(M-1)\cdot 2} \tag{7.47}
$$

The maximum duty cycle value achieved in DCM mode corresponds to the value in CCM and is defined as:

$$
d_{\max} = \frac{M-1}{M} \tag{7.48}
$$

The minimum frequency of the RHPZ is thus:

$$
f_{\mathrm{RHPZ,min}} = \frac{f_\mathrm{s}}{\pi} \tag{7.49}
$$

The minimum frequency is in the range of the switching frequency and can be neglected in further considerations. The transfer function has the following zero point

$$
|s_{0,1}| = \left|\frac{1}{R_\mathrm{C}\cdot C}\right| \tag{7.50}
$$

and a pole point defined as:

$$
|s_{\infty,1}| = \left|\frac{r_2+R_\mathrm{l}}{C\cdot(r_2\cdot R_\mathrm{l}+r_2\cdot R_\mathrm{C}+R_\mathrm{l}\cdot R_\mathrm{C})}\right| \tag{7.51}
$$

The definition of the pole is simplified with the assumption: $r_2\cdot R_\mathrm{C}\approx R_\mathrm{l}\cdot R_\mathrm{C}\ll r_2\cdot R$. Following, the pole is defined as:

$$
|s_{\infty,1}| = \left|\frac{1}{C\cdot(r_2||R_\mathrm{l})}\right| \tag{7.52}
$$

The simplified duty cycle to voltage transfer function is given:

$$
G_{\mathrm{vd}}(s) = \frac{\partial V_{\mathrm{HV}}}{\partial d} = \frac{2\cdot V\cdot(r_2||R_\mathrm{l})}{d\cdot(M-1)\cdot R_\mathrm{e}}\cdot\frac{1}{2\cdot(M-1)}\cdot\frac{1}{1+s\cdot\frac{L}{r_1}}\cdot\frac{1+s\cdot R_\mathrm{C}\cdot C}{1+s\cdot C\cdot(r_2||R_\mathrm{l})} \tag{7.53}
$$

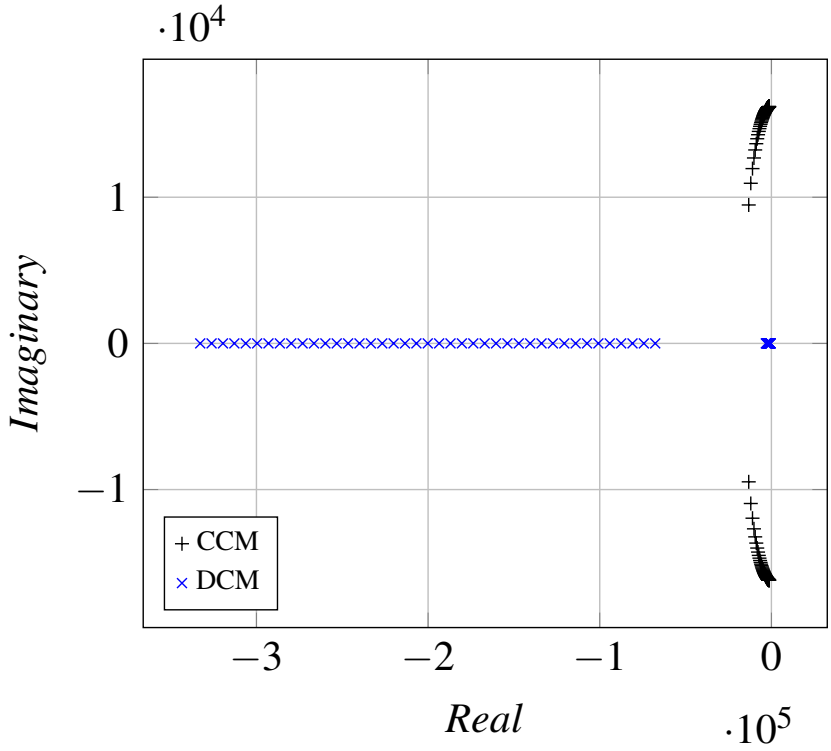


Figure 7.21: Calculated poles of the duty cycle to transfer functions in DCM (marked blue) and CCM (marked black).

7.6.2.3 Current to Voltage Transfer Function $G_{\mathrm{vi}}(s)$

The current to voltage transfer function is determined by the equations (7.53) and (7.41), whereby j_1 was replaced according to the value specified in Tab. 7.2.

$$G_{\mathrm{vi}}(s) = \left.\frac{\partial I}{\partial d}\right|_{\partial V_{\mathrm{HV}}=0} = \frac{G_{\mathrm{vd}}(s)}{G_{\mathrm{id}}(s)} = \frac{(r_2||R_1)}{M} \cdot \frac{1+s\cdot R_{\mathrm{C}}\cdot C}{1+s\cdot C\cdot(r_2||R_1)} \tag{7.54}$$

7.7 Poles and Zeros Consideration

The poles of the duty to current transfer function differ significantly in CCM and DCM operation in buck mode (Fig. 7.21, Tab. 7.3). The poles in CCM mode tend towards the imaginary axis with an increasing resistance. The zeros of the transfer function do not change with the change of the operation mode from CCM to DCM in buck mode. In the case of the boost converter, the change to DCM mode results in significant advantages in terms of control. The RHPZ is high frequent in DCM and therefore does not affect the control behavior. The duty to current transfer function is reduced to a PT1 element with a high-frequency pole, which shows significant advantages in terms of control complexity.

7.8 Summary

The small-signal behavior of a bidirectional half-bridge DC-DC converter in buck and boost modes was analyzed in this chapter using the averaging technique. The averaged equivalent circuit diagrams were used to comprehensibly derive the transfer functions relevant to voltage and average current control, including the current to

voltage transfer functions. The poles and zeros of the buck and boost modes, each considering the CCM and DCM, were listed comparatively and form the basis for the analysis of the overall control structure and the design of the corresponding controller approaches.

Table 7.3: Poles and zeroes of the transfer functions for CCM and DCM in buck [383] and in boost [384] mode of a bidirectional DC-DC converter.

	Boost CCM		**Boost DCM**	
Transfer Function	Poles	Zeroes	Poles	Zeroes
$G_{\mathrm{id}}(s)$	$\lvert s_{\infty,1,2}\rvert = \frac{1}{2\cdot R_{\mathrm{l}}\cdot C}\pm \pm\frac{\sqrt{1-\frac{4\cdot C\cdot {R_{\mathrm{l}}}^2\cdot(1-d)^2}{L}}}{2\cdot L\cdot C}$	$\lvert s_{0,1}\rvert = \frac{2}{R_{\mathrm{l}}\cdot C}$	$\lvert s_{\infty}\rvert = \frac{r_{\mathrm{l}}}{L}$	—
$G_{\mathrm{vi}}(s)$	$\lvert s_{\infty,1}\rvert = \frac{2}{R_{\mathrm{l}}\cdot C}$	$\lvert s_{0,1}\rvert = \frac{R_{\mathrm{l}}(1-d)^2}{L}$ $\lvert s_{0,2}\rvert = \frac{1}{R_{\mathrm{C}}\cdot C}$	$\lvert s_{\infty,1}\rvert = \frac{1}{C(r_2 \lvert\rvert R_{\mathrm{l}})}$	$\lvert s_{0,1}\rvert = \frac{(M-1)\cdot 2}{M\cdot d^2\cdot T_{\mathrm{s}}}$ $\lvert s_{0,2}\rvert = \frac{1}{R_{\mathrm{C}}\cdot C}$
	Buck CCM		**Buck DCM**	
Transfer Function	Poles	Zeroes	Poles	Zeroes
$G_{\mathrm{id}}(s)$	$\lvert s_{\infty,1,2}\rvert = \lvert\frac{\pm\sqrt{1-4\frac{C}{L}{R_{\mathrm{l}}}^2}-1}{2\cdot R_{\mathrm{l}}\cdot C}\rvert$	$\lvert s_0\rvert = \frac{1}{R_{\mathrm{l}}\cdot C}$	$\lvert s_{\infty,1,2}\rvert = \frac{(\frac{L}{r_2}+R_{\mathrm{l}}C)\pm\sqrt{(\frac{L}{r_2}+R_{\mathrm{l}}C)^2-4LC\frac{R_{\mathrm{l}}}{r_2}(1+\frac{R_{\mathrm{l}}}{r_2})}}{2\cdot L\cdot C\cdot\frac{R_{\mathrm{l}}}{r_2}}$	$\lvert s_{0,1}\rvert = \frac{1}{R_{\mathrm{l}}\cdot C}$
$G_{\mathrm{vi}}(s)$	$\lvert s_{\infty,1}\rvert = \frac{1}{R_{\mathrm{l}}\cdot C}$	$\lvert s_{0,1}\rvert = \frac{1}{R_{\mathrm{C}}\cdot C}$	$\lvert s_{\infty,1}\rvert = \frac{1}{R_{\mathrm{l}}\cdot C}$	$\lvert s_{0,1}\rvert = \frac{1}{R_{\mathrm{C}}\cdot C}$

8

Hardware and Software-based Implementation of the Average Current Mode Control with Outer Voltage Control of the Bidirectional DC-DC Converter

For safe operation of heterogeneous batteries combined in one system, it is necessary to limit the (dis)charge current depending on various, variable operating factors, such as temperature, state of charge and state of health. Additionally, it is necessary to convert the different battery terminal voltages to a common DC line voltage level. The bidirectional DC-DC converter realizes a power flow in charge and discharge direction. The heterogeneity of the system and the chosen architecture result in special requirements for the DC-DC converter and its control. To support different batteries, a variable and wide voltage range at the low voltage side and adjustable (dis)charge current limitation are essential. The (dis)charge current limit must be adjustable during active operation for safe battery operation, For a variety of different applications, an adjustable voltage at the high voltage side is required. Accurate current and voltage control in buck mode for step down and boost mode for step up, as well as in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) (Fig. 8.1), is demanded for stable system operation.
The following chapter first describes basic approaches to control DC-DC converters. Subsequently, the selection of the control method is justified and the development of the current and voltage controllers is presented. The hardware- and software-based controller implementations are described and their advantages and disadvantages are discussed. The phase and amplitude responses are determined for buck and boost in the CCM and DCM, respectively. Finally, the calculated phase and amplitude

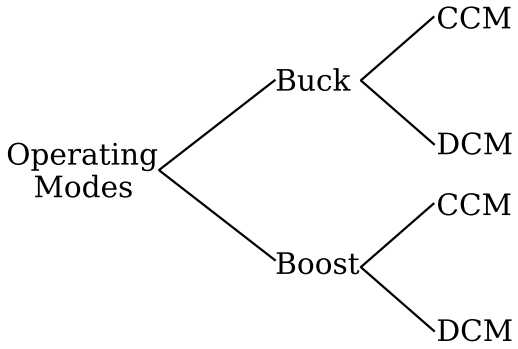


Figure 8.1: Overview of the operating modes of the bidirectional DC-DC converter.

responses are compared with those measured in hardware. For this purpose, the phase and amplitude responses of the hardware implementation of the bidirectional DC-DC converter are measured using the analog, harware-based and the digital, software-based controller implementation.

8.1 Motivation

Battery systems significantly support renewable energy integration and contribute to cleaner and more efficient energy systems. They are used to power portable devices, to store energy for backup power systems, to provide intermediate storage for grid stabilization and in off-grid micro-grids and to supply electric vehicles. Ongoing research and development is focused on improving battery capacity, efficiency, lifetime, environmental impact, safety and cost through variation of electrodes, electrolyte and separator materials. Different battery cell chemistries thereby exhibit varying characteristics in terms of permissible operating temperature range, maximum load current, available capacity and terminal voltage.
Decentralized heterogeneous battery systems allow the combination of several batteries with varying chemical compositions and resulting different properties, such as fast charging capability or high temperature use. They also enable the integration of second life batteries. These batteries already have a reduced capacity and lower state of health as well as increased internal resistance due to initial use, for example in an electric vehicle. As a result, the dynamic response of these batteries, i.e. rapid (dis)charge of high load currents, is lower. In applications with lower requirements in terms of dynamics, such as in home storage systems, they can still be used reasonably with a limited operating range. The integration of second life batteries is helpful to counteract the too low storage capacity for area-wide integration of renewable energies and to extend the service life of the batteries, thus delaying the costly recycling process and improving the environmental impact of the batteries.
Applications such as grid-connected intermediate storage require high system availability and reliability. Decentralized architectures are characterized by distributed nodes that operate locally and independently of each other and are functionally identical. In contrast to centralized or hierarchical architectures, they reduce the probability of single point of failures due to the functional equivalence of the individual nodes and the associated redundancy. Furthermore, decentralized architectures are characterized by increased flexibility through scalability and

reconfigurability. Batteries of different chemistry or capacity can be added or removed according to the requirements of the application. Leveraging the strengths of different battery technologies, such as high energy density lithium-ion batteries and high power density lead-acid batteries, offers the potential to optimize system efficiency. Selecting appropriate batteries based on application requirements enables achieving the optimum combination of energy density, power density, lifetime, cost efficiency, and system efficiency. To ensure that each battery is used according to its intended purpose, specific control and power electronics requirements arise. Bidirectional DC-DC converters are required to achieve voltage compatibility for batteries connected in parallel with different, variable and state of charge dependent terminal voltages. They have to be able to handle the different input voltage ranges and provide the required output voltage levels for the connected loads. During the charge of the batteries, it is necessary to convert the output voltage level of the generators to the different terminal voltages of the batteries. The control objective hereby is to maintain the DC link voltage at the set point regardless of the actual load and generation power. This requires voltage control in buck and boost mode.
The bidirectional DC-DC converter under investigation offers the following features:

- low voltage range from 0 V to 15 V,
- high voltage range from 18 V to 48 V,
- current range from 0 A to 13 A (analog) or 0 A to 40 A (digital),
- fixed switching frequency and
- hard commutation.

For safe operation of the batteries, it is necessary to limit the (dis)charge current depending on various variable operating factors such as temperature, state of charge and state of health. The DC-DC converter must provide a (dis)charge current limit that can be adjusted during active operation as a basis for safe battery operation. Furthermore, it is necessary to distribute the total load current among the available and usable batteries based on their state to prevent overload of individual ones. This requires accurate current control.
The requirements for the DC-DC converters and their control can be summarized as follows:

- variable voltage range at the low voltage side
- adjustable voltage at the high voltage side
- adjustable (dis)charge current limitation
- accurate current and voltage control in buck and boost mode

In the following, basic approaches for controlling DC-DC converters are described first. Subsequently, the selection of the control methods is justified and the development of the controllers is presented. The hardware and software-based controller implementations are presented and their advantages and disadvantages are discussed. The phase and amplitude responses of the step response, closed current control loop, current to voltage transfer function ($G_{\mathrm{vi}}(s)$) as well as the open uncontrolled and controlled loop are calculated. For this purpose, the components are dimensioned according to the hardware implementation. The phase and amplitude responses are determined for buck and boost in the CCM and DCM respectively.
Finally, the calculated phase and amplitude responses are compared with hardware measured ones. For this purpose, the phase and amplitude responses of the hardware implementation of the bidirectional DC-DC converter with the analog controller are measured.

8.2 Theoretical Background

The basis for the controller design is the modeling of the DC-DC converter and the derivation of the transfer functions, which is described in detail in Chapter 7. Subsequently, the feedback loop is closed, i.e. the controller type is selected and the controller parameters are dimensioned in a way that the transfer function of the controller ensures stability and the dynamic requirements are met. In the following, different control concepts based on pulse width modulation with fixed switching frequency are briefly presented. The following description of the controller approaches is mainly a brief summary of the description in [385].

8.2.1 Voltage Control

The output voltage of DC-DC converters is generally driven by pulse width modulation and is a function of the uncontrolled input voltage $v_g(t)$, the duty cycle $d(t)$, the load current $i_{load}(t)$ and the real values of the electrical components. The overall control objective is to achieve and maintain a constant output voltage $v(t) = V$, despite fluctuations in $v_g(t)$ and $i_{load}(t)$ and despite variations in the values of the converter circuit elements. In the following, a DC-DC converter with hard commutation is considered.
For the control of DC-DC converters, closed loops are commonly used to precisely control fluctuations in the input voltage and load in the static case and to achieve the required dynamic response in the control process.

8.2.1.1 Direct Duty Cycle Control

In the Direct Duty Cycle Control (DDCC), the output voltage v_{out} is controlled by modifying the duty cycle $d(t)$ (Fig. 8.2). The controller output v_c corresponds to the difference between the setpoint voltage V_{set} and the output voltage v_{out} and is applied to the input of a comparator. The comparator compares the controller output v_c with a sawtooth voltage v_{st} of constant amplitude V_{st} and generates rectangular pulses with a constant period. This PWM signal consequently controls the power transistor.
The main advantage besides the efficient design and analysis of the feedback loop of this control method is the suitability for parallel operation of several DC-DC converters. Nevertheless, a higher-level control is required for uniform load sharing. Otherwise, if the output voltages are not exactly equal, the DC-DC converter with the highest output voltage will take over the required load current.
Disadvantageously in continuous conduction mode, the DDCC is not very effective with oscillatory two-pole filters (L-C circuit at the output) with 180° phase jump at the resonant frequency. Changes in V_{set} or the load must first propagate through these poles to cause the desired output voltage changes, resulting in poor settling time. Compensation is complicated by the fact that loop gain changes with the input voltage. Furthermore, the input voltage change is not directly taken into account. Changes in the input voltage are only compensated with a delay, which requires a higher loop gain to achieve the desired dynamics.[385]

8.2.1.2 Voltage Feedforward Control

A variation of the DDCC is the Voltage Feedforward Control (VFC), which considers the input voltage changes. Compared to the DDCC, the amplitude V_{st} of v_{st} is no

longer constant, but changes proportionally to the input voltage. Advantages of this method include improved control of input voltage changes and a lower loop gain, which is independent of the input voltage. [385]

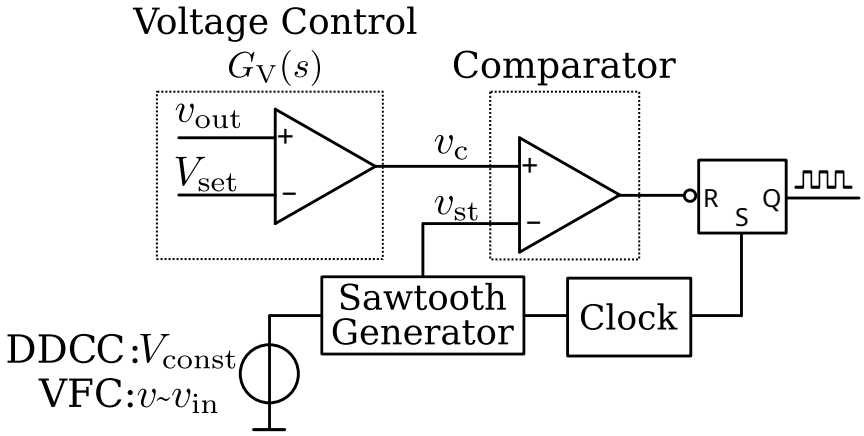


Figure 8.2: Principle of the voltage control approaches direct duty cycle control (DDCC) and voltage feedforward control (VFC). The difference between the setpoint voltage V_{set} and the output voltage v_{out} and the sawtooth voltage v_{st} are the input signals of the comparator, that generates the PWM signal to control the transistor. [385]

8.2.2 Current Control

In the case of a voltage-only control, the voltage deviation directly influences the duty cycle. A cascaded control structure is required for voltage and current control, whereby a subordinate control loop is used for the current control. Since the current also influences the output voltage, the comparator output of the current control readjusts the duty cycle (Fig. 8.3, Fig. 8.4). The setting of the voltage controller based on the voltage control deviation only indirectly influences the duty cycle and forms the setpoint for the subordinate current control loop. The current through the inductor is controlled, whose mean value I_L is equal or proportional to the mean value of the output current I_{out}. This approach exhibits a shorter settling time of the controlled variable in comparison to the DDCC and VFC: The current through the inductor i_L immediately follows an input voltage v_{in} change. Using a voltage control, the effect of the current change on the output voltage v_{out} has to occur before adjusting the control parameters. The disadvantages of the DDCC of slow reactions to input voltage changes and the dependence of the loop gain are significantly reduced by adding the subordinate current control. [385]

8.2.2.1 Peak Current Mode Control

Peak Current Mode Control (PCMC) detects and controls the peak value of the inductor current. The current value is measured via a low impedance shunt resistor. The voltage over the shunt v_{Shunt} replaces the sawtooth voltage of the pure voltage control and is input signal of the comparator (Fig. 8.3). This voltage is compared with the setpoint v_c specified by the voltage controller. If v_{Shunt} is greater than v_c, the latch is deleted, otherwise it is set. If the latch is set, the switch is conductive and the current through the inductance increases. The subordinate current control cancels the pole of the transfer function caused by the inductor and thus reduces the denominator

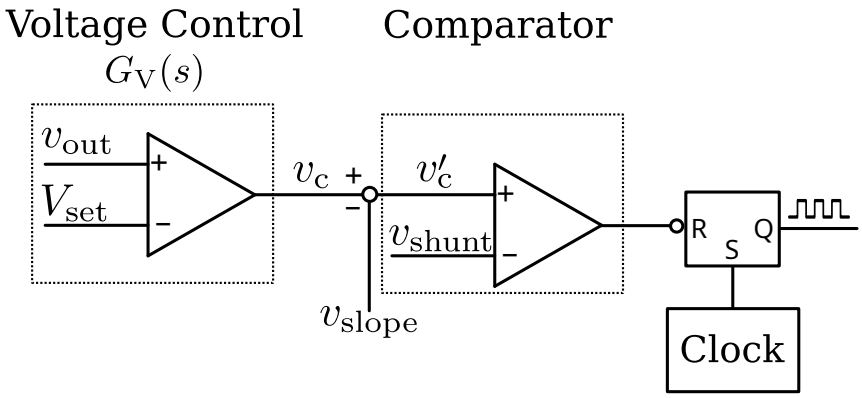


Figure 8.3: Principle of the Peak Current Mode Control (PCMC): The voltage controller output v_c corresponds to the difference between the actual voltage and the setpoint value and is the input signal of the comparator. To account for the current control, the voltage v_{Shunt} is also applied to the input of the comparator. Slope compensation is used to stabilize the current control in case of duty cycles greater than 0.5 for continuous conduction mode. This prevents subharmonic oscillations and consequently spikes in the measured current. [385]

polynomial in continuous operation by one order and the phase rotation of the entire transfer function by 90°. This has a positive effect on the stability characteristics. Gain and bandwidth can be significantly increased compared to voltage only control. In addition, it results in a larger phase margin which makes the entire control more robust against parameter variations, such as age-related changes in the capacitance value or the series equivalent resistance.
With this control approach, the average value of the actual inductor current remains below the specified current setpoint. However, the external voltage control loop compensates for any remaining deviations and the output voltage remains stable. The current, however, is not controlled to an exact value. Another disadvantage is the higher effort in controller design and circuit analysis. Furthermore, the ratio of peak current to average current is in many cases strongly dependent on the duty cycle. Another disadvantage of this method is the sensitivity to measurement inaccuracies as a result of switching peaks. In the moment the switch is closed, current spikes are generated and the voltage v_{Shunt} increases accordingly. As a result, the switch might be directly reset, resulting in a subharmonic operation mode with significantly higher ripples. For applications that require the control of the average current and have lower requirements on the control dynamics, such as battery systems, the average current mode control (ACMC) is recommended. The disadvantages of the PCMC regarding necessary slope compensation, current errors at constant v_c and variable input voltage as well as current control inaccuracies since only the current peak is taken into account are eliminated by the ACMC. [385, 386]

8.2.2.2 Average Current Mode Control

In Average Current Mode Control (ACMC), an integrating current controller is inserted in addition to the voltage controller (Fig. 8.4). Analogous to the previously presented control approaches, the voltage controller determines the difference between the actual output voltage v_{out} and the setpoint V_{set}. This forms the current-proportional setpoint $v_{i,set}$ for the inner current control loop. The current controller

is essentially integrating up to the bend of the PI controller characteristic. It forms the controller output v_c from the difference between $v_{i,set}$ and v_{Shunt}, which is the input signal of the following comparator. The comparator compares v_c with an applied sawtooth voltage of fixed switching frequency and amplitude and generates a corresponding PWM signal for switching the power transistor. The voltage applied to the inductor is controlled according to the switching pattern of the transistor until the value $v_{i,set}$ is set and the requested average current flow is reached.
The ACMC is characterized by high current control accuracy for buck-boost converters even for small currents in discontinuous conduction mode. Furthermore, the voltage loop is not directly affected by the change of the operating mode and both input and output currents of buck-boost converters can be controlled. In contrast to the PCMC, no slope compensation is required. For maintaining the control stability, the loop gain must be limited. Short current spikes that occur during switching operations do not affect the current control or only affect it slightly. The integrating part of the current controller prevents that short current spikes and corresponding changes of the voltage v_{Shunt} directly lead to switching operations of the transistor. In comparison to the PCMC, the ACMC has a lower control dynamic due to the slower, inner current control loop. [385, 386]

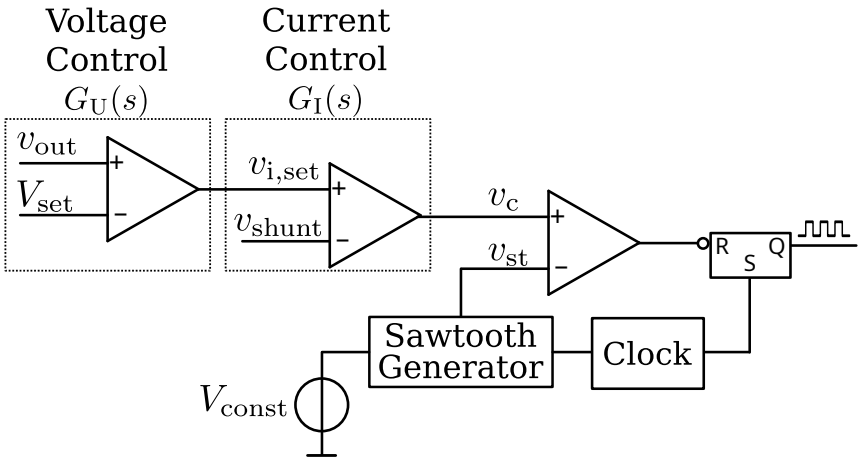


Figure 8.4: Principle of the Average Current Mode Control (ACMC): The voltage controller compares the actual voltage value v_{out} with the setpoint V_{set}. The additional current controller subsequently compares the current-proportional setpoint $v_{i,set}$ with the current voltage across the shunt resistor v_{Shunt} and generates the controller output v_c. The following comparator generates corresponding switching pulses to control the power transistor until v_{Shunt} corresponds to the value $v_{i,set}$ and the required average current value is reached. [385]

8.3 Control Approach Selection for the Bidirectional DC-DC Converter

For the control of the bidirectional DC-DC converter of the decentralized battery management system, a cascaded voltage control with a subordinate current control is implemented. Direct Duty Cycle Control (DDCC) is employed for the voltage control, which is one of the single-loop control approaches. For current control, the two-loop Average Current Mode Control (ACMC) is applied.

8.3.1 Voltage Control Method

With the DDCC, the output voltage is controlled directly by manipulating the duty cycle. Figure 8.5 shows the control loop of the DDCC for the voltage control of the DC-DC converter.

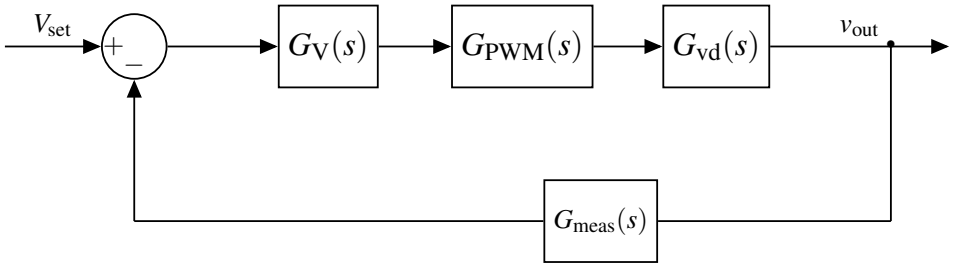


Figure 8.5: Control loop of the Direct Duty Cycle Control (DDCC) for voltage control of the bidirectional DC-DC converter.

The transfer function of the PWM generator corresponds to $G_{PWM}(s)$ and the transfer function of the measurement is described by $G_{meas}(s)$. The transfer function of the voltage controller is represented by $G_V(s)$. The duty cycle to voltage transfer function $G_{vd}(s)$ was determined in the previous Chapter 7 for buck and boost mode as well as for continuous and discontinuous conduction mode respectively. The transfer functions $G_{meas}(s)$ and $G_{PWM}(s)$ do not exhibit a frequency-dependent transfer behavior. Thus, the controller only has to compensate the frequency response of $G_{vd}(s)$.
In order to avoid a stationary control deviation, a pole in zero is used for compensation. For stability this means that the controlled system should not have a phase rotation of more than -90°. With higher phase rotations, it is not possible to achieve satisfactory behavior in terms of control dynamics and transient response. The considered duty cycle to voltage transfer functions, which were previously determined (Chapter 7), have a phase rotation of 180° for buck operation and 270° for boost.
For this reason, special controllers with phase boost have to be implemented. These are characterized by several poles or zeros, which cause a phase boost in a certain range.

8.3.2 Current Control Method

An accurate current control is the basis for the battery state-dependent load sharing between the batteries connected in parallel. The control of the current peaks, as it is the case with the PCMC, is not sufficient for this. Therefore, the ACMC is utilized in the control of the bidirectional DC-DC converter. Unlike the DDCC, which is a voltage-only control, two control loops are used (Fig. 8.6). The inner subordinate loop controls the average current through the inductor. The components of the entire subordinate current control loop with the voltage control loop are shown in figure 8.6. The transfer function of the voltage controller is represented by $G_V(s)$ and the one of the current controller by $G_I(s)$. The transfer function of the PWM generator corresponds to $G_{PWM}(s)$ and the duty cycle to current transfer function is described by $G_{id}(s)$. $G_{vi}(s)$ is the current to voltage transfer function. The feedback block of the inner control loop ($G_{meas}(s)$) corresponds to the amplified (K) voltage across the shunt resistor (R_{Shunt}). A quite small shunt resistor is selected to keep the resulting losses low. In order to generate a reasonable voltage level for the control, an amplifier

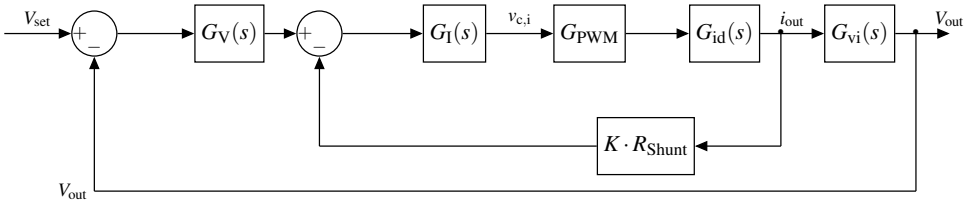


Figure 8.6: Cascaded control loop: For voltage and current control, an outer voltage control loop is placed around the inner current control loop (ACMC). The measured output voltage v_{out} is compared with the setpoint voltage V_{set}. The voltage controller $G_V(s)$ processes the error signal and produces the reference signal $v_{i,set}$ for the current control loop. The reference signal is compared with the voltage across the shunt resistor v_{Shunt}. The current controller processes the error signal and produces the controller output signal v_c, which in turn is used for generating the switching signal.

is required. To prevent the measurement from being falsified by noise influences, an offset voltage is added to the signal.
The closed-loop current control loop is dimensioned in such a way that the transfer function remains constant over a wide frequency range. The crossover frequency of the voltage control loop is thereby significantly lower than the crossover frequency of the current control loop. The current control loop can be assumed to be approximately constant for the dimensioning of the voltage controller.

8.3.3 General Control Design of the Average Current Mode Control with Outer Voltage Control Loop

The cascaded average current mode control is designed as a two-loop structure consisting of an inner current loop and an outer voltage control loop (Figs. 8.6, 8.7). The following is a general description of the controller design which corresponds to a summary of [385, pp. 1297-1310] and [387, pp. 786-799].
First, the inner current control loop is considered in detail with reference to the analog implementation. Subsequently, the design of the current and voltage controller with the help of the small-signal model is discussed in general.

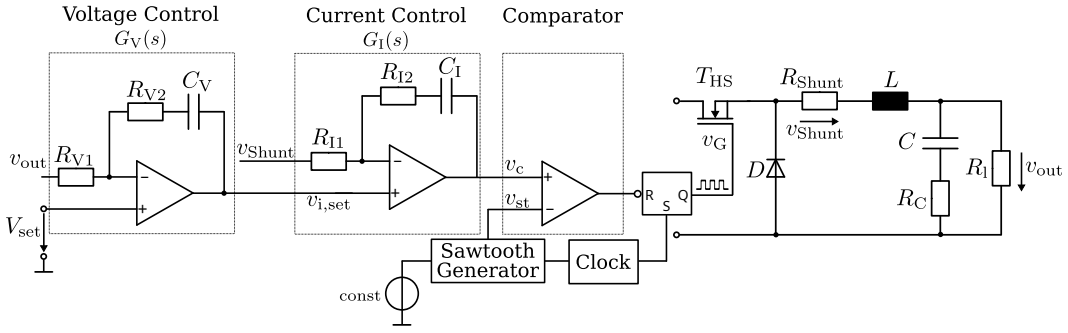


Figure 8.7: Principle circuit diagram of the Average Current Mode Control using hardware based current and voltage controllers. [385]

Inner Current Control Loop

The current through the inductor is measured by a low impedance shunt resistor R_{Shunt}. The current controller amplifies the deviation between the voltage across the

shunt resistor v_{Shunt} and the voltage to specify the set current $v_{\text{i,set}}$ and forms the controller output voltage v_{c}. The subsequent comparator compares the controller output voltage v_{c} with a sawtooth voltage v_{st}. The resulting PWM signal controls the duty cycle of the switching element, which in the case of the buck mode corresponds to the high side MOSFET T_{HS}. The switching times of the MOSFET in turn regulates the voltage across the inductor which changes the current until v_{Shunt} is equal to $v_{\text{i,set}}$. In the static state, the following applies for the current through the inductor ($I_{\text{L,set}}$):

$$I_{\text{L,set}} = \frac{V_{\text{i,set}}}{R_{\text{Shunt}}} \tag{8.1}$$

The voltage across the shunt resistor is:

$$V_{\text{Shunt}} = I_{\text{L}} \cdot R_{\text{Shunt}} \tag{8.2}$$

The output voltage of the DC-DC converter is set via the duty cycle d:

$$V_{\text{out}} = d \cdot V_{\text{in}} = \frac{v_{\text{c}}}{V_{\text{st}}} \cdot V_{\text{in}} \tag{8.3}$$

The transfer function of the current controller is given by:

$$\begin{aligned} G_{\text{I}}(s) &= \frac{v_{\text{c}}(s)}{V_{\text{i,set}} - V_{\text{Shunt}}} = \frac{R_{\text{I2}}}{R_{\text{I1}}} \cdot \left(1 + \frac{1}{R_{\text{I2}} \cdot C_{\text{I}} \cdot s}\right) \\ &= K_{\text{I}} \cdot \left(1 + \frac{1}{T_{\text{I}_\text{z}} \cdot s}\right) \end{aligned} \tag{8.4}$$

The current controller corresponds to a PI controller with the following coefficients:

$$K_{\text{I}} = \frac{R_{\text{I2}}}{R_{\text{I1}}} \tag{8.5}$$

$$T_{\text{I}_\text{z}} = R_{\text{I2}} \cdot C_{\text{I}} \tag{8.6}$$

At constant input voltage V_1, the voltage across the inductor is equal to:

$$V_{\text{e}}(s) = d(s) \cdot V_1 = \frac{v_{\text{c}}(s)}{V_{\text{st}}} \cdot V_1 \tag{8.7}$$

The transfer function of the PWM and the switching element results in:

$$G_2(s) = \frac{V_{\text{e}}(s)}{v_{\text{c}}(s)} = \frac{V_{\text{in}}}{V_{\text{st}}} \tag{8.8}$$

The transfer function between the uncontrolled voltage at the input V_g and the current through the inductor I_L for the L-C filter is given by:

$$G_\mathrm{ig}(s) = \frac{I_\mathrm{L}(s)}{V_\mathrm{g}(s)} = \frac{1}{R_\mathrm{x} + s \cdot L + \frac{R_\mathrm{L} \cdot (R_\mathrm{c} + \frac{1}{s \cdot C})}{R_\mathrm{L} + R_\mathrm{C} + \frac{1}{s \cdot C}}} \tag{8.9}$$

Where R_x corresponds to the series connection of the internal resistance with the resistance of the inductance $R_\mathrm{x} = R_\mathrm{Ind} + R_\mathrm{i}$. According to the general description follows:

$$G_\mathrm{ig}(s) = K_{1,\mathrm{s}} \cdot \frac{1 + s \cdot T_\mathrm{E}}{1 + \frac{2 \cdot D_\mathrm{r}}{\omega_0} \cdot s + \frac{1}{\omega_0^2} \cdot s^2} \tag{8.10}$$

The coefficients follow under the assumption that $R_\mathrm{x}, R_\mathrm{C} \ll R_\mathrm{l}$:

$$K_{1,\mathrm{s}} = \frac{1}{R_\mathrm{l}} \tag{8.11}$$

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}} \tag{8.12}$$

$$\omega_E = \frac{1}{T_\mathrm{E}} = \frac{1}{(R_\mathrm{l} + R_\mathrm{C}) \cdot C} \tag{8.13}$$

$$2 \cdot D_r = \frac{R_\mathrm{C} + R_\mathrm{X} + \frac{L}{C \cdot R_\mathrm{l}}}{\omega_0 \cdot L} \approx \frac{1}{\omega_0 \cdot C \cdot R_\mathrm{l}} \tag{8.14}$$

The gain between the controller output voltage v_c and the current through the inductor I_L for the open loop is defined as:

$$\begin{aligned} G_{\mathrm{I_L,V_c}} &= \frac{\delta I_\mathrm{L}(s)}{\delta v_\mathrm{c}(s)} \\ &= \frac{V_\mathrm{in}}{V_\mathrm{st}} \cdot K_{1,\mathrm{s}} \cdot \frac{1 + s \cdot T_\mathrm{E}}{1 + \frac{2 \cdot D_\mathrm{r}}{\omega_0} \cdot s + \frac{1}{\omega_0^2} \cdot s^2} \end{aligned} \tag{8.15}$$

For the current loop transfer function, in addition to the current controller, the output filter and the PWM and the switching element, the shunt resistor must also be taken into account:

$$\begin{aligned} G_\mathrm{o,i}(s) &= G_\mathrm{I}(s) \cdot G_2(s) \cdot G_\mathrm{ig}(s) \cdot R_\mathrm{Shunt} \\ &= K_\mathrm{I} \cdot \left(1 + \frac{1}{T_{\mathrm{I_Z}} s}\right) \cdot \frac{V_\mathrm{in}}{V_\mathrm{st}} \cdot \frac{R_\mathrm{Shunt}}{R_\mathrm{l}} \cdot \frac{1 + s \cdot T_\mathrm{E}}{1 + \frac{2 D_\mathrm{r}}{\omega_0} s + \frac{1}{\omega_0^2} s^2} \end{aligned} \tag{8.16}$$

Apart from the resonance overshoot, the gain curve shows approximately I-behavior. To estimate the maximum gain of the control loop, the transfer function is specialized for large values of s to consider the range of the crossover frequency f_c. The crossover frequency is the frequency at which the amplitude response intersects the 0 dB axis,

i.e. the gain of the control loop is equal to the value 1.

$$|T(j2\pi f_c)| = 1 \Rightarrow 0\,dB \tag{8.17}$$

Furthermore, the crossover frequency is a measure of how quickly the setpoint is reached after a sudden load change. The higher the crossover frequency is, the higher is the reaction speed and the faster is the step response in the time domain.
For large values of s and considering $R_c \ll R_l$, equation (8.16) results in:

$$\begin{aligned} G_{o,i}(s) &\approx K_I \cdot \frac{V_{in}}{V_{st}} \cdot \frac{R_{Shunt}}{R_l} \cdot \frac{C \cdot (R_l + R_c)}{s \cdot L \cdot C} \\ &\approx K_I \cdot \frac{V_{in}}{V_{st}} \cdot \frac{R_{Shunt}}{sL} \end{aligned} \tag{8.18}$$

K_I is the gain of the current amplifier and for the crossover frequency the following must apply by definition:

$$\left| K_I \cdot \frac{V_{in}}{V_{st}} \cdot \frac{R_{Shunt}}{s \cdot L} \right| = \left| K_I \cdot \frac{V_{in}}{V_{st}} \cdot \frac{R_{Shunt}}{L} \cdot \frac{1}{2 \cdot \pi \cdot f_c} \right| = 1 \tag{8.19}$$

The determination of K_I depends on the slope of the sawtooth signal.
The maximum permissible current amplification is required to determine the crossover frequency. This in turn depends on the voltage measured at the shunt and on the sawtooth signal:

$$v_{Shunt} = K_{I,max} \cdot R_{Shunt} \cdot i_L \tag{8.20}$$

The following applies for the limit case:

$$K_{I,max} \cdot R_{Shunt} \cdot \frac{di_L}{dt} = \frac{V_{st}}{T} \tag{8.21}$$

The current through the inductor in buck mode depends on the higher voltage:

$$\left| \frac{di_L}{dt} \right| = \frac{V_{out}}{L} = \frac{V_{HV}}{L} \tag{8.22}$$

With constant voltage on the high side and the substitution of equation (8.22) into (8.21) gives :

$$\begin{aligned} K_{I,max} \cdot R_{Shunt} \cdot \frac{V_{out}}{L} &= \frac{V_{st}}{T} \\ K_{I,max} &= \frac{V_{st}}{T} \cdot \frac{L}{V_{out} \cdot R_{Shunt}} \end{aligned} \tag{8.23}$$

K_I is the gain factor of the current controller and corresponds to the transfer function between the voltage measured at the shunt resistor v_{Shunt} and the controller output v_c.

Thus, the following applies in general:

$$G_{\mathrm{I}}(s) = \frac{\delta v_{\mathrm{c}}}{\delta V_{\mathrm{Shunt}}} \tag{8.24}$$

With the assumption that the controller has a consistent gain near the crossover frequency it follows:

$$G_{\mathrm{I}}(s) = K_{\mathrm{I}} = const. \tag{8.25}$$

By substituting the equation (8.23) into (8.18) and setting equation (8.18) equal to the value 1, the crossover frequency can be determined:

$$\begin{aligned} |G_{\mathrm{o,i}}(s)| &= \left| \frac{V_{\mathrm{st}}}{T} \cdot \frac{L}{V_{\mathrm{out}} \cdot R_{\mathrm{Shunt}}} \cdot \frac{V_{\mathrm{in}}}{V_{\mathrm{st}}} \cdot \frac{R_{\mathrm{Shunt}}}{s_{\mathrm{c}} L} \right| = 1 \\ |G_{\mathrm{I,o}}| &= \left| \frac{V_{\mathrm{st}}}{T} \cdot \frac{L}{V_{\mathrm{out}} \cdot R_{\mathrm{Shunt}}} \cdot \frac{V_{\mathrm{in}}}{V_{\mathrm{st}}} \cdot \frac{R_{\mathrm{Shunt}}}{2\pi f_{\mathrm{c}} L} \right| = 1 \end{aligned} \tag{8.26}$$

With $T = \frac{1}{f_{\mathrm{s}}}$, it follows:

$$\begin{aligned} \frac{V_{\mathrm{in}}}{V_{\mathrm{out}}} \cdot \frac{f_{\mathrm{s}}}{2\pi f_{\mathrm{c}}} &= 1 \\ f_{\mathrm{c}} &= \frac{V_{\mathrm{in}}}{V_{\mathrm{out}}} \cdot \frac{f_{\mathrm{s}}}{2\pi} \end{aligned} \tag{8.27}$$

8.3.4 General Controller Design with the Small-Signal Model

The objectives for controller dimensioning are

- the achievement of the highest possible crossover frequency for high control dynamic,
- a preferably constant gain curve up to the crossover frequency,
- highest possible gain at low frequencies for high control accuracy,
- lowest possible gain for high frequencies to suppress the disturbances given there,
- preferably high phase and magnitude reserve and
- a slope (roll-off) of -20 dB per decade at the crossover frequency. [385, 387]

The basis for the controller design is the analysis of the small-signal model and the investigation of the poles and zeros of the derived transfer functions. Zero points inside the left half plane show an increase in the gain of $+20$ dB/decade and a phase change of $+90°$. This is the exact opposite of a pole on the left half plane. Its gain value is -20 dB/decade and its phase changes by $-90°$. To achieve the desired crossover frequency, phase and magnitude margin, zeros are introduced to compensate for an existing pole of the same frequency, and analogously, pole points are introduced for zero compensation.
The zero in the right half plane (RHP) also has a gain of $+20$ dB/decade but with a phase change of $-90°$. A pole in the right half plane has a gain of -20 dB/decade with a phase change of $+90°$.
The characteristic of a right half plane zero is difficult to compensate and usually requires lower crossover frequencies and a reduction in loop gain at lower frequencies. This leads to significant limitations in dynamic range.

Considering the average current mode control, it is required that the slope of the controller output v_c does not exceed the one of the sawtooth in order to avoid switching oscillations. This condition determines the upper limit of the gain factor $K_{I,max}$.
The averaged small-signal model of the DC-DC converter is used to analyze the effects of the feedback on the small-signal transfer functions. The loop gain is defined as the product of the small-signal gains in the feedback and forward plants. Large loop gains result in the influence of the disturbance on the output being small and the controller output quantities being close to the setpoint with little dependence on the forward plant gain. Consequently, the magnitude of the loop gain is a measure of how well the control system is performing.
To avoid oscillation, ringing, overshoot, or other undesirable behavior, sufficient phase margin is necessary. Determining phase margin is a simple method for evaluating the stability of the system. The phase margin is the distance of the phase at the crossover frequency to -180° and is defined as follows:

$$\varphi_m = 180 + \angle T(j2\pi f_c) \tag{8.28}$$

If the phase margin is positive and there is no right half plane zero, the system is stable. Too small phase reserves lead to resonant pole positions of the closed loop transfer functions which in turn can cause overshoots and ringings.
The magnitude margin is measured at the frequency where the phase shift is equal to $-180°$. It is defined as the distance from the measured gain to a gain of 0 dB. The greater the value of the magnitude margin, the greater is the stability of the system. The magnitude margin refers to the amount of gain that can be increased or decreased without the system becoming unstable, i.e., reaching 0 dB. Magnitude and phase margin represent the distance from the points where instability could occur. A higher distance corresponds to more stability.
In the following, the current and voltage loops (Fig. 8.8) are considered more generally as the basis for the subsequent hardware- and software-based control.

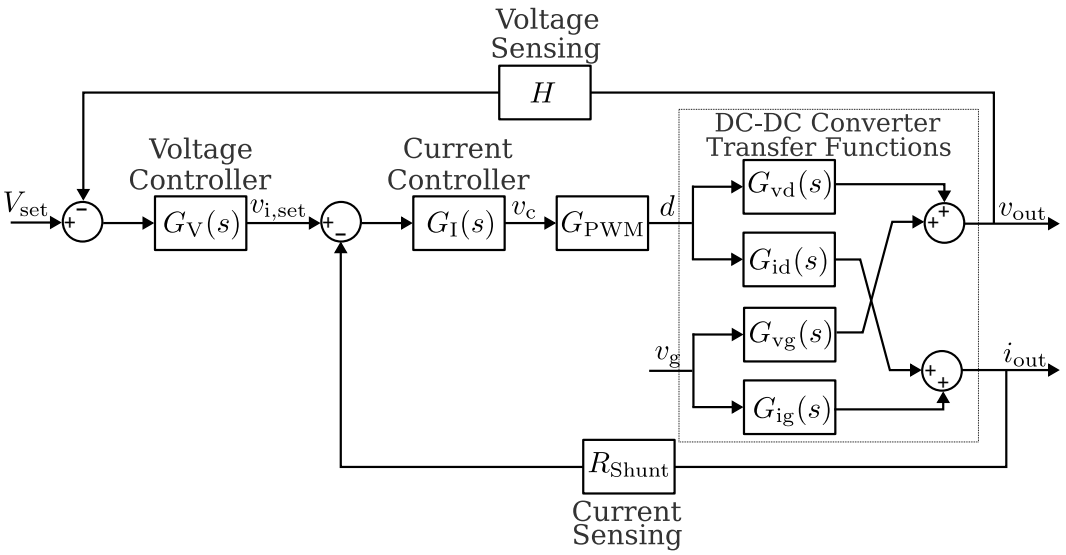


Figure 8.8: Block diagramm of the inner average current mode control and the outer voltage control loop with the small-signal model of the DC-DC converter and the relevant transfer functions, which are described in Chapter 7. [387]

Using the feedback theorem, the small-signal closed loop response of the current is obtained:

$$i_{\text{out}} = \frac{1}{R_{\text{Shunt}}} \cdot \frac{T_{\text{i}}}{1+T_{\text{i}}} \cdot v_{\text{i,set}} + G_{\text{ig}} \cdot \frac{1}{1+T_{\text{i}} \cdot v_{\text{g}}} \tag{8.29}$$

with

$$T_{\text{i}} = R_{\text{Shunt}} \cdot G_{\text{I}} \cdot G_{\text{PWM}} \cdot G_{\text{id}} \tag{8.30}$$

The closed control to current transfer function follows:

$$G_{\text{I,c}} = \left.\frac{i_{\text{out}}}{v_{\text{i,set}}}\right|_{v_g=0} = \frac{1}{R_{\text{Shunt}}} \cdot \frac{T_{\text{i}}}{1+T_{\text{i}}} \tag{8.31}$$

According to the feedback theorem the following results for the small-signal output voltage:

$$v_{\text{out}} = \left(G_{\text{I}} \cdot G_{\text{PWM}} \cdot G_{\text{vd}} \cdot \frac{1}{1+T_{\text{i}}}\right) \cdot v_{\text{i,set}} + \left(G_{\text{vg}} - \frac{G_{\text{ig}}}{G_{\text{id}}} \cdot G_{\text{vd}} \cdot \frac{1}{1+T_{\text{i}}}\right) \cdot v_{\text{g}} \tag{8.32}$$

For the control to output voltage transfer function with closed inner current control loop follows:

$$\begin{aligned} G_{\text{V,c}} &= \left.\frac{v_{\text{out}}}{v_{\text{i,set}}}\right|_{v_g=0} = G_{\text{I}} \cdot G_{\text{PWM}} \cdot G_{\text{vd}} \cdot \frac{1}{1+T_{\text{i}}} \\ &= \frac{1}{R_{\text{Shunt}}} \cdot \frac{G_{\text{vd}}}{G_{\text{id}}} \cdot \frac{1}{1+T_{\text{i}}} \end{aligned} \tag{8.33}$$

For the voltage controller, the gain of the voltage loop T_{v} is adjusted accordingly:

$$T_{\text{v}} = H \cdot G_{\text{V}}(s) \cdot G_{\text{VI,c}}(s) \tag{8.34}$$

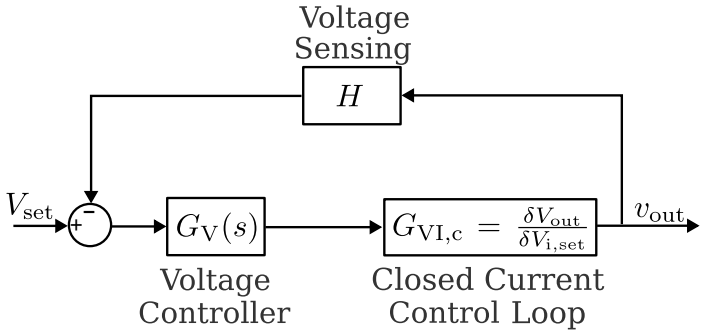


Figure 8.9: Block diagram of the voltage control loop with the closed inner current control. [387]

8.3.5 Multiphase Bidirectional Current Controller

For the implementation of the ACMC, the multiphase bidirectional current controller LM5170 device from Texas Instrument is utilized [388] (Figs. 8.10, 8.11). In the corresponding data sheet, a PI controller with an additional pole is recommended.

This pole improves the damping of high-frequency components. For the following considerations of the current control loop this controller is referred to. The transfer function of the controller from the data sheet [388] is defined as:

$$G_{\mathrm{I}}(s) = \frac{G_{\mathrm{m}}}{C_{\mathrm{COMP}}} \cdot \frac{1 + s \cdot R_{\mathrm{COMP}} \cdot C_{\mathrm{COMP}}}{s \cdot (1 + s \cdot R_{\mathrm{COMP}} \cdot C_{\mathrm{HF}})} \tag{8.35}$$

Thereby C_{COMP} and R_{COMP} describe the components of the compensation network for adjusting the total gain of the inner current loop. G_{m} is the transconductance of the error amplifier, which is $1\,\frac{mA}{V}$ (Fig. 8.11).

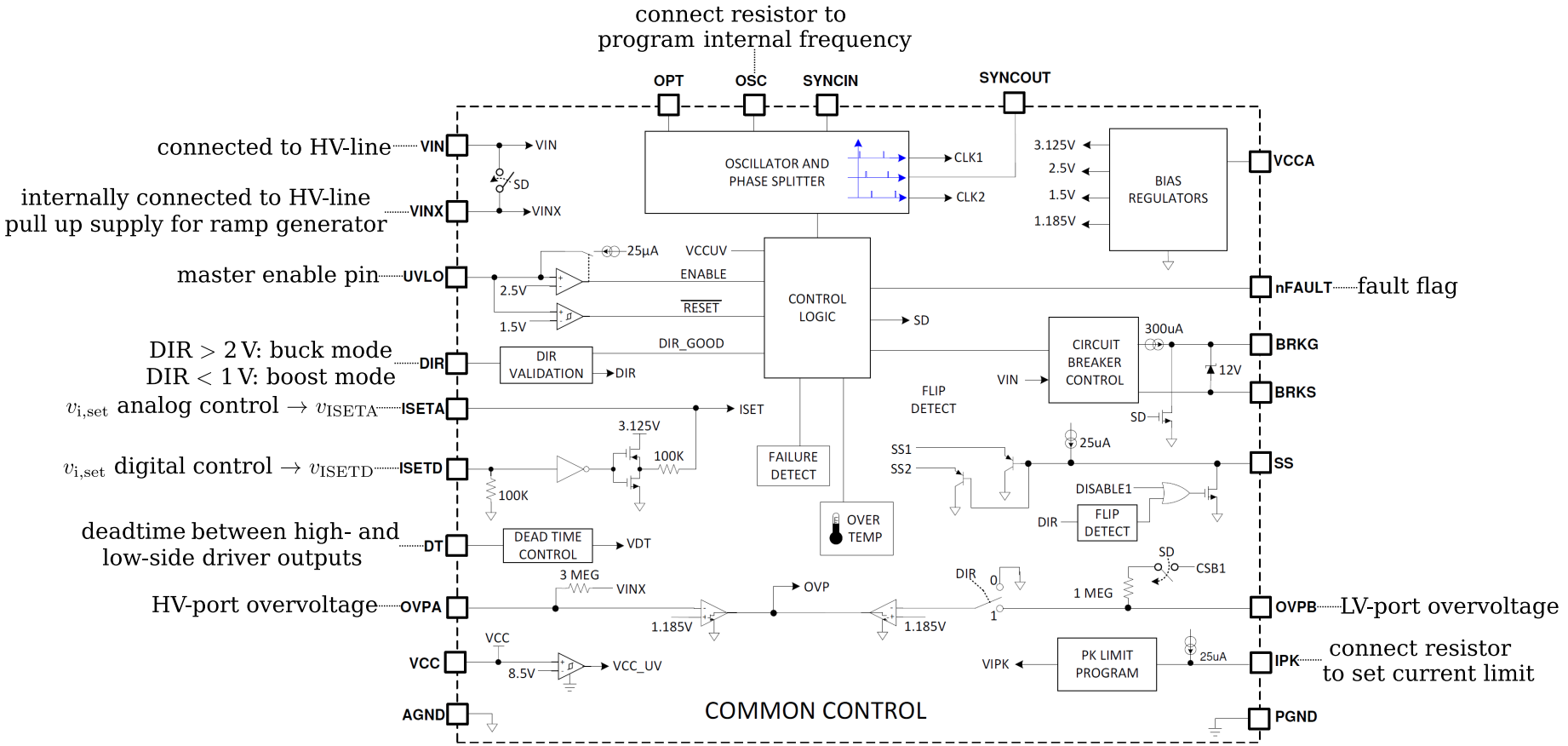


Figure 8.10: Functional diagram of the common control block of the ACMC integrated circuit (IC) LM5170 [388]. The main functions include fault detection, overvoltage protection, buck or boost selection, and analog or digital control option. (Picture slightly adapted from [388])

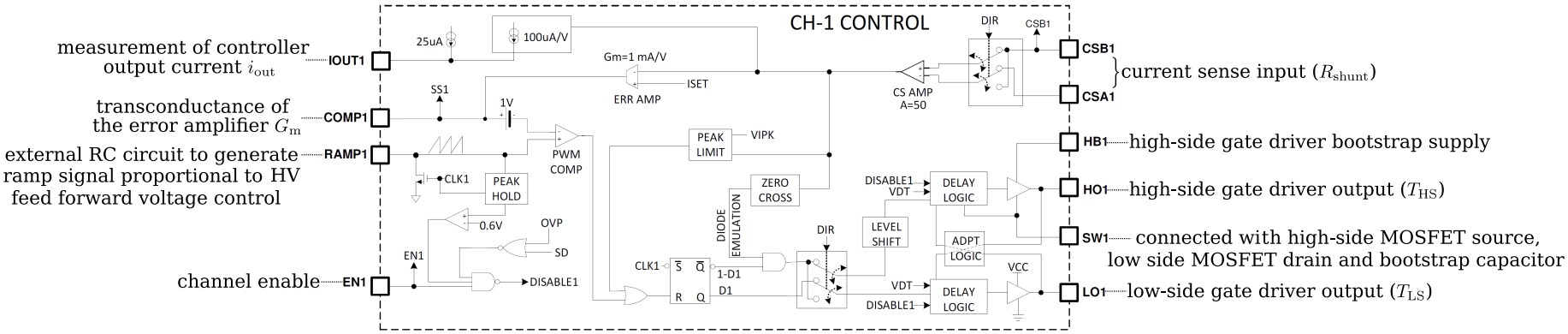


Figure 8.11: Functional diagram of one of the two channel average current mode control units of the LM5170 [388]. Main functions are the control of the two MOSFETs, the generation of the ramp signal and the measurement of the controller output. (Picture slightly adapted from [388])

8.3.6 Generation of the PWM Signal for Switching the Transistors G_{PWM}

Part of the ACMC is the comparison of the controller output variable v_{c} with the voltage of the sawtooth generator v_{st} (Fig. 8.4). The voltage of the sawtooth generator is applied to the inverting input of the operational amplifier, while the controller output is applied to the non-inverting input (Fig. 8.12).

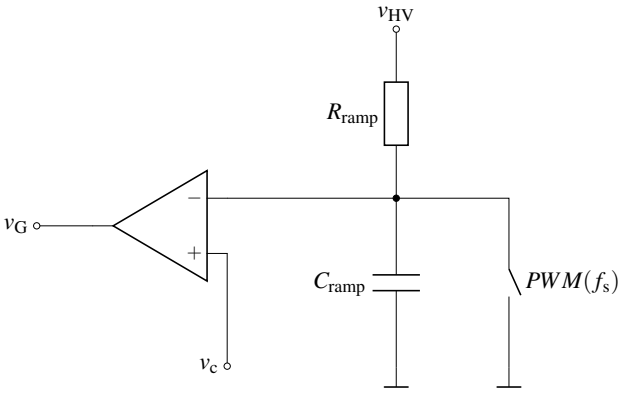


Figure 8.12: To generate the switching edges $v_{\mathrm{G}}(t)$, the controller output is connected to the non-inverting input of an operational amplifier. The voltage of the sawtooth generator is applied to the inverting input.

To obtain a sawtooth shaped voltage, the capacitor C_{ramp} must be chosen sufficiently large. The switch is closed at the end of the clock period to discharge the capacitor. The feed forward gain K_{FF} is defined as:

$$K_{\mathrm{FF}} = \frac{1}{R_{\mathrm{ramp}} \cdot C_{\mathrm{ramp}} \cdot f_{\mathrm{s}}} \tag{8.36}$$

The switching frequency thereby corresponds to f_{s}.
The feed forward gain causes the small-signal transfer function to be independent of the input voltage. The total transfer function G_{PWM} for the PWM generator is given by the following equation:

$$G_{\mathrm{PWM}} = \frac{\partial d}{\partial v_{\mathrm{c}}} = \frac{1}{v_{\mathrm{HV}} \cdot K_{\mathrm{FF}}} \tag{8.37}$$

The transfer function of the PWM modulator is a real number and causes no phase rotation.
The duty cycle d is defined by:

$$d = \frac{v_c}{v_{\mathrm{st}}} \tag{8.38}$$

8.3.7 Current Transfer Function H_{S}

The total transfer function of the closed current control loop is derived resulting from the two previously calculated functions.

$$H_\mathrm{s} = \frac{G_\mathrm{I}(s) \cdot G_\mathrm{id}(s) \cdot G_\mathrm{PWM}(s)}{1 + K \cdot R_\mathrm{Shunt} \cdot G_\mathrm{I}(s) \cdot G_\mathrm{id}(s) \cdot G_\mathrm{PWM}(s)} \tag{8.39}$$

For the current transfer function of two channels, a factor of two has to be considered. For high gains of the open circuit, the following applies:

$$\lim_{G_\mathrm{id}(s)\,G_\mathrm{PWM}(s)\,G_\mathrm{I}(s) \to \infty} H_\mathrm{s} = \frac{2}{K \cdot R_\mathrm{Shunt}} \tag{8.40}$$

The current controller, which was implemented by the LM5170 chip from Texas Instruments, leads to a high gain of the open circuit. For this reason, the approximation from equation (8.40) is valid up to a high cutoff frequency ω_g.

$$G(j\omega_\mathrm{g}) \cdot G_\mathrm{id}(j\omega_\mathrm{g}) = 1 \mathrel{\widehat{=}} 0\,dB \tag{8.41}$$

$$G_\mathrm{id,A}(s) = \frac{V_\mathrm{HV}}{(R_\mathrm{x} + R_\mathrm{l})} \cdot \frac{1}{1 + \frac{L}{R_\mathrm{x}+R_\mathrm{l}} \cdot s} \tag{8.42}$$

$$\approx \frac{V_\mathrm{HV}}{R_\mathrm{l}} \cdot \frac{1}{1 + \frac{L}{R_\mathrm{l}} \cdot s} \tag{8.43}$$

The approximate transfer function of the buck converter in the continuous conduction mode (Equ. (8.43)), which was derived in Chapter 7, together with the transfer function of the controller (Equ. (8.35)) results in the following:

$$s_{1,2} = \frac{(C_1 \cdot C_2 - C_3) \pm \sqrt{(C_1 \cdot C_2 - C_3)^2 + 4 \cdot C_1 \cdot C_2 \cdot C_4}}{2 \cdot C_4 \cdot C_3} \tag{8.44}$$

$$C_1 = K \cdot R_\mathrm{Shunt} \cdot G_\mathrm{m} \tag{8.45}$$

$$C_2 = R_\mathrm{COMP} \cdot C_\mathrm{COMP} \tag{8.46}$$

$$C_3 = C_\mathrm{COMP} \cdot (1 + R_\mathrm{COMP} \cdot C_\mathrm{HF}) \cdot R_\mathrm{l} \tag{8.47}$$

$$C_4 = \frac{L_\mathrm{m}}{R_\mathrm{l}} \tag{8.48}$$

Thereby, C_HF is a capacitor of the compensation network and L_m is the power inductor. The cutoff frequency is in the range of the switching frequency. It is evident that the cut-off frequency depends on the load. Experience shows that the crossover frequency of the voltage control is selected in the range of $\frac{1}{20} \ldots \frac{1}{50}$ of the switching frequency. For this reason, the dynamic behavior does not play a significant role for the voltage control. The considerations for all other transfer functions is similar and provides analogous results. In Fig. 8.13, the magnitude and phase frequency response for the buck converter in CCM mode is shown. As a result, the assumption that only the dynamic response of the output filter needs to be considered for voltage control is reasonable:

$$H_\mathrm{s} \approx \frac{2}{K \cdot R_\mathrm{Shunt}} \tag{8.49}$$

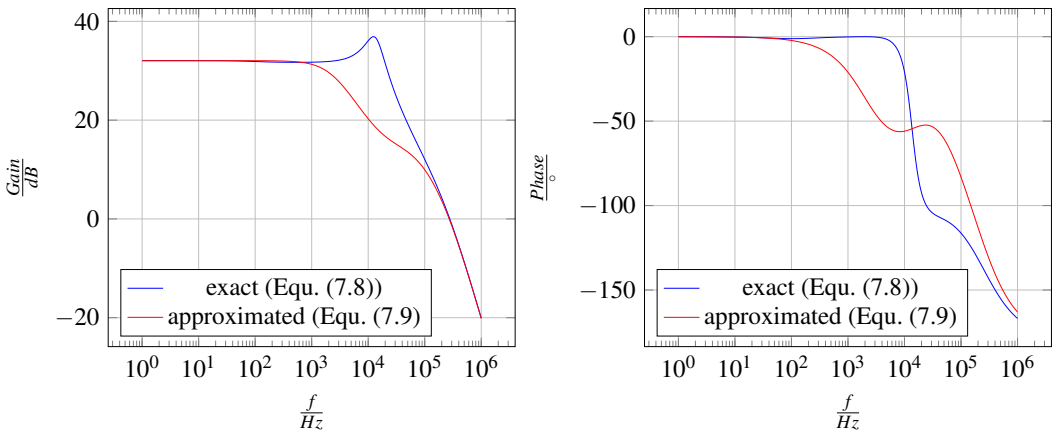


Figure 8.13: Calculated Bode diagram of the closed current control loop of the buck converter in the CCM. The closed current control loop with the approximated $G_{id,A}(s)$ (Equ. (7.9) on p. 7.9)) and the exact $G_{id}(s)$ (Equ. (7.8) on p. 7.8)) current to duty cycle transfer function is shown.

8.4 Design of the Controller

The design process of an average current mode control with outer voltage control loop starts with the design of the inner current controller followed by the outer voltage controller. Usually PI-compensators are sufficient for both [387]. In this case, PI-compensators are also used for both controllers. It is common practice to select the crossover frequency of the voltage controller well below the crossover frequency of the current controller. This is not the only available option, but is also used in the case of the controller design for the bidirectional DC-DC converter.

8.4.1 Design of the Current Controller $G_{\mathrm{I}}(s)$

The open loop of the current control $G_{\mathrm{o,i}}(s)$ corresponding to the control loop in Figure 8.6 is given by:

$$G_{\mathrm{o,i}}(s) = G_{\mathrm{I}}(s) \cdot G_{\mathrm{PWM}}(s) \cdot G_{\mathrm{id}}(s) \cdot K \cdot R_{\mathrm{Shunt}} \tag{8.50}$$

The structure of $G_{id}(s)$ is identical in CCM operation for the buck and the boost converter. The modeling of the DC-DC converter and the derivation of the transfer functions showed that the controlled system exhibits PT1 behavior if the resonance overshoot is neglected. Therefore, a PI controller is sufficient to control this system. The high frequency pole is compensated with the zero point of the controller. The objective is to achieve the highest possible crossover frequency, whereby the crossover frequency can be adjusted with the help of the gain factor.

8.4.2 Design of the Voltage Controller $G_{\mathrm{V}}(s)$

The open loop of the voltage control $G_{\mathrm{o,v}}$ is significant for the voltage control (Fig. 8.6) . It consists of the closed-loop current control loop H_{s}, the current to voltage transfer function G_{vi} and the transfer function of the measuring unit G_{m} (Fig. 8.9).

$$G_{\mathrm{o,v}}(s) := G_{\mathrm{m}} \cdot H_{\mathrm{s}} \cdot G_{\mathrm{vi}}(s) \cdot G_{\mathrm{V}}(s) \tag{8.51}$$

$$H_{\mathrm{s}} := \frac{G_{\mathrm{I}}(s) \cdot G_{\mathrm{PWM}}(s) \cdot G_{\mathrm{id}}(s)}{1 + K \cdot R_{\mathrm{Shunt}} \cdot G_{\mathrm{I}}(s) \cdot G_{\mathrm{PWM}}(s) \cdot G_{\mathrm{id}}(s)} \tag{8.52}$$

8.4.3 Controller Design for Buck Mode

In the following, general aspects of current and voltage control for buck mode are considered.

Control Aspects of the Continuous Conduction Mode in Buck Mode

The current transfer function H_{s} (Equ. (8.52)) exhibits a pole, which, as shown in the small-signal analysis and the derivation of the current transfer function, is high-frequent and therefore it is only required to consider it indirectly for the control. The current to voltage transfer function $G_{vi}(s)$ has a zero and a pole. The frequency of the pole is significantly lower than the one of the zero. The frequency of the zero is difficult to estimate because the resistance R_{C} depends on many factors. If capacitors with low R_{C} values are used, the frequency of the zero is very high. In the following, it is assumed that the zero frequency is greater than the crossover frequency. Consequently, the total gain of the open loop corresponds to a first order system and can thus be controlled with a PI controller. The general form of the voltage controller is given by:

$$G_{\mathrm{V}}(s) = K \cdot \frac{Ts + 1}{s} \tag{8.53}$$

The zero is placed in a way that it compensates the pole of the output filter $G_{\mathrm{id}}(s)$ (Equ. (7.8) on p. 115).

$$T = \frac{1}{2\pi RC} \tag{8.54}$$

The gain factor K can be determined with the required crossover frequency f_{c}:

$$G_{\mathrm{o,v}}(s) \approx H(0) \cdot (1 + R_{\mathrm{C}} \cdot C \cdot s) \cdot \frac{K}{s} \tag{8.55}$$

$$\left| G_{\mathrm{o,v}}(2\pi f_{\mathrm{c}}) \right| = 1 = \left| H(0) \cdot R_{\mathrm{l}} \cdot \frac{K}{j2\pi f_{\mathrm{c}}} \right| \tag{8.56}$$

Thus K results in:

$$K = \frac{2\pi f_{\mathrm{c}}}{H(0) \cdot R_{\mathrm{l}}} \tag{8.57}$$

The resulting Bode diagram shows approximately the behavior of a purely integral element (Fig. 8.14). Frequencies greater than the crossover frequency contribute only marginally to the time response.

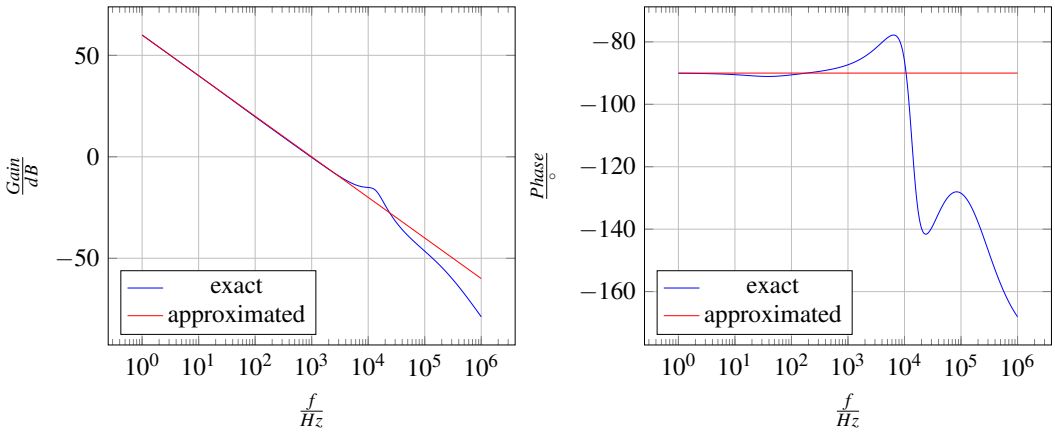


Figure 8.14: Bode diagram of the controlled open loop at a crossover frequency of $f_c = 1\,kHz$ and an approximation with $\frac{2\pi f_c}{s}$

The reverse transformation into the time domain provides for the integral approximation:

$$\mathscr{L}^{-1}\{\frac{2\pi \cdot f_c}{2\pi \cdot f_c + s}\} = 2\pi \cdot f_c \cdot e^{-2\pi \cdot f_c \cdot t} \tag{8.58}$$

The reverse transformation corresponds to an exponential function with negative exponent. The system will not overshoot, but converge to the lower limit.

Control Aspects of the Discontinuous Conduction Mode in Buck Mode

If the pole frequency of the closed current control loop is greater than the crossover frequency of the voltage control loop, the latter can still be regarded as constant. This is achieved by selecting the crossover frequency accordingly. Since the current to voltage transfer function G_{vi} in the CCM (Equ. (7.16) on p. 116) and DCM (Equ. (7.27) on p.122) are identical, the control transfer function can be determined in the same way as in the CCM.

8.4.4 Controller Design for Boost Mode

For the design the controller for boost mode, the maximum value of the crossover frequency is limited by the right half plane zero. A general approach to determine the crossover frequency f_c is thereby:

$$f_c < \frac{1}{20} \cdot f_{RHPZ} \tag{8.59}$$

The consideration of the pole and zero points is otherwise identical to the consideration of the buck converter. The calculation of the controller coefficients is also the same.

8.5 Implementation of the Control

The control of the bidirectional DC-DC converter with the controller module LM5170 is realized analog, hardware based and digital, software based. Hardware-based controllers are designed for one operating point and the electrical components are

dimensioned accordingly. They are characterized by robustness and high dynamics with low flexibility due to the fixed control parameters realized by the respective electrical components. With software-based controllers, the control parameters can be adapted depending on the current operating point and thus a sufficient control behavior can be realized at a variety of operating points. This offers the possibility to support a wide range of different load types. Depending on the sampling frequency and the resolution, dead times and discretization errors occur.
In the following, the hardware- and software-based implementation of the control is described.

8.5.1 Hardware-based Implementation

Analog controllers are designed via the corresponding dimensioning of the electrical components and are characterized by fixed operating points. Variable resistors and capacitors, e.g. resistor values that can be adjusted via respective microcontroller interfaces, are an exception and allow adjustments within a certain range. In general, the electrical components are designed in such a way that the stability of the control loop is ensured over the entire operating range. A controller design is only reasonably feasible within a limited load range.
At very high output resistances, the pole frequencies reduce towards zero in the limit case. This leads to a phase rotation, which is significantly smaller than -180°. Physically, this can be explained by the fact that a DC-DC converter designed for high currents has large energy storage components in the form of capacitors and inductors. These have a significant damping effect at low currents.
The analog controller is implemented with an operational amplifier. The general structure of the controller is shown in Fig. 8.15.

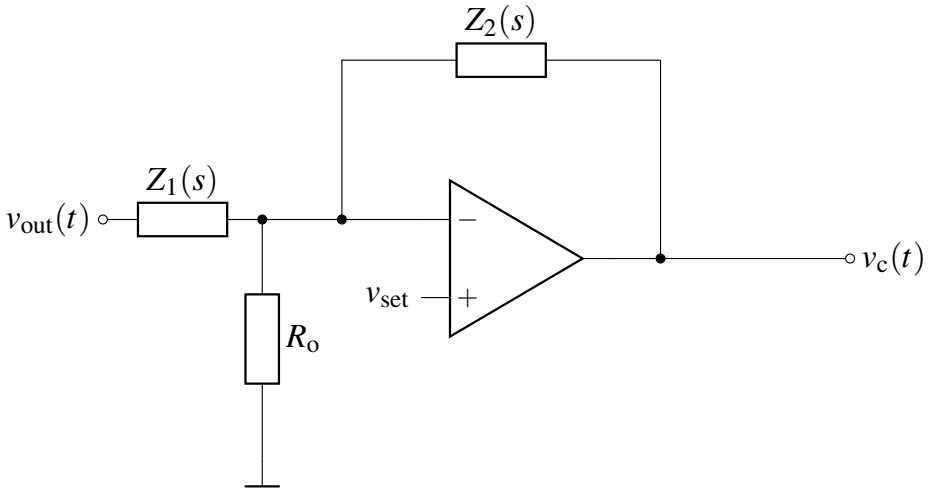


Figure 8.15: General structure of an analog controller

The large signal behavior of the controller is represented by:

$$V_{\mathrm{set}} = \frac{R_{\mathrm{o}}}{Z_1(0) + R_{\mathrm{o}}} \cdot V_{\mathrm{out}} \tag{8.60}$$

The voltage divider sets the operating point of the controller. The small-signal behavior is defined by:

$$v_c(s) = -\frac{Z_2(s)}{Z_1(s)} \cdot v_{\text{out}}(s) \tag{8.61}$$

The minus sign here results from the negative feedback. The phase rotation of 180° is often not shown in the Bode diagram. The maximum value of the manipulated variable is determined by the supply voltage of the operational amplifier. A subsequent voltage divider can be used for limiting the maximum if necessary.

8.5.2 Software-based Implementation

Digital controllers allow to adjust the control parameters according to the load at the output. The calculation of the gain and the time constant is performed by the microcontroller. Digitizing the controller results in a dead time that depends on the sampling frequency. This dead time results in a phase rotation defined by the following equation:

$$\phi_{\text{dead}} = e^{-sT_{\text{dead}}} \tag{8.62}$$

Where T_{dead} corresponds to the time between the sampling of the actual current and voltage values and the setting of the new controller value. Under the assumption that the calculation after sampling always takes the same time and is done in one sampling period, the dead time corresponds to the sampling period. Depending on the selected sampling frequency, the phase rotation can be neglected. According to the Nyquist criterion, the sampling frequency must be at least twice the maximum occurring frequency. In this case, a factor of 10 is selected. Since all frequencies higher than the crossover frequency of the control loop are attenuated by at least 8 $\frac{dB}{oct}$, the sampling frequency has to be at least one decade higher.
For digital control, the controller must be z-transformed. This is done with the help of the Tustin approximation.

$$s \approx \frac{2}{T} \cdot \frac{1-z^{-1}}{1+z^{-1}} \tag{8.63}$$

In numerical mathematics, this procedure is known as the trapezoidal rule. The z-transformation of the PI-controller results in:

$$\mathscr{Z}\{K \cdot \frac{Ts+1}{s}\} = K \cdot T + K \cdot \frac{1+z^{-1}}{\frac{2}{T_s}(1-z^{-1})} \tag{8.64}$$

The new manipulated variable $y[n]$ is finally given by:

$$y[n] = \left(e[n] \cdot \left(T + \frac{T_s}{2}\right)\right) - e[n-1] \cdot \left(T - \frac{T_s}{2}\right)\right) \cdot K + y[n-1] \tag{8.65}$$

Thereby e describes the control deviation.

8.6 Concrete Implementation and Consideration of the Control Approaches

Selecting a multiphase DC-DC converter with two channels enables the use of significantly smaller components. This has a positive effect on the thermal behavior of the converter. The current ripple, which has to be smoothed by the output capacitance, can also be significantly reduced by a suitable shift in the switching times. In the literature, this is referred to as ripple cancelling [389].
The position of the boundary conduction is crucial for the control.
The given equations (7.4) on p. 114 and (7.31) on p. 124 for the boundary refer to one channel. Consequently, I_{BCM} doubles for two channels.
All relevant component values, current and voltage values as well the large signal parameters are listed in Table 8.1.

Table 8.1: Key figures and components values for each of the two channels

Description	Value
V_{HV}	24 V
V_{LV}	12 V
f_{s}	100 kHz
R_{Ramp}	$95\,k\Omega$
C_{Ramp}	$1\,nF$
R_{shunt}	$3\,m\Omega$
K_{shunt}	50
$I_{\mathrm{BCM,Boost}}$	3 A
$I_{\mathrm{BCM,Buck}}$	6 A
$d_{\mathrm{Buck,CCM}}$	0.5
$d_{\mathrm{Buck,DCM}}$	$\frac{2}{\sqrt{2R}}$
$d_{\mathrm{Boost,CCM}}$	0.5
$d_{\mathrm{Boost,DCM}}$	$\frac{1}{\sqrt{R}}$
R_{Boost}	$[1.2\,\Omega,\infty]$
R_{Buck}	$[0.6\,\Omega,\infty]$
L	$10\,\mu H$
C_{LV}	$757{,}8\,\mu F$
$R_{\mathrm{C,LV}}$	$\approx 4\,m\Omega$
C_{HV}	$637\,\mu F$
$R_{\mathrm{C,HV}}$	$\approx 4\,m\Omega$

8.6.1 Controller Dimensioning

The dimensioning of the controller approaches can be implemented effectively based on the previously analyzed transmission behavior and according to the described general control approaches. First, general annotations on voltage control are given below. In the following, the closed loop current control, the current to voltage transfer function, the open uncontrolled loop and the open controlled loop for buck and boost mode at different load resistances are observed.

Voltage Control

The zero of the plant to be controlled lies in the frequency range of 10 kHz. The crossover frequency is generally set to the value of $\frac{1}{20}...\frac{1}{50}$ of the switching frequency. Consequently, for the switching frequency of 100 kHz used in this case, the crossover frequency is in a range between 2 kHz up to 5 kHz. Therefore, the zero point is outside the relevant range to be considered and does not have to be taken into account further for the design of the controller.
The maximum frequency of the pole position, which results from the load and output capacitance, is significantly below the crossover frequency in this application. The minimum frequency is zero. The zero point of the controller must also lie in this range.
Since the system has a maximum phase rotation of 90° before the crossover frequency, this design ensures the stability of the system. Depending on the position of the pole in this range, different transient response behavior is obtained. The considerations made before are valid for both the buck and the boost mode of the DC-DC converter. In boost mode, the crossover frequency is determined by the frequency of the right half plane zero. Usually, and also in this application, $f_c = \frac{1}{20} f_{RHPZ}$ is chosen. At low currents, the closed loop pole becomes much lower frequency, causing a phase rotation before the crossover frequency.

8.6.2 Controller Analysis of the Buck Mode

The closed current control loop both in buck and boost mode is given by:

$$G_{c,i} = \frac{2 \cdot G_{ig}(s) \cdot G_I(s) \cdot G_{PWM}}{1 + (K_{shunt} \cdot R_{Shunt} \cdot G_{ig}(s) \cdot G_I(s) \cdot G_{PWM})} \tag{8.66}$$

Equation (8.35) applies to the current controller $G_I(s)$ and equation (8.37) to the transfer function of the PWM generator.
The transfer function between the uncontrolled voltage at the input V_g and the current through the inductor I_L for the L-C filter is given by the equations (8.10) to (8.14) together with the component values defined in Tab. 8.1 for the buck converter in CCM. For the DCM mode, the following applies according to the equivalent circuits from Chapter 7:

$$G_{ig,Bu,DCM}(s) = \frac{j_2 \cdot (1 + (R_c + R_l) \cdot C \cdot s)}{(1 + \frac{R_l}{r_2}) + s \cdot (\frac{L}{r_2} + (R_l + R_c) \cdot C + \frac{R_l \cdot R_c \cdot C}{r2}) + s^2 \cdot (L \cdot C \cdot \frac{R_c + R_l}{r_2})} \tag{8.67}$$

The following equation applies to the open uncontrolled loop $G_{o,u}$:

$$G_{o,u} = G_{c,i} \cdot G_{vi}(s) \tag{8.68}$$

The current to output transfer function in buck mode is the same for CCM and DCM. They were derived in Chapter 7 and correspond to the equation (7.16) on p. 116 for CCM and to equation (7.27) on p.122 for DCM.

$$G_{vi}(s) = R_l \cdot \frac{1 + R_c \cdot C \cdot s}{1 + (R_l + R_c) \cdot C \cdot s}$$

The open controlled loop $G_{o,c}$ is defined as:

$$G_{o,c} = G_{c,i} \cdot G_{vi}(s) \cdot G_V(s) \tag{8.69}$$

The voltage controller $G_V(s)$ is given by the equation 8.53. The following applies to the control parameters:

$$K = \frac{2 \cdot \pi \cdot f_c}{KC \cdot R_{op}} \tag{8.70}$$

$$f_c = \frac{1}{50} \cdot f_s \tag{8.71}$$

$$KC = \frac{2}{K_{shunt} \cdot R_{Shunt}} \tag{8.72}$$

$$T = \frac{1}{2 \cdot \pi \cdot f_p} \tag{8.73}$$

$$f_p = \frac{1}{2 \cdot \pi \cdot (R_{op} + R_c) \cdot C} \tag{8.74}$$

R_{op} is the operating point required for adjusting the analog controller.
Figures A.1 to A.5 show the step response (Fig. A.1 on p. 393), the closed current control loop (Fig. A.2 on p. 394), the current to voltage transfer function (Fig.A.3 on p. 395), the open uncontrolled loop (Fig. A.4 on p. 396) and the open controlled loop (Fig. A.5 on p. 396) of the buck converter in the CCM at a load resistance of $R_l = 2\,\Omega$. The closed current loop shows the desired behavior of the current controller.
Figures A.6 to A.10 show the step response (Fig. A.6 on p. 397) and the transfer functions (Fig. A.7–A.10 on p. 397–399) of the buck converter in the DCM at a load resistance of $R_l = 1\,k\Omega$. In the comparison it can be seen that the transfer functions depend on the load resistance.
Also within CCM and DCM the load resistance influences the behavior. The controlled open loop was obtained using the analog controller with a fixed operating point.

8.6.3 Controller Analysis of the Boost Mode

In boost mode within the CCM, the transfer function between the uncontrolled input voltage V_g and the output current I_L is defined as follows:

$$G_{ig,Bo,CCM}(s) = 2 \cdot \frac{V_{HV}}{R_l} \cdot \frac{1 + s \cdot C \cdot R_l \cdot 0.5^2}{\left(\frac{V_{LV}}{V_{HV}}\right)} + s \cdot \frac{L}{R_l} + s^2 \cdot L \cdot C \cdot 0.5 \tag{8.75}$$

The current to voltage transfer function corresponds to equation (7.32) on p. 124 derived in Chapter 7.

In boost mode and DCM, the transfer function between the uncontrolled input voltage and the output current $G_{\mathrm{ig}}(s)$ is defined as:

$$G_{\mathrm{ig,Bo,DCM}}(s) = \frac{j_1}{1 + s \cdot \frac{L}{r_1}} \tag{8.76}$$

For the following analysis, the exact current to voltage transfer function is applied and it is given by:

$$G_{\mathrm{vi,exact}}(s) = \frac{r_2 \cdot R_\mathrm{l}}{M \cdot (r_2 + R_\mathrm{l})} \cdot (1 - s \cdot L \cdot \frac{M}{Re \cdot (M-1)}) \cdot \frac{1 + s \cdot R_\mathrm{c} \cdot C}{1 + s \cdot C \cdot \frac{r_2 \cdot R_\mathrm{l}}{r_2 + R_\mathrm{l}}} \tag{8.77}$$

The approximation of $G_{\mathrm{vi,approx}}(s)$ in boost mode and DCM was determined previously in Chapter 8.
The crossover frequency of the voltage controller $G_\mathrm{V}(s)$ is determined by the right half plane zero:

$$RHPZ = \frac{1}{2 \cdot \pi \frac{L}{R_{\mathrm{BCM}} \cdot (1 - d_{\mathrm{Boost,CCM}})^2}} \tag{8.78}$$

$$f_\mathrm{c} = \frac{1}{50} \cdot RHPZ \tag{8.79}$$

Apart from the crossover frequency, the equations (8.53), (8.70), (8.72), (8.73) and (8.74) apply analogously to the voltage controller in boost mode.
The step response, the closed current control loop, the output current to output voltage transfer function, the open uncontrolled as well as the open controlled loop for the component dimensioning according to Table 8.1 are shown. Here, Figures A.11 to A.15 (pp. 400–402) correspond to the simulative calculations for the boost mode in CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. Figures A.16 to A.20 (pp.402–404) show the behavior in boost mode in DCM and a load resistance of $R_\mathrm{l} = 1\,k\Omega$. In the comparison, it can be clearly seen that the transfer functions depend on the load resistance and on the mode (CCM or DCM). The open controlled loop was obtained using the fixed operating point analog controller.

8.7 Verification of the Small-Signal Model by Hardware Measurements

To validate the small-signal model, the derivations of the transfer functions and the designed controller approaches, the simulated results are compared with hardware measurements.
The bode diagrams are obtained by measurements conducted with the Bode 100 network analyzer. There are several application notes for this measuring instrument, in which the exact measuring method is described in detail [390]. For this reason, only the measurement results are considered in the following (Figs. 8.16–8.28). For the numerical calculation of the small-signal transfer function, the values from Table 8.1 are used. The current to duty cycle transfer function $G_{\mathrm{id}}(s)$ cannot be measured directly due to the implementation of the average current mode control with the LM5170 IC. The closed loop current control can be determined by measurement.

The measurement curves (Fig. 8.16, 8.17, 8.20, 8.21, 8.23, 8.24, 8.27, 8.28) show only minor deviations from the calculations.
The deviations in the range of the switching frequency result from the Nyquist theorem. Due to electromagnetic interference, the measurements were performed with a high signal strength, which is why saturation effects can be seen in the measurements.

8.8 Summary

In this chapter, the local control of the DC-DC converters was discussed in detail. For accurate voltage and current control, the average current mode control with outer voltage control loop was selected. In contrast to the peak mode control, not only the current limit is controlled, but the average current value. This is necessary for safe and in terms of battery degradation optimized battery operation. The derivation of the control method has been described and the hardware- and software-based implementation using of the LM5170 current controller IC. The hardware-based, analog implementation is designed for one load point and limited to a maximum current of $13.3A$ by the currently used voltage divider. The hardware-based implementation shows advantages when the microcontroller is loaded by additional system tasks like a software update or leader election process. For the setpoint specification it is only necessary to specify a reference voltage via the digital to analog converter of the microcontroller.
The software-based implementation is characterized by flexibility. The controllers can be designed for a large number of different load points. For this purpose, different control parameters dimensioned for the corresponding load range are stored in software and it is possible to switch between them during operation. This improves the control dynamics and stability over a wide load range. The maximum current of the software-based implementation is limited by the current controller IC to $40A$.
The theoretical models partly in combination with the designed controllers were fully verified by hardware measurements. Only minor deviations between the calculations and the hardware measurements occurred. With the help of the modeling, the controllers, both as fixed-value controllers and as adaptive controllers, can be realized. The latter brings advantages in terms of control dynamics and accuracy with variable loads. The local current and voltage control presented in this chapter is the basis for the higher-level global load distribution control.

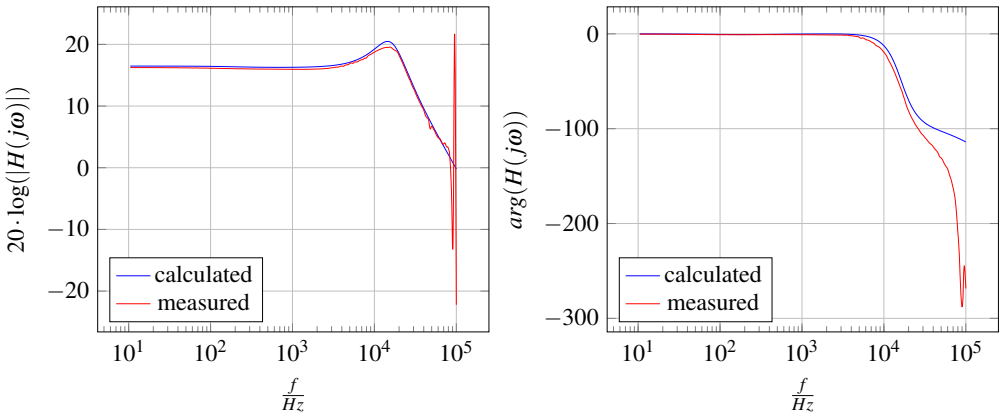


Figure 8.16: Magnitude and phase response of the closed-loop current control loop in buck mode and CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equations (7.19), (8.35), (8.39), and (8.37) were used.

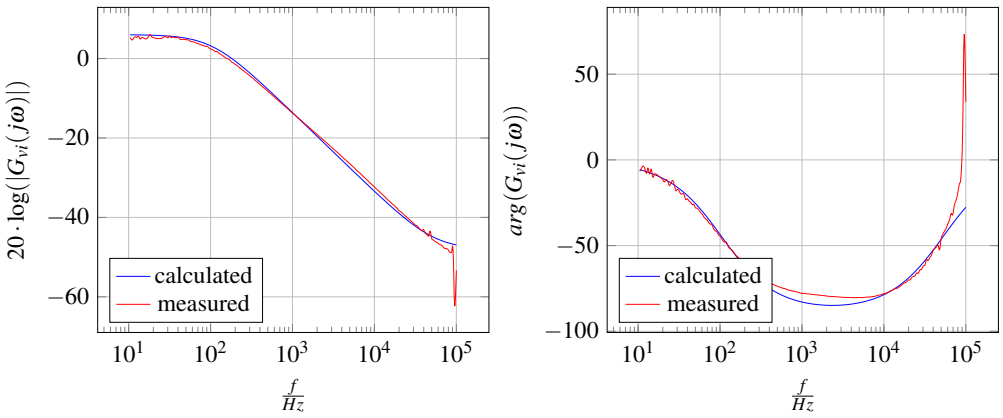


Figure 8.17: Magnitude and phase response of the current to voltage transfer function G_vi in buck mode and in CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The analog controller was used during the measurements. The equation (7.27) is the basis for the calculated results.

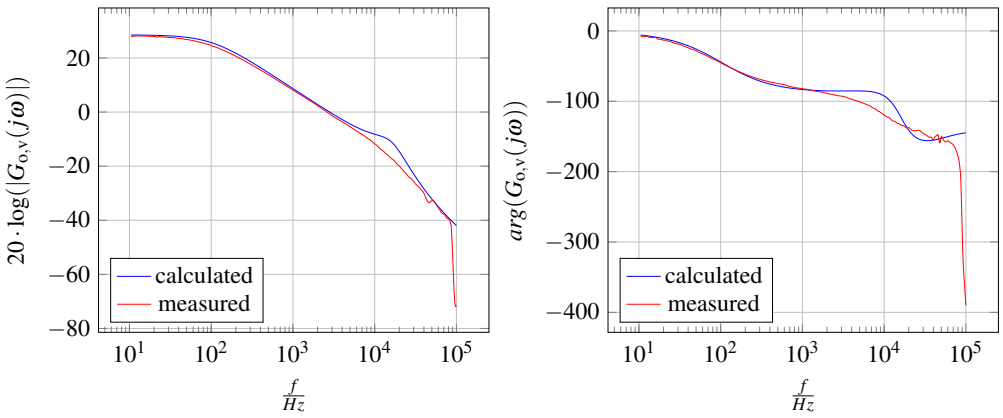


Figure 8.18: Magnitude and phase response of the open loop of the voltage control in buck mode and CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used.

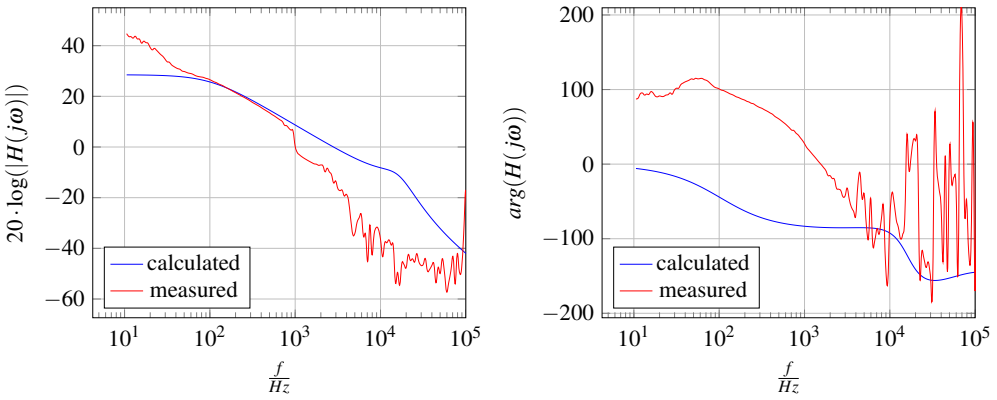


Figure 8.19: Magnitude and phase response of the open loop of the voltage control in buck mode and CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The hardware measurements were acquired using the digital controller. For the calculation the equation (8.51) was used.

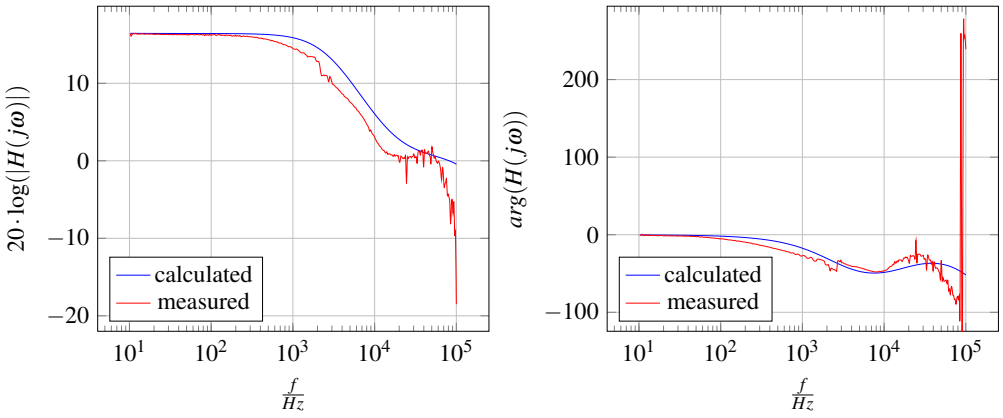


Figure 8.20: Measured and calculated magnitude and phase response of the closed current loop of the buck converter in DCM mode at a load resistance of $R_\mathrm{l} = 24\,\Omega$. The equations (7.22), (8.35), (8.39), and (8.37) were used for the calculation. Hardware measurements were acquired using the analog controller.

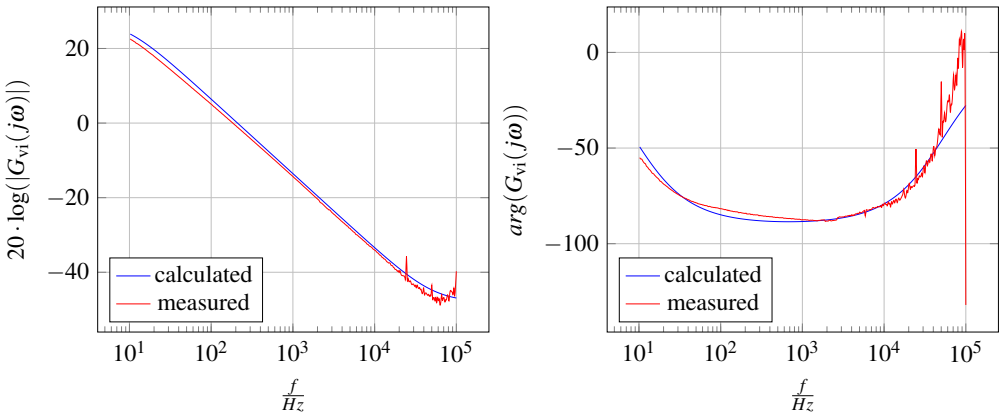


Figure 8.21: Measured and calculated magnitude and phase response of the current to voltage transfer function G_vi of the buck converter in DCM at a load resistance of $R_\mathrm{l} = 24\,\Omega$. The analog controller was used for the hardware measurements and the calculation is based on the equation (7.27).

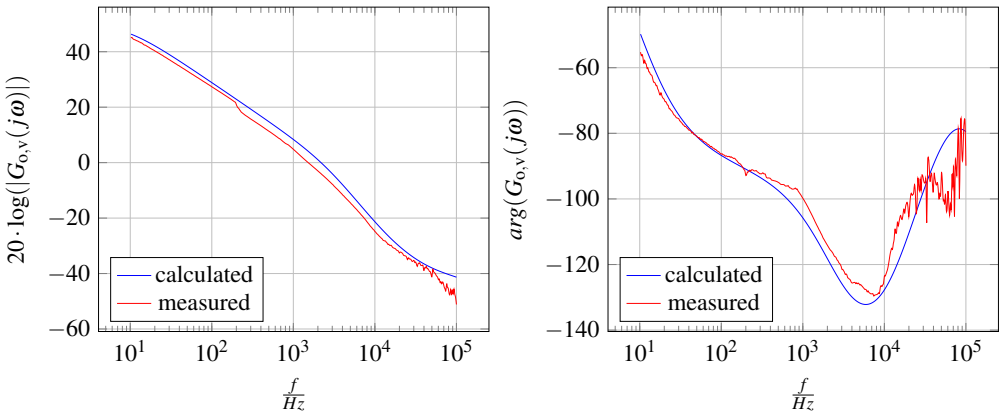


Figure 8.22: Magnitude and phase response of the open loop of the voltage control in buck mode and DCM at a load resistance of $R_l = 24\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used.

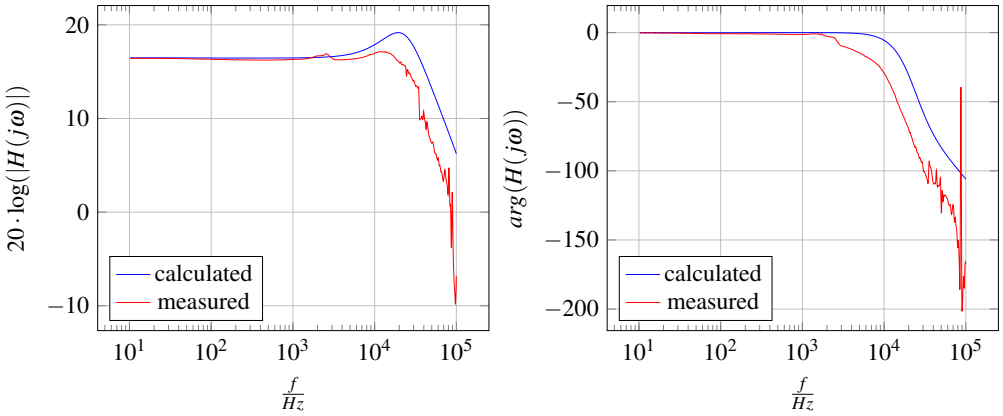


Figure 8.23: Measured and calculated magnitude and phase response of the closed-loop current control circuit of the boost converter in CCM mode at a load resistance of $R_l = 6\,\Omega$. The calculations were conducted using the equations (7.32), (8.35) and (8.39) and (8.37).

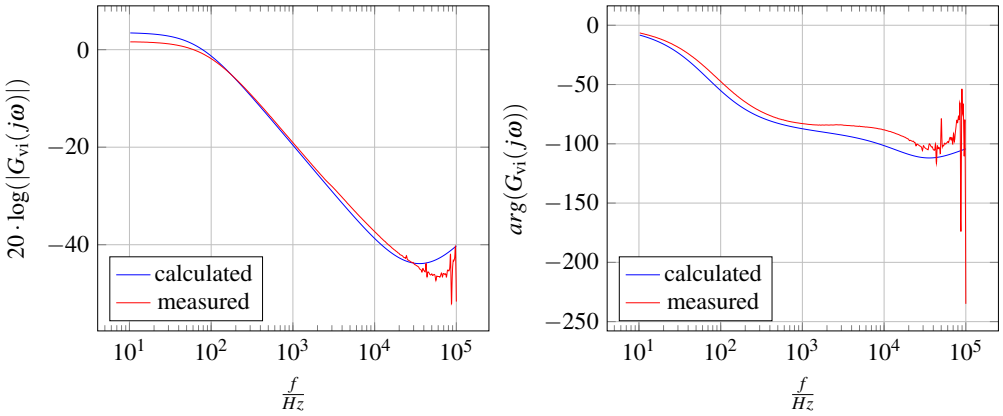


Figure 8.24: Measured and calculated magnitude and phase response of the current to voltage transfer function G_{vi} of the boost converter in CCM mode at a load resistance of $R_l = 6\,\Omega$. For the calculation equation (7.40) was used.

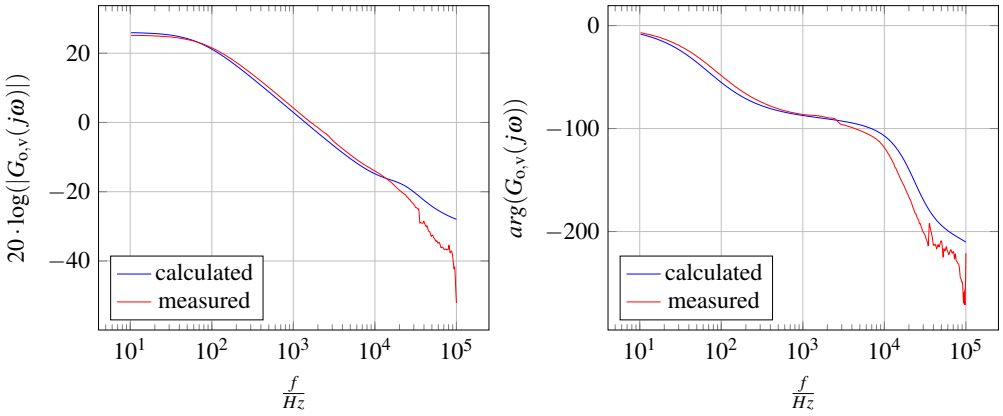


Figure 8.25: Magnitude and phase response of the open loop of the voltage control in boost mode and CCM at a load resistance of $R_l = 6\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used.

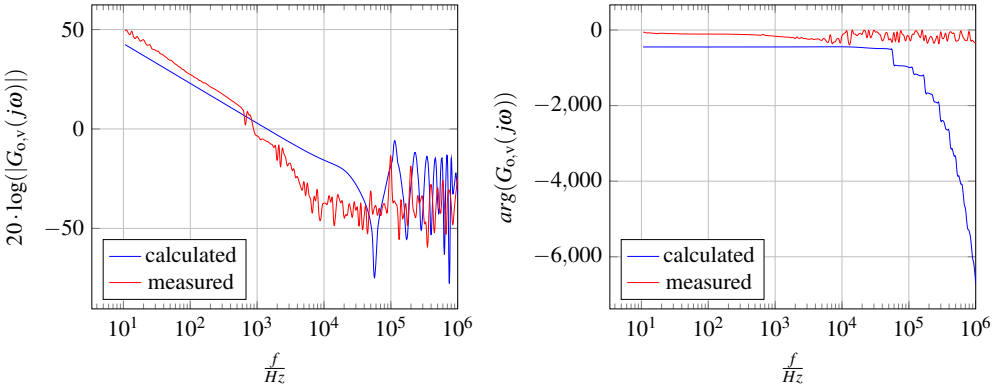


Figure 8.26: Magnitude and phase response of the open loop of the voltage control in boost mode and CCM at a load resistance of $R_l = 6\,\Omega$. The hardware measurements were acquired using the digital controller. For the calculation the equation (8.51) was used.

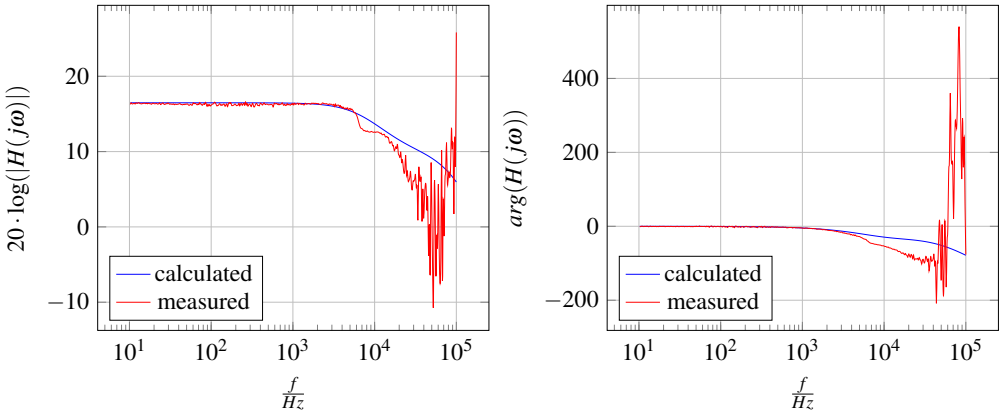


Figure 8.27: Measured and calculated magnitude and phase response of the closed loop current control circuit of the boost converter in DCM mode at a load resistance of $R_l = 24\,\Omega$. Equations (7.41), (8.35), (8.39), and (8.37) served for the calculation.

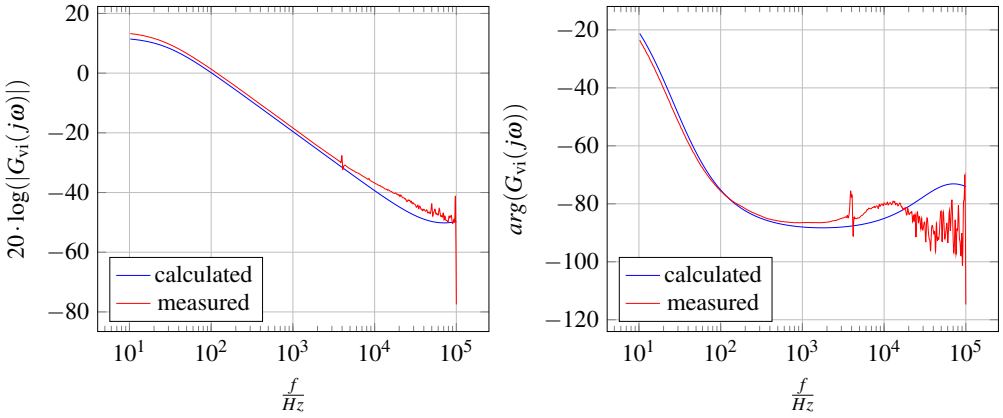


Figure 8.28: Measured and calculated (Equation (7.54)) magnitude and phase response of the current to voltage transfer function G_{vi} of the boost converter in DCM mode at a load resistance of $R_{\mathrm{l}} = 24\,\Omega$.

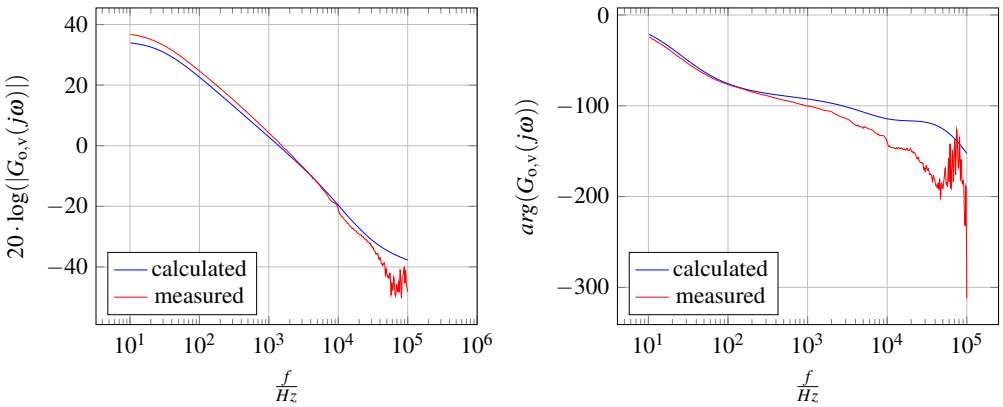


Figure 8.29: Magnitude and phase response of the open loop of the voltage control in boost mode and DCM at a load resistance of $R_{\mathrm{l}} = 24\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used.

9

Battery-State-Aware Load Distribution Control Strategies for a Parallel Connection of Heterogeneous Batteries

Heterogeneous battery management systems combine various batteries in one system. Differences in cell chemistry, nominal capacity, and safe operating areas (SOA) require battery state-dependent load current distribution. The distribution factors have to be adjusted according to the actual battery state during active operation for enhancing safety in a heterogeneous battery system. In the following chapter, general control methods for load sharing between DC-DC converters connected in parallel are first reviewed. This is followed by a review of existing work addressing the management of heterogeneity in the control and operation of battery systems. Two different control approaches are presented: a droop-based method and a novel communication-based one. The droop-based approach emphasizes the distributed control architecture and relies only on local measurements, allowing load sharing without communication and total current measurements. However, limited accuracy is observed due to persistent control deviations. The communication-based approach provides current sharing control without affecting the voltage control, thus ensuring stable voltage control even in the presence of errors, such as incorrect load sharing factors or erroneous total current measurements. The design of both control schemes is described in detail in the following chapter.

9.1 Motivation

Advances in the integration of renewable energy sources are accompanied by increased energy storage demand. Battery storage systems are one possibility to balance the temporal difference between energy supply and demand and to compensate for load and generation peaks. To achieve sufficient battery capacity, the

use of multiple battery modules is required. The parallel connection of the batteries increases the output power, the storage capacity, the reliability, the availability, the fault-tolerance and the modularity of the battery system. Since the battery terminal voltage depends on the battery type, the SoC, and the internal resistance, bidirectional DC-DC converters are required to connect components with different output voltage levels in parallel.

For safe battery operation, it is necessary to limit the (dis)charge current depending on the battery state. Furthermore, a current sharing strategy between the parallel connected bidirectional DC-DC converters, which can be changed during active operation according to the battery states, is required. Even with identical batteries and DC-DC converters an imbalance in current sharing can occur due to component variations, manufacturing tolerances, line resistances, and temperature differences. Even if a current distribution between the components can be achieved at the begin of life of the system, it will not last due to non-identical age-related changes in the components. [391]

In this case, one of the DC-DC converters will take on a majority of the load. This not only leads to inefficiencies and decreased reliability of the system but also accelerates battery degradation due to high (dis)charge currents. In the worst case, the safe operating area of the battery is exceeded, which can have drastic consequences such as thermal runaway, battery fire and system failure. Furthermore, differences in the components used or varying load conditions can lead to output voltage imbalances, which must be compensated by the global control method. Simultaneous operation of DC-DC converters connected in parallel can lead to an interaction of the control loops. This in turn can lead to instability, oscillation or deteriorated control dynamic. The higher-level global control strategy has to include strategies to avoid unwanted interactions between the control loops, for example synchronization procedures. To meet the system requirements of fault tolerance, availability, and reliability, it is necessary that the failure of individual components does not endanger the operation of the DBMS.

In the following, special focus is given to the failure of the global communication and the failure of individual battery components, including failure of the battery itself and the DC-DC converter. Furthermore, for the energy efficiency of the overall system, control strategies are required to take into account the load-dependent efficiency of the bidirectional DC-DC converter. For the heterogeneous decentralized battery system, it is additionally necessary to divide the load current according to the battery state. The motivation for implementing a battery state dependent load distribution approach is to enable the simultaneous operation of batteries with different SOAs. Additional optimizations such as increasing the performance, reliability, availability, efficiency and lifetime of the battery system can be addressed if sufficient battery capacity is available. Heterogeneous batteries exhibit different characteristics such as high power or energy density, high temperature capability, dynamic response, or tolerance to high peak currents. With the battery-state dependent load distribution approach, the different battery characteristics can be optimally utilized. Furthermore, additional objectives, such as achieving a common end of life for all batteries including the second life batteries can be achieved. Usage history can be incorporated into the distribution factor and the load can be distributed more equitably, extending the overall life of the battery system. This additionally reduces the safety risk and the probability of failure. Overall, a load distribution approach in a parallel connection of heterogeneous batteries can provide efficient utilization of the batteries,

balanced deterioration, improved reliability, optimized thermal management, higher performance, and enhanced safety.
The main challenges are to achieve a stable DC link voltage and balanced current distribution between the DC-DC converters connected in parallel in all operating states, including system start-up and shutdown. Voltage stability must not be compromised in the event of sudden load or generation changes or failure of individual components. Furthermore, the control approach must be scalable within a range of $n \in 2 \ldots 64$ DC-DC converters, although realistically, considering the efficiencies of the DC-DC converters, far fewer than $n_{\max} = 64$ DC-DC converters will be used simultaneously.
The control and the load sharing have to be largely independent of the load profile within a predefined range and of the number of active DC-DC converters. Reconfiguration of the system, i.e. adding or removing individual battery nodes, must not seriously endanger the load sharing and voltage stability.
The main contributions of this chapter can be summarized as follows:

- Two different control approaches to realize the load current distribution among parallel connected bidirectional DC-DC converters while maintaining a stable DC line voltage. A droop-based approach is characterized by a complete decentralization of the global control and requires neither a temporary leader nor communication between the nodes. A novel communication-based, load distribution control approach that introduces a superimposed current sharing control in addition to the local average current mode control with outer voltage control is proposed. This approach is characterized by accurate load sharing, but requires communication between nodes and a temporary leader. In turn, the approaches can each be implemented in a hardware- or software-based manner.
- On-the-fly adjustable, battery-state dependent distribution factor are used to share the entire load current among the DC-DC converters. The change of the distribution factors thereby does not endanger the stability of the DC line voltage, nor the security of supply or the safe operation of the heterogeneous batteries.
- The possibility of deactivating specific DC-DC converters as well as the individual current limitation provide the basis for further higher level energy management strategies to implement different optimization targets, i.e. improved energy efficiency by considering the switching losses of the DC-DC converters and the internal resistances of the batteries or increased battery lifetime by reduced (dis)charge current rates.
- The proposed load current distribution approaches are compatible with the system requirements of decentralization, scalability, availability reconfigurability and robustness. Furthermore the local control approaches and the selected hardware are considered in the design of the controller.

The remainder of the chapter is structured as follows: First, existing related works are presented about load distribution control strategies in parallel connected DC-DC converters without specific consideration of batteries. Subsequently, existing works focusing on load distribution in battery systems are reviewed and classified according to the hardware implementation and the control strategy. Subsequently, the droop-based approach to realize load sharing is presented first, followed by the communication-based approach.

9.2 Related Work

In the following, first existing work on general control approaches for load distribution between parallel connected DC-DC converters without explicit reference to battery systems is reviewed. Following this, related work about load distribution and the management of heterogeneity in battery systems is examined. Heterogeneity in this context refers to differences in battery performance metrics such as SoC on the one hand, and differences in cell chemistry and capacity on the other hand.

9.2.1 General Load Distribution Approaches

Systems consisting of DC-DC converters connected in parallel make it possible to increase output power and improve reliability and maintainability. One of the main challenges in parallel connection of DC-DC converters is to ensure voltage stability and balanced current distribution between all active DC-DC converters [392]. Existing work on load sharing control strategies is reviewed below. First, fundamental and overview work is shown. This is followed by a listing of the most relevant load distribution strategies categorized by their architecture. Digital control approaches for load distribution are considered independently of their underlying architecture. Finally, decentralized approaches without the need for a central control unit, which are also referred to in the literature as democratic and team-oriented, are discussed in more detail. Existing work on load sharing strategies in input series output parallel connected DC-DC converters, e.g. approaches like this [393], are thereby excluded. In [394], the circuit theory of parallel connected DC-DC converters is first considered and subsequently parallel circuits with and without current-sharing loops are compared in terms of performance and load sharing. The necessity of current sharing loops is thereby demonstrated. Another model of parallel connected DC-DC converters is presented in [395].
A commonly used classification of load sharing control strategies is the subdivision into droop based and active current sharing mechanisms [322, 396]. The latter include, for example, peak and average current sharing as well as different master slave approaches (fixed, rotating or automatic master). A description of the control approaches as well as their advantages and disadvantages can be found in [322, 396–398].
From the control point of view, parallel connections of DC-DC converters can be considered as multi-agent systems for which centralized, distributed, or decentralized control strategies can be implemented (Fig. 9.2).
The droop control belongs to the decentralized control approaches for load distribution. In conventional droop control, an additional resistor is added to the output characteristics of the individual DC-DC converters to achieve the desired load sharing [399–410]. There are approaches which use real resistors or virtual resistors. The latter has advantages in terms of power dissipation and adaptability of the droop resistor value. The droop resistor causes the DC-DC converter output voltage to drop as the load increases. The instantaneous value of the output voltage, together with the droop resistance curve, serves as the basis for determining the output current. Droop control is a robust, fully decentralized load sharing approach based on local measurements only. However, load sharing between DC-DC converters requires that a sufficiently large voltage droop occurs [391]. The droop control can be optimized with respect to either optimal voltage control or load sharing. There are

numerous approaches to improve voltage regulation and load sharing: One possible approach to improve the accuracy of load current sharing is to consider the line resistances [411, 412].
Another possibility is to introduce additional secondary and tertiary controllers. In this case, the droop control is the local, primary controller in a hierarchical control architecture [413, 414]. The higher control layers compensate for the remaining control deviation and adjust the droop resistances for improved load distribution. This improves the control accuracy. There are also approaches that use non-droop based primary controllers [415].
Besides the droop based control, the master slave control is widely used. It belongs to the centralized control strategies and to the active current distribution methods [416–426]. The aim is to distribute the load to different DC-DC converters equally or proportionally to their rated power. For this purpose, one of the DC-DC converters becomes the master and controls the output voltage, while it specifies the setpoints of the other DC-DC converters, which operate as slaves. Despite its simplicity, the master-slave architecture is prone to failures, since the master converter represents a single point of failure in such structures. A variation of the master slave architecture is central current limit control.

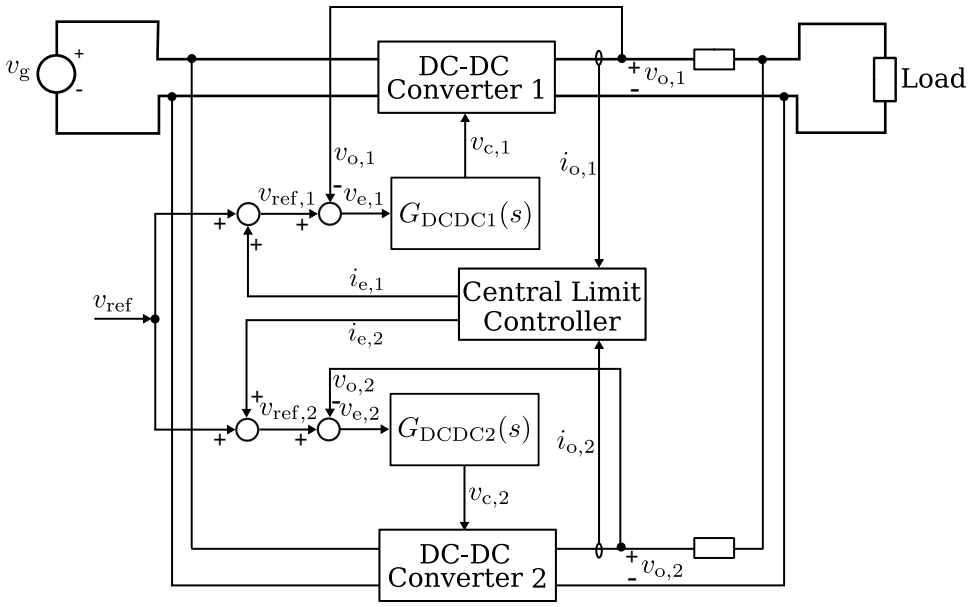


Figure 9.1: Block diagram of the central control limit with individual voltage feedback path and dynamic voltage reference for two DC-DC converters connected in parallel. [427–430]

Central current limit control [427–431] is one of the centralized load current distribution approaches. To control the voltage across the common load, the instantaneous voltage value is acquired by the voltage feedback loops. The PWM control voltage for each DC-DC converter is compensated by an appropriate current error signal corresponding to the difference between the desired and the actual output current of the converter to achieve the desired load distribution ratio. The figure 9.1 shows a central current limit control with independent voltage feedback and dynamic voltage reference. Thereby the output voltages of the parallel connected DC-DC converters, in this case two, are controlled independently from each other. The DC-DC converters are regulated to different output voltage levels to achieve the desired current sharing ratio. There are also approaches with fixed voltage references

and a common voltage feedback. Furthermore there are approaches to compensate the effects of different cable lengths. They lead to varying cable impedances and consequently to irregularities in the current distribution. The approach in this case is mainly limited to a suitable selection of an output resistor. [427, 428] Even with the introduction of a dedicated controller, the disadvantage remains that central control units form a single point of failure and significantly endanger reliability and system availability.
Distributed control approaches use local information to achieve global goals while minimizing the need for communication [432–437]. For example, DC bus line voltage measurement is used as local information and basis for control. For load sharing between nodes, different output resistances or varying reference voltages are additionally used to determine the duty cycle of the PWM signals. Communication between the neighboring nodes enables adjustments of the sharing factors. The communication is usually a point-to-point connection between the DC-DC converters. While centralized, hierarchical and distributed approaches have only been considered in a general way, a more detailed review of decentralized, also called democratic or team-oriented, approaches is provided in the following. The reason for this is that the approach presented in this thesis differs significantly from the others due to its architecture. There are architectural similarities among the existing decentralized approaches, which is why a clear distinction is drawn between them and a more detailed description is given below.

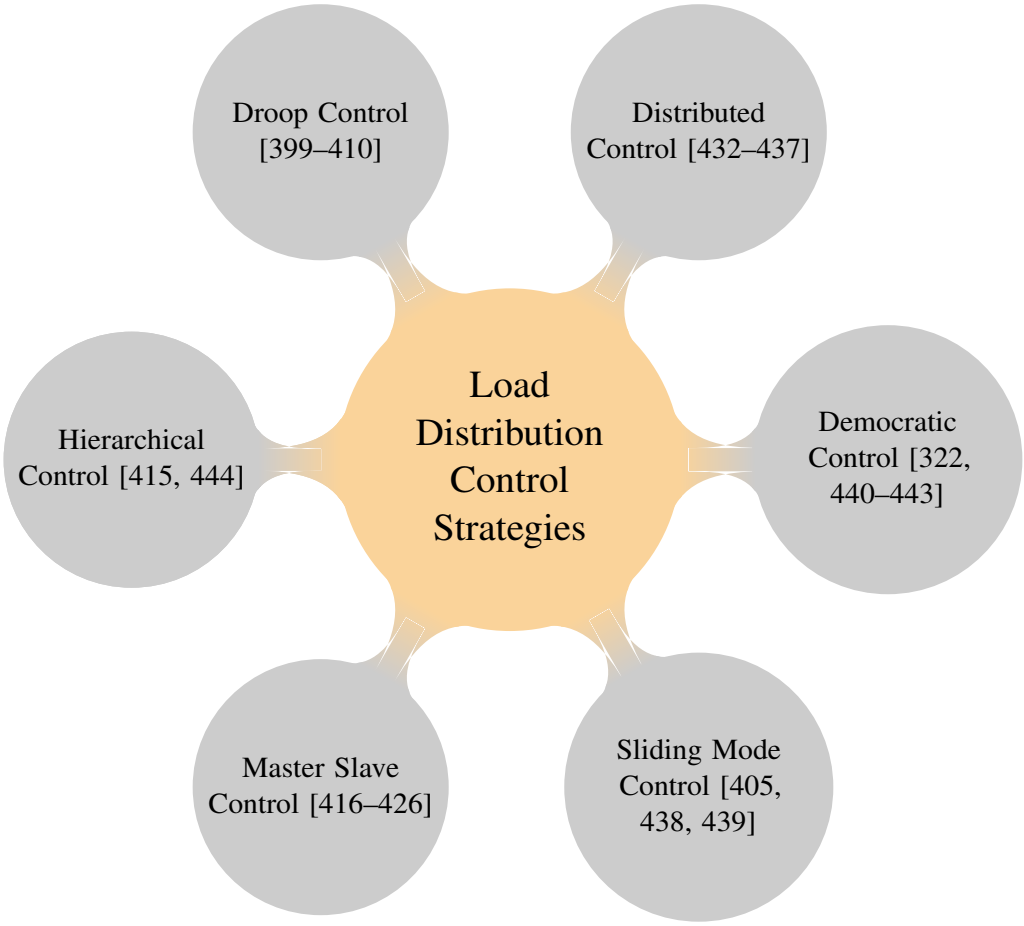


Figure 9.2: Overview of the most relevant control strategies for load distribution of parallel connected DC-DC converters categorized by the underlying control architecture.

A decentralized, team-oriented load distribution control approach for a parallel connection of DC-DC converters in buck mode is proposed [445], which does not require a central control unit. For accurate voltage control and load sharing, a cascaded control loop consisting of an inner voltage control loop and an outer current control loop is applied. A local election protocol is implemented to determine the output currents. The nodes compare their local current values with the averaged current values of all nodes and, if necessary, adjust the reference voltage and consequently the local voltage setpoints. A division according to the output power of the DC-DC converters is possible, so that various ones can be combined. As different local voltage measurements have affected the current control and distribution, averaging voltage estimators are introduced. The proposed control structure is different from the one proposed below. Furthermore, no change in current sharing factors is implemented in this approach. In addition, neither boost mode nor differences for the control of the system depending on the CCM and DCM are addressed. A drawback of the proposed approach is the reliance on a working communication. In case of complete communication failure between the nodes, the current ratings can no longer be determined and the voltage estimators can neither be used. [445]
In the approaches [440] and [441] democratic load sharing is defined in such a way that the sharing of the total current is proportional to the total output current rating of the corresponding DC-DC converter. This load distribution strategy does not require a master nor a central controller. For correct load sharing, either the correct sharing factors must be initially stored or communication between the DC-DC converters is required to determine the nominal current ratings. The first approach is unsuitable for reconfigurable systems and limits flexibility. With either approach, it is unclear whether voltage regulation and load sharing will remain stable if one of the DC-DC converters fails. With the communication-based approach, it is at least possible to detect the failure and update the sharing factors. Both approaches have limits in the adaptability of load sharing factors and robustness.
In the decentralized multi-agent approach [442], there are control and consumer agents, both of which have the identical basic tasks of measuring the output voltage and calculating the global total current. Initially, a negotiation is performed between the agents and one of them becomes the active agent, while the others change to the passive state. The active agent coordinates the system while the passive ones do not make any decisions but only receive messages. Only in case of failure or restart of the system a new active agent is chosen.
The load current sharing strategy takes into account a cost function so that the DC-DC converters are operated as efficiently as possible, i.e. at operating point with maximum efficiency. The strategy provides that $n-1$ DC-DC converters operate in their optimal operating range while the n_{th} converter provides the required residual current. The burden on the n_{th} DC-DC converter is not analyzed in detail. This is especially critical when considering the application investigated in this case in a battery system, since it is not possible here for one of the battery node to supply arbitrarily high currents to compensate for the control deviation.
A fully decentralized masterless system is proposed in [443]. The parallel connected DC-DC converters are each controlled independently by their own FPGA-based digital controller and are interconnected via CAN lines. The load current is dynamically shared between the nodes in a predetermined manner, in this case proportional to a weight. A method to compensate for voltage measurement errors is proposed, as well as an approach that allows all converters to automatically time-shift

their PWM gate signals to minimize current ripple (interleaving). The system is suitable for reconfigurable systems and is characterized by high reliability due to the autonomous DC-DC converters. It is not clear from the description whether the current control is a peak or average current mode control. The latter is required for optimized battery operation and is used in the proposed approach.

9.2.2 Management of Heterogeneity in Battery Systems

Load distribution strategies are required in heterogeneous battery systems to manage the physical differences of the batteries. These include differences in SoC, nominal capacity, and terminal voltage. Figure 9.3 shows an overview of control strategies for managing heterogeneity in battery systems. The term heterogeneity is also used for systems with batteries of the same chemistry and differences in SoC and remaining capacity. Approaches for batteries of identical chemistry with differences in SoC or SoH are also included, as they still form the majority.

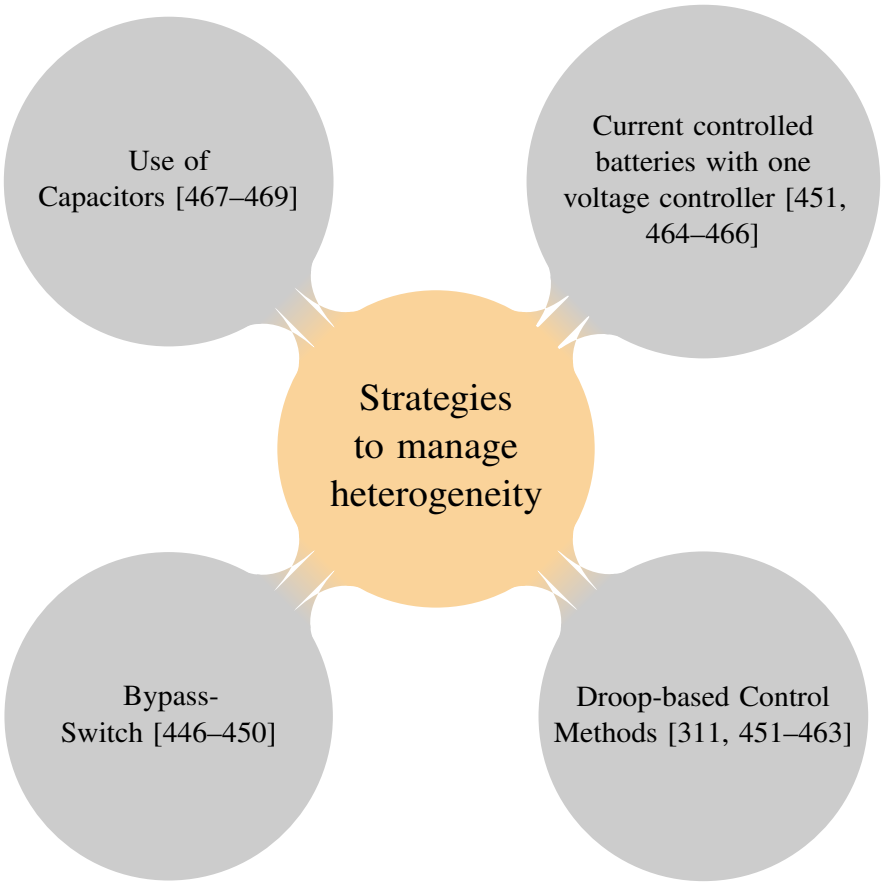


Figure 9.3: Overview and categorization of common strategies to manage heterogeneity in battery systems.

One approach is to use switches. Each cell is equipped with at least one switch. Depending on the architecture, there is the possibility to separate the cells from the rest of the pack (bypass switch) or, in more sophisticated approaches, to dynamically reconfigure the architecture and connect a number of cells in series or in parallel. The advantage of this approach is that the battery module can still be operated safely even if individual cells fail. Furthermore, no additional power electronic components are required. A battery-state aware load distribution is possible with this approach and the SoC can be balanced without additional re-charge transfer

losses. With regard to the use of cells with different battery chemistries, it should be noted that cells with different nominal output voltages cannot be connected in parallel without additional components [450]. Even in the case of cells with identical nominal terminal voltages, high equalization currents may occur with in the event of significant differences in SoC [32]. Thus, only the connection of cells with similar output voltage characteristics is possible. Furthermore, for reliable system operation, it is necessary to monitor the condition of the batteries and switches and to control the large number of switches. The use of additional DC-DC converters at the battery module level [448] allows the combination of battery modules of different terminal voltages, whereby the implementation issues regarding the power electronic topology and the challenge of the coordination of all the switches are not addressed.
One way to compensate for different nominal output voltages is to use coupling capacitors. This also offers, for example, the possibility of combining energy- and power-dense batteries in one system. The supercapacitors are used to achieve DC decoupling and a significant reduction in circulating currents. For example, one possibility is to connect the power-dense battery pack with a supercapacitor [467]. This allows the power-dense battery to take over only high frequency power transients and thus inherently creates load current sharing between the batteries. This allows the connection and simultaneous use of different batteries with different energy and power characteristics. However, the SoC, the SoH and the actual capacity are not considered in the load current sharing. For balanced SoC, an additional active BMS is required to control the recharge currents.
In systems with batteries connected to DC-DC converters, another approach is to operate several batteries in a current-controlled manner and to use an outer voltage control loop. The advantage here is that the battery current can be limited according to the actual battery state. For accurate voltage control it is required that one component, usually a battery, compensates for the voltage deviation regardless of the current battery state. Furthermore, a fixed allocation is usually used. As a result, the component responsible for voltage control forms a potential single point of failure.
Similar to the general load distribution strategies for parallel connected DC-DC converters, droop based approaches dominate the control strategies for managing heterogeneity in battery systems. To deal with different battery parameters, a virtual droop resistor is usually used, and in some cases a virtual capacitance is added. There are numerous approaches to improve the load distribution accuracy in droop-based control. High load sharing accuracy is achieved with stable voltage control. However, droop-based approaches do not allow accurate current control, as is the case, for example, with the average current mode control. The charge and discharge current (C-rate) is a crucial factor for battery degradation-aware operation. In most cases, the amount of current directly affects degradation, i.e. the lower the current flowing through the battery, the longer the battery life [470].
There are numerous approaches for load distribution between DC-DC converters connected in parallel and for managing heterogeneity in battery systems.
However, there is still no approach that provides accurate average current mode control with local voltage control loops distributed across all battery components, while additionally providing battery state dependent load distribution. In the following, an approach is described that fulfills these characteristics and, in addition, meets the system objectives of reliability and availability using a decentralized, scalable architecture.

9.3 Communicationless Droop-based Control

Droop-based control is fully decentralized and does not require communication between the nodes or a centralized control authority for coordination. The nodes operate completely autonomously and the control is based solely on local measurements and calculations. These characteristics result in this control approach having high robustness and a reduction of potential single points of failures. No communication between nodes is required, which has a positive effect on the scalability of the system and the control dynamics by eliminating delays due to message latencies. By choosing an appropriate droop characteristic, load sharing can be implemented between a diverse mix of different energy storage devices, including, for example, fuel cells in combination with different batteries.
The main challenge is to achieve accurate load sharing between the components. Furthermore, it is not possible to realize a precise voltage control. The robust, communicationless approach based on local measurements is nevertheless the control strategy of choice during leader election, when communication errors or communication failures are detected, or during operating states that require increased computational effort like system start up or software update processes.

9.3.1 Technical Background on Droop-Based Control

The output characteristic of a DC-DC converter corresponds approximately to an ideal voltage source. The output voltage is thereby independent of the output current:

$$V_{\text{out}}(I_{\text{out}}) = V_{\text{out}} \tag{9.1}$$

For a parallel connection of n DC-DC converters, the current through the converter is dominated by the parasitic elements of the components. In the worst case, one of the DC-DC converters takes over the entire load, which can lead to overloading and overheating, and consequently to component failure and reduced system availability. A commonly used method for controlling load sharing is the Droop-based control. Mathematically, this is a modification of the output characteristic. The DC-DC converter characteristic has the form of a linear function with a negative slope (Fig. 9.8). There are two basic methods to realize this.

a) Additional Resistor for Adjustment of the DC-DC Converter Internal Resistance For a DC-DC converter with low power, an additional resistor can be connected in series. This additional resistor is called droop resistor and together with the internal resistance of the DC-DC converter determines the load sharing between the components.
The output voltage results in:

$$V_{\text{out,n}} = V_{\text{n}} - r_{\text{d,n}} \cdot i_{\text{n}} \tag{9.2}$$

Each voltage is thus assigned to a distinct current value. The negative slope results in a stable operating point for converters connected in parallel. A real internal resistance is only used for DC-DC converters with very low power due to high power losses.

b) Virtual Internal Resistance for the Setting of the Droop Characteristic At higher output powers, the droop characteristic is simulated by a virtual droop resistor

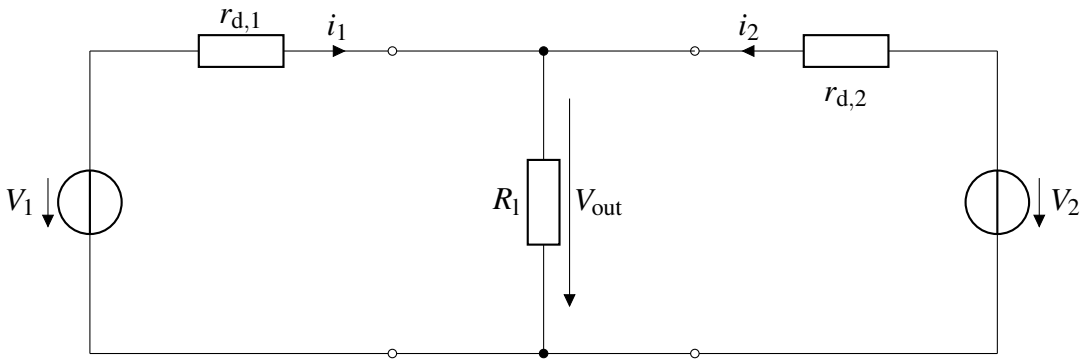
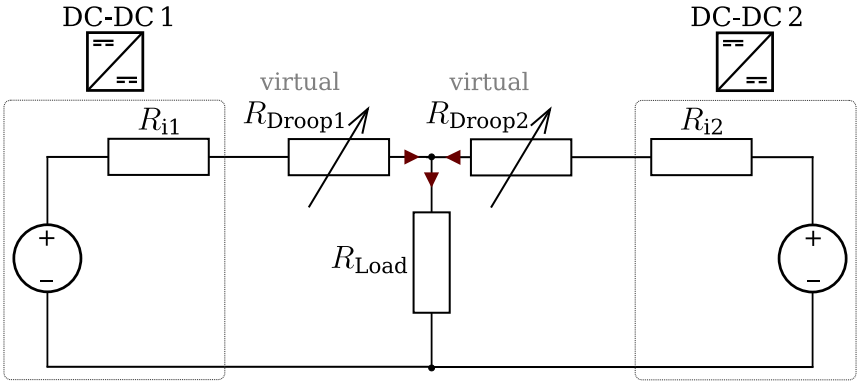


Figure 9.4: Equivalent circuit diagram of the droop control where the load sharing between the DC-DC converters, in this case two, is set via the droop resistances r_{d1}, r_{d2}.

for the setpoint modification.

$$v^*_{ref} = v_{ref} - r_d \cdot i_{out} \tag{9.3}$$



$$\left.\begin{aligned} V_{Load} &= V_{DC/DC1} - (R_{i1} + R_{Droop1}) \cdot I_1 \\ V_{Load} &= V_{DC/DC2} - (R_{i2} + R_{Droop2}) \cdot I_2 \end{aligned}\right\} \quad I_1 = \frac{R_{i2} \cdot R_{Droop2}}{R_{i1} \cdot R_{Droop1}} \cdot I_2$$

Figure 9.5: For higher output powers, the droop resistor is implemented virtually in order to reduce the power dissipation. The reference voltage is adjusted using the virtual resistance according to Equation (9.3).

The droop-based control is accompanied by limitations in the control accuracy of the voltage.

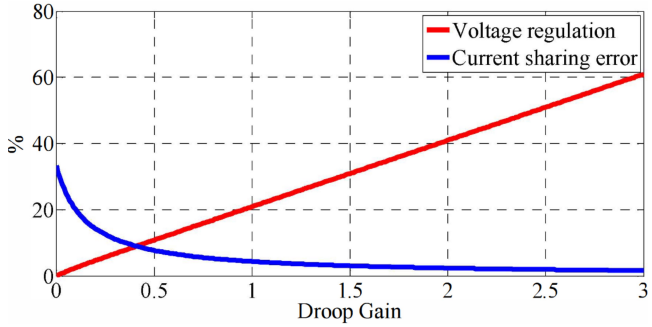


Figure 9.6: Course of the current distribution error over the droop resistor [471]

With the conventional droop control according to Equation (9.3), the deviation from the setpoint increases with the value of the droop resistor r_d. To correct this error, a corresponding adjustment of the setpoint is required. There are numerous different adaptive methods, for example [472], [473], to adjust the reference voltage.
Another method to reduce the error is to use a higher order polynomial instead of a linear (Equ.(9.3)) in the output characteristic.
The reference voltage without adaptation is generally defined as:

$$v^*_{\text{ref}} = v_{\text{ref}} - r_{\text{d}} \cdot i^{\alpha}_{\text{out}} \tag{9.4}$$

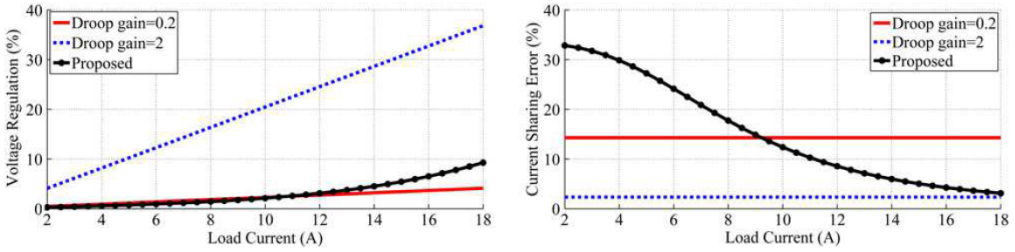


Figure 9.7: Droop control methods to reduce the error [471], black curve based on Equation (9.4), red and blue curve based on Equation (9.3).

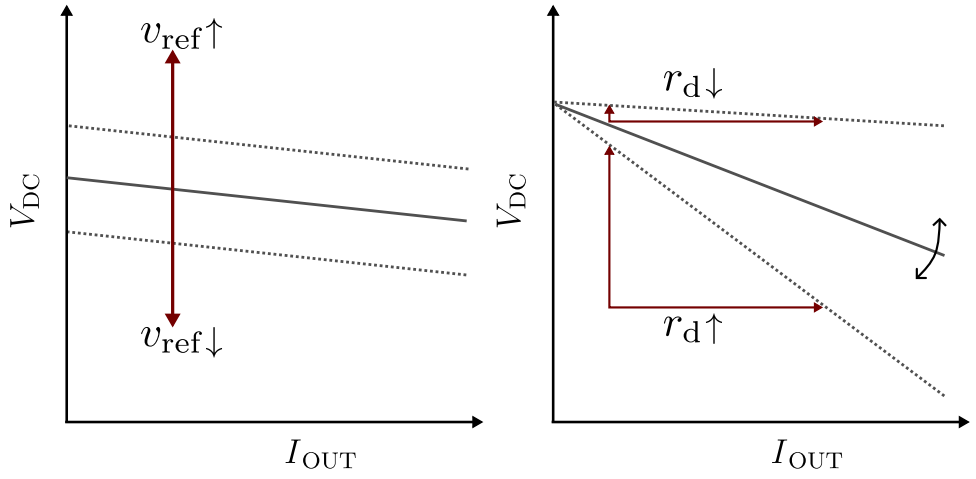


Figure 9.8: Example of the implementation of the droop-based control at local level. Two software variables v_{ref} and r_{d} are used to set the level of the voltage to be controlled and the slope of the droop characteristic.

Droop control is a compromise between a voltage control close to the set point or an accurate load current distribution. Figure 9.7 shows a variant of the droop-based control which focuses on accurate voltage control. Only minor deviations from the voltage setpoint occurs. Simultaneously, a significant error occurs in the load current distribution, which in turn decreases significantly with higher output power.
For the analysis of the control behavior of parallel connected DC-DC converters with current control and the load sharing between them by the means of droop control, a general control loop is deduced first (Fig. 9.9). In the following, structurally identical DC-DC converters are considered, whereby these are also distinguished by manufacturing tolerances and differences in aging effects (parasitic resistances) due to, e.g. varying operating temperature or workload.

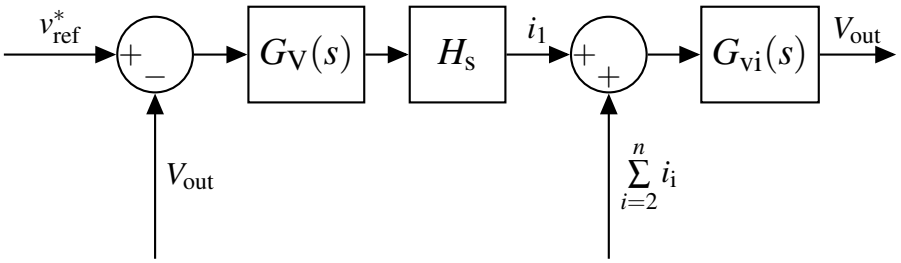


Figure 9.9: General control loop of the parallel connection of structurally identical DC-DC converters with current control and a droop based control for voltage control and current distribution. In this case a parallel connection of two DC-DC converters is considered.

According to the control loop, the following equation follows for the output current i_1 of one DC-DC converter:

$$i_1 = (v_{\text{ref}} - r_{\text{d}} \cdot i_1 - V_{\text{out}}) \cdot G_{\text{V}}(s) \cdot H_{\text{s}} \tag{9.5}$$

The equations for the output currents of all further DC-DC converters i_2 to i_n are equivalent to Equation (9.5).
The sum of the currents considering Equ. (9.5) results in:

$$\frac{\sum_{i=1}^{n} i_i}{H_{\text{s}} G_{\text{V}}(s)} = n \cdot v_{\text{ref}} - \sum_{i=1}^{n} (i_i \cdot r_{\text{d,i}}) - n \cdot V_{\text{out}} \tag{9.6}$$

For the DC-DC converter output voltage applies:

$$V_{\text{out}} = \sum_{i=1}^{n} i_i \cdot G_{\text{vi}}(s) \tag{9.7}$$

From the equations (9.6) and (9.7) the voltage transfer function follows accordingly:

$$\frac{V_{\text{out}}}{v_{\text{ref}} - \frac{\sum_{i=1}^{n} i_i \cdot r_{\text{d,i}}}{n}} = \frac{n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}}{1 + n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}} \tag{9.8}$$

Equation (9.8), explicitly the denominator $v_{\text{ref}} - \frac{\sum_{i=1}^{n} i_i \cdot r_{\text{d,i}}}{n}$, shows that there is a remaining deviation from the voltage setpoint.

9.3.2 Hardware-based Implementation of the Droop Control

Since droop control is a robust control method that does not require communication and is based purely on local measurements, it is used as a fallback control strategy. In the following, the implementation of a droop control with the use of a virtual resistor and the hardware-based analog control is explicitly described. The droop-based control is used in the system only as a fallback control strategy in combination with the analog control. An implementation with the software-based, digital control is also possible, but is not considered here in more detail. The reason for this is that digital

control shows its advantages when, for example, different sets of control parameters corresponding to different load ranges are required for optimum control. This is not the case with droop control. Changes to the virtual droop resistor are carried out flexibly in the software and are subsequently taken into account in the calculation of the reference voltage (Equ. (9.4)). The microcontroller performs the calculation and provides the reference voltage v_{ref} via the digital to analog converter.
In buck mode, the voltage to be controlled corresponds to the low side voltage V_{LV}. It is dimensioned via a voltage divider and compared with the reference voltage v_{ref} to determine the control deviation. The setpoint to actual value comparison provides the voltage V_{ISETA}, which corresponds to the reference voltage v_{c} for the downstream average current mode control.
The same applies to the boost mode with the difference that the voltage to be controlled corresponds to the high side voltage V_{LV}.

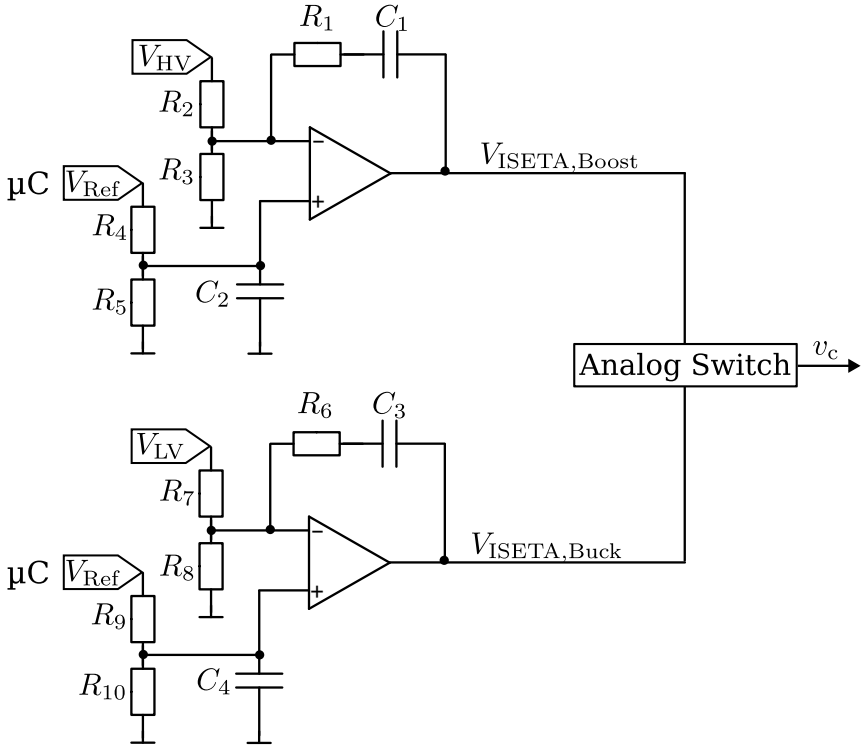


Figure 9.10: Circuit for the implementation of analog control. Since the control paths for buck and boost mode are different, two separate controllers are required, which differ in the dimensioning of the electrical components. The droop control is realized by a virtual impedance. A reference voltage determined according to Equation (9.4) is specified via the digital to analog converter of the microcontroller.

9.3.2.1 Topology of the Droop-based Controller

The path behavior of the bidirectional DC-DC converter in buck mode differs from the one in boost mode. Therefore two separate analog implemented controllers are required.
The voltage divider resulting from the resistors R_1 R_3 and R_2 R_3 is referred to as G_{Merge} hereafter.
The controllers are switched on in a complementary manner. To avoid unwanted current flow between the controllers, the diodes D_1 and D_2 are used (Fig. 9.11). For switching off the controllers, the reference voltage v_{ref} is set to 0 V by a MOSFET.

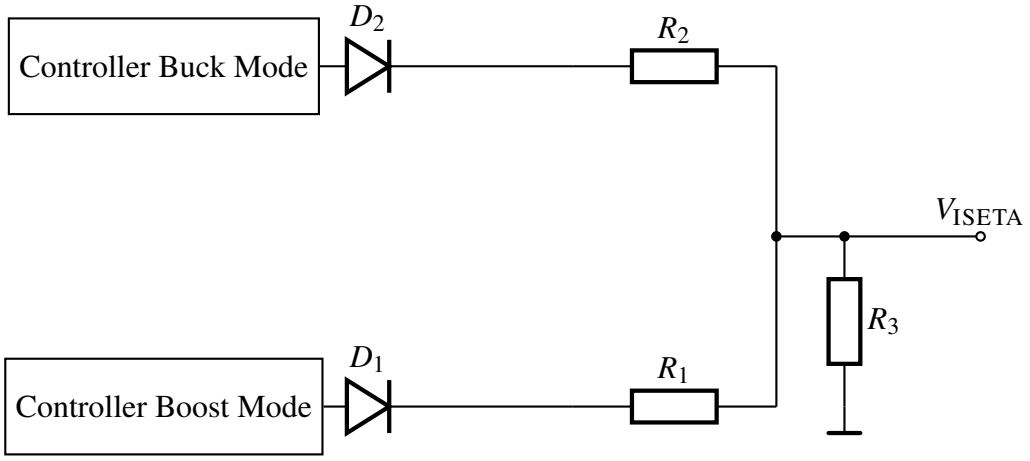


Figure 9.11: Merging the controls for buck and boost mode. The resulting voltage divider is referred to as G_{Merge} hereafter.

9.3.2.2 Switch between the Controllers

The first hardware implementation of the analog controller (Fig. 9.12) showed that the voltage V_{ISETA} had an offset of $100\,mV$. Since the voltage V_{ISETA} is the current controller reference voltage v_{c} for the average current mode control, this offset led to erroneous output currents.
After some analysis and measurements, it appears that the controller shutdown circuit is the source of this voltage offset. In the real setup, a resistor of 20Ω was used for R_{A}. The result was that a voltage dropped across it. This voltage was amplified and superimposed to the control signal of the opposite controller. Also using $R_{\text{A}} = 0$ the offset error does not approach zero. The voltage drop across the transistor is also shown to be significant and clearly measurable. To cancel the interactions between the controllers, an analog switch for merging the two analog controllers was included in the subsequent implementations (Fig. 9.13).

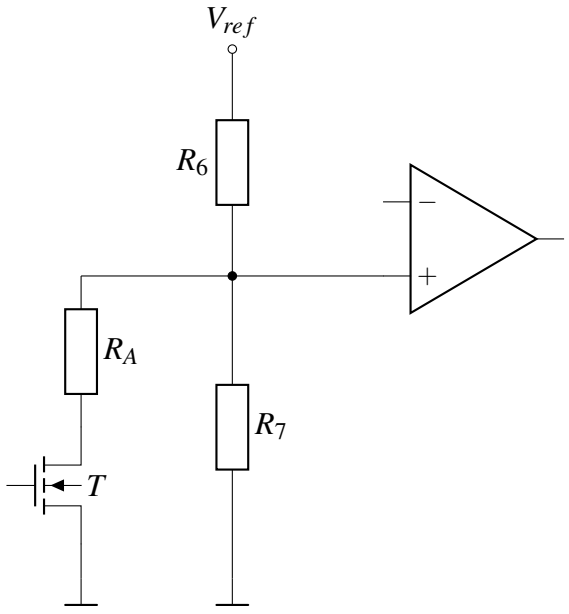


Figure 9.12: First hardware implementation of the controller shutdown circuit causing offset voltages.

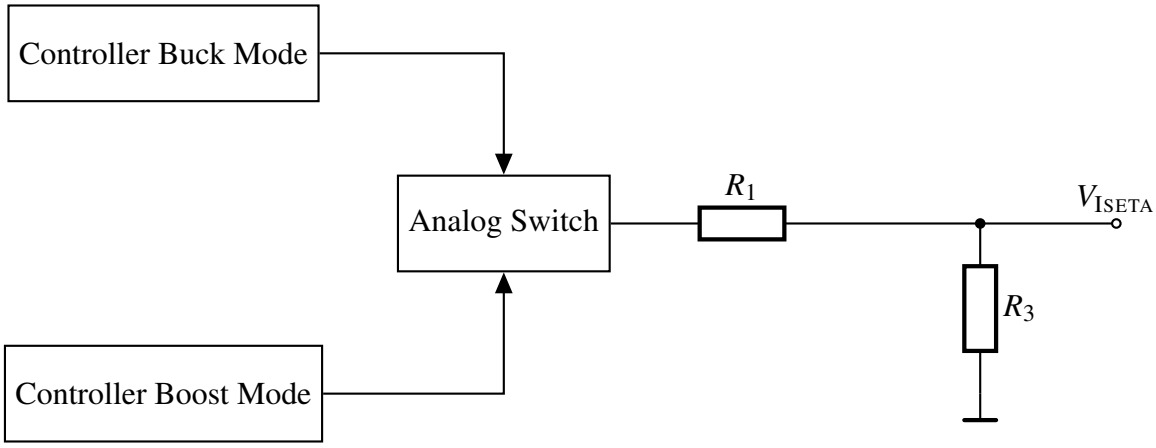


Figure 9.13: In subsequent hardware implementations, an analog switch is used to change between the controllers according to buck and boost mode.

9.3.2.3 Limitation of the Output Signal

The analog controller is followed by the limitation of the control signal. This limits the current through the DC-DC converter and thus there are no exaggerated demands on the source and converter. This is realized by an operational amplifier circuit.

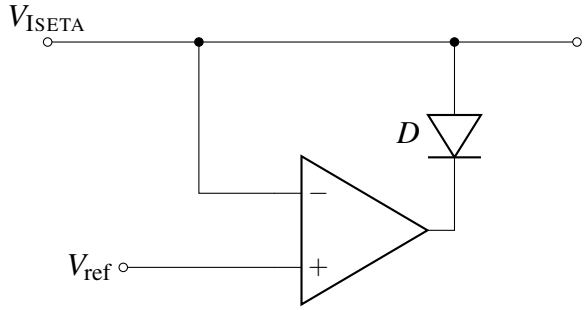


Figure 9.14: Circuit to limit the output signal.

If the voltage V_{ISETA} is greater than the reference voltage V_{ref}, current flows through the diode D and the value V_{ISETA} settles to the value of the reference voltage V_{ref}. In the initial hardware implementation, a bipolar operational amplifier was used. The maximum differential drive of this operational amplifier was exceeded. The result was the saturation of an input transistor and consequently the increase of the input current. This caused an offset voltage of $100\,mV$ via the voltage divider of the controller. The corrective for this is an operational amplifier with based ond CMOS technology, which has nearly no input current.

9.4 Communication-based Load Distribution Control

For safe operation of batteries connected in parallel with DC-DC converters, an additional control strategy for load distribution is required. The described droop-based control already offers a variant to distribute the load between parallel connected DC-DC converters based on local measurements. The realization based on virtual impedances offers additional advantages: Compared to the hardware-based realization the power dissipation is lower and by software changeable droop resistors offer improved flexibility. The droop resistors can be changed during active operation,

which allows to account for the battery condition. A significant disadvantage is, that the droop-based control remains a trade off between accurate voltage control or precise load distribution.
An exact current distribution according to the battery state is not possible with the droop-based control and according to Equation (9.8) it is evident that a voltage deviation remains, even if it is minor. Therefore, a novel communication-based load distribution strategy for DC-DC converters connected in parallel is presented hereafter. The load distribution factors α_n, $n \in 0 \ldots 63$, are specified by one of the nodes, the temporary leader, via the communication line, in this case based on CAN FD. For safe or even optimized battery operation according to different goals, such as lifetime or costs, it is necessary that the load distribution factors can be adjusted during operation and that they are kept as accurate as possible.

9.4.1 Control Structure of Communication-Based, Battery State-Dependent Load Distribution

The basis for a battery state-dependent load distribution is an accurate control of the (dis)charge currents. For reliable supply of the loads, it is also necessary to keep the DC link voltage at the specified setpoint. For this purpose, the average current mode control with an outer voltage control loop is used, which was analyzed in detail in chapter 8. For load distribution among the DC-DC converters, an additional superimposed feed back control is added. Figure 9.15 shows the overall control structure for one of the DC-DC converters, whereby the total number of DC-DC converters is $i = 2$ in the shown case. In the following, the elements of the load distribution control are analyzed in detail.

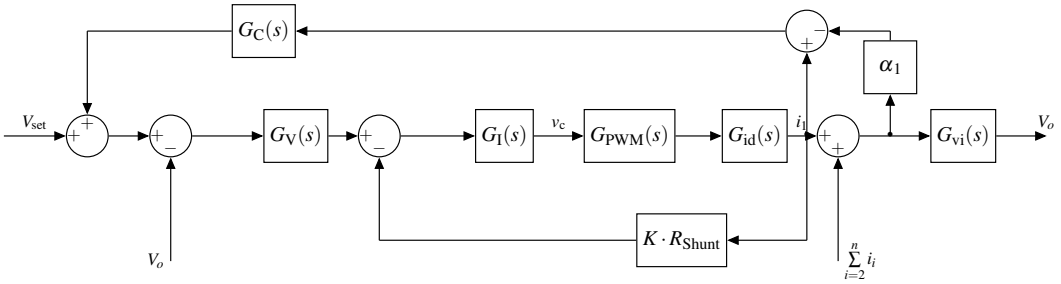


Figure 9.15: Structure of the load distribution control and average current mode control with outer voltage control: An additional superimposed control loop has been introduced for load distribution according to the distribution factor α_i.

9.4.2 Reference Transfer Functions of the DC-DC converter

Initially, the reference transfer function, which describes the relation between the output variable and the setpoint, is determined. From this, the steady-state and dynamic behavior of the system can be derived and the system stability can be deduced. For the description of the reference transfer function, the inner current control loop H_s (Fig. 9.15) is summarized to a single block:

$$H_\mathrm{s} = \frac{G_\mathrm{I}(s) \cdot G_\mathrm{PWM}(s) \cdot G_\mathrm{id}(s)}{1 + K \cdot R_\mathrm{Shunt} \cdot G_\mathrm{I}(s) \cdot G_\mathrm{PWM}(s) \cdot G_\mathrm{id}(s)} \tag{9.9}$$

The block diagram of the entire control structure according to figure 9.15 is simplified to the representation in figure 9.16.

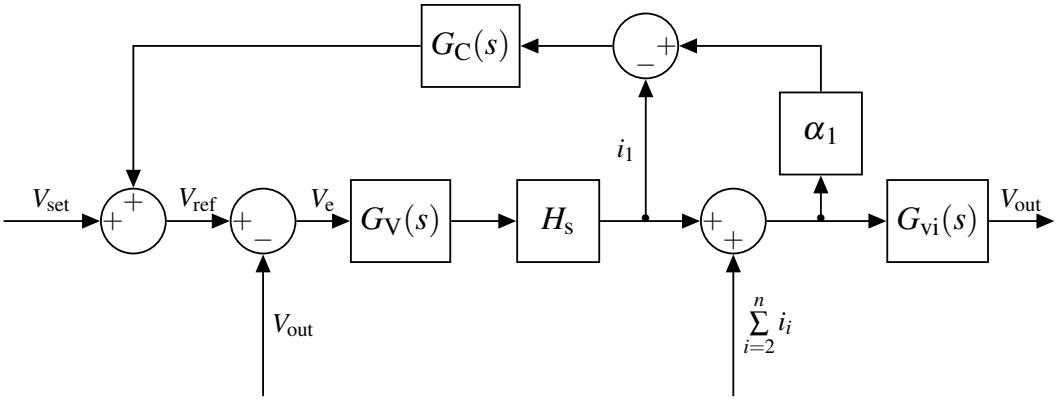


Figure 9.16: Complete control loop of the load distribution control with summarized, closed inner current control loop H_s.

The following equations can be derived from the control loop (Fig. 9.15):

$$V_{ref} = V_{set} + G_C(s)\left(\alpha_1 \sum_{i=1}^{n} i_i - i_1\right) \tag{9.10}$$

$$V_e = V_{ref} - V_{out} \tag{9.11}$$

$$i_1 = H_s \cdot G_V(s) \cdot V_e \tag{9.12}$$

$$V_{out} = G_{vi}(s) \cdot \sum_{i=1}^{n} i_i \tag{9.13}$$

$$\alpha_i = \frac{i_i}{\sum_{i=1}^{n} i_i} \tag{9.14}$$

9.4.2.1 Reference Transfer Function of the Voltage Control Loop

The reference transfer behavior of the voltage control loop can be derived from the Equations (9.10)–(9.14):

$$\frac{i_1}{H_s \cdot G_V(s)} = V_{set} - V_{out} + G_C(s) \cdot \alpha_1 \sum_{i=1}^{n} i_i - G_C(s) \cdot i_1 \tag{9.15}$$

The equations for the currents i_2 to i_n are equivalent. From the definition of α_i corresponding to Equation (9.14) follows:

$$\sum_{i=1}^{n} \alpha_i = 1 \tag{9.16}$$

The sum over all currents results in:

$$\begin{aligned} \frac{1}{H_s \cdot G_V(s)} \cdot \sum_{i=1}^{n} i_i &= n \cdot V_{set} - n \cdot V_{out} + G_C(s) \cdot \sum_{i=1}^{n} i_i - G_C(s) \cdot \sum_{i=1}^{n} i_i \\ &= n \cdot V_{set} - n \cdot V_{out} \end{aligned} \tag{9.17}$$

Considering the Equation (9.13), the relation between the setpoint voltage V_{set} and the DC-DC converter output voltage V_{out} results in:

$$\frac{V_{\text{out}}}{V_{\text{set}}} = \frac{n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}}{1 + n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}} \tag{9.18}$$

The open loop transfer function for the voltage control ($G_{\text{o,v}}$) depends on the number of DC-DC converters connected in parallel. In addition, the voltage control is shown to be independent of the current control:

$$G_{\text{o,v}} = n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}} \tag{9.19}$$

9.4.2.2 Current Transfer Function

From the Equation (9.18) the transfer function of the current can be calculated as:

$$\begin{aligned}
\frac{i_1}{H_{\text{s}} \cdot G_{\text{V}}(s)} =& V_{\text{set}} - V_{\text{out}} + G_{\text{C}}(s) \cdot \alpha_1 \cdot \sum_{i=1}^{n} i_i - G_{\text{C}}(s) \cdot i_1 \\
=& V_{\text{set}} - G_{\text{vi}}(s) \cdot \sum_{i=1}^{n} i_i + G_{\text{C}}(s) \cdot \sum_{i=1}^{n} i_i - G_{\text{C}}(s) \cdot i_1 \\
=& \frac{1 + n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}}{n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}} \cdot G_{\text{vi}}(s) \cdot \sum_{i=1}^{n} i_i - G_{\text{vi}}(s) \cdot \sum_{i=1}^{n} i_i \\
&+ G_{\text{C}}(s) \cdot \sum_{i=1}^{n} i_i - G_{\text{C}}(s) \cdot i_1
\end{aligned} \tag{9.20}$$

After further simplifications, the following results for the output current of the DC-DC converter i_1:

$$\begin{aligned}
\frac{i_1}{\sum_{i=1}^{n} i_i} &= \frac{\frac{1 + n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}}{n \cdot G_{\text{vi}}(s) \cdot G_{\text{V}}(s) \cdot H_{\text{s}}} G_{\text{vi}}(s) - G_{\text{vi}}(s) + G_{\text{C}}(s) \cdot \alpha_1}{\frac{1}{G_{\text{V}}(s) \cdot H_{\text{s}}} + G_{\text{C}}(s)} \\
&= \frac{\frac{1}{n \cdot \alpha_1} + G_{\text{V}}(s) \cdot G_{\text{C}}(s) \cdot H_{\text{s}}}{1 + G_{\text{V}}(s) \cdot G_{\text{C}}(s) \cdot H_{\text{s}}} \cdot \alpha_1 \\
&= \frac{\frac{1}{n}}{1 + G_{\text{V}}(s) \cdot G_{\text{C}}(s) \cdot H_{\text{s}}} + \frac{G_{\text{V}}(s) \cdot G_{\text{C}}(s) \cdot H_{\text{s}}}{1 + G_{\text{V}}(s) \cdot G_{\text{C}}(s) \cdot H_{\text{s}}} \cdot \alpha_1
\end{aligned} \tag{9.21}$$

Assuming that the open circuit exhibits approximately I-behavior, the following simplifications follow for low (Equ. (9.22)) and high (Equ. (9.23)) frequencies:

$$\lim_{s \to 0} \frac{i_1}{\sum_{i=1}^{n} i_i} = \frac{G_{\text{V}}(s) G_{\text{C}}(s) H_{\text{s}}}{1 + G_{\text{V}}(s) G_{\text{C}}(s) H_{\text{s}}} \cdot \alpha_1 \tag{9.22}$$

$$\lim_{s \to \infty} \frac{i_1}{\sum_{i=1}^{n} i_i} = \frac{\frac{1}{n}}{1 + G_{\text{V}}(s) G_{\text{C}}(s) H_{\text{s}}} \tag{9.23}$$

In the static case, the current converges towards the α_1-fold of the total current. The voltage control exhibits I-behavior and consequently there is no steady-state control deviation using the load distribution control approach.

9.4.3 Load Behavior of n DC-DC Converters Connected in Parallel

For the consideration of the control behavior of a DC-DC converter in a system consisting of n DC-DC converters connected in parallel, it is relevant which load the corresponding DC-DC converter perceives. In the following, a parallel connection of two DC-DC converters is considered. Thereby it is assumed that the current control is several times faster than the voltage control and thus H_s can be interpreted as a controlled current source.

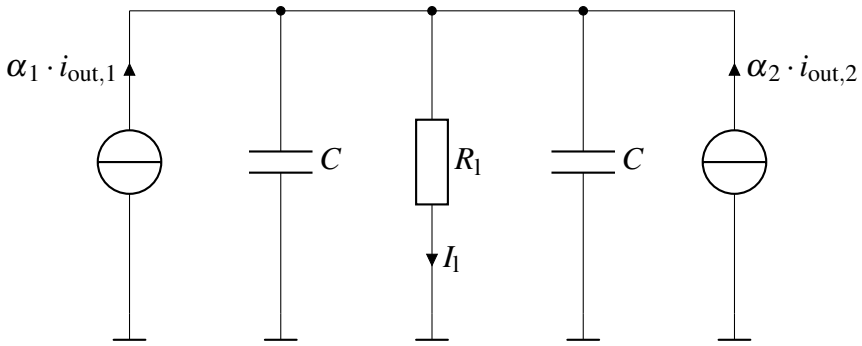


Figure 9.17: Parallel connection of two converters with identical output capacitance C

The total load corresponds to the parallel connection of the three passive components (Fig. 9.17):

$$Z_{out} = \frac{1}{\frac{1}{R_l} + s \cdot 2 \cdot C} = \frac{R_l}{1 + s \cdot 2 \cdot R_l \cdot C} \tag{9.24}$$

The output voltage is given by the total current through the impedance Z_{aout} and is defined as:

$$V_{out} = I_l \cdot Z_{out} \stackrel{!}{=} \alpha_1 \cdot i_l \cdot Z_1 = \alpha_2 \cdot i_l \cdot Z_2 \tag{9.25}$$

The two impedances Z_1 and Z_2 are given depending on α:

$$Z_1 = \frac{Z_{out}}{\alpha_1} \tag{9.26}$$

$$Z_2 = \frac{Z_{out}}{\alpha_2} \tag{9.27}$$

This consideration can be transferred to n DC-DC converters. The total impedance Z_{out} is given by:

$$Z_{out} = \frac{1}{\frac{1}{R_l + s \cdot n \cdot C}} = \frac{R_l}{1 + s \cdot n \cdot R_{out} \cdot C} \tag{9.28}$$

For the equivalent impedances follows:

$$Z_{\mathrm{i}} = \frac{Z_{\mathrm{out}}}{\alpha_i} = \frac{R_{\mathrm{l}}}{\alpha_i} \Big|\Big| \alpha_i \cdot n \cdot C \tag{9.29}$$

It follows that the load consideration of a DC-DC converter in a system of parallel connected DC-DC converters can be reduced to the consideration of only one converter.

9.4.4 Dimensioning of the Load Distribution Control

The current and voltage controller are dimensioned according to the principles of Average Current Mode Control with outer voltage control (Chapter 8). If a high number of DC-DC converters are planned to be used, the gain must be adjusted accordingly. According to Equation (9.21), the path to be controlled corresponds to the load distribution of the open loop of the voltage control for one DC-DC converter. The measurement of the current through a converter is already realized by the structure of the ACMC and is based on a shunt resistor. The total current can be measured in different ways: One variant of the measurement is the addition of the individual currents. In this case, the individual currents must be passed on to the other converters through a communication structure. Digital communication results in discretization and delays of the measurement data. Another variant is an additional total current measurement on the common DC line. Both variants were implemented in order to continue total current measurement and thus load sharing control in case of a failure of the total current sensor. Since the open loop voltage control is already stable and does not require any further control, $G_{\mathrm{C}}(s)$ only needs to compensate for the behavior of the measurement. For this reason, a P-controller is usually sufficient. For the dimensioning of the controller it is assumed that the open loop has an ideal I-behavior. Furthermore, it is assumed that the measurement of the total current is conducted with the frequency f_{m}. The gain of the measurement is supposed to be constant at M. The crossover frequency f_c is intended to be a factor k below f_m due to the sampling of the signal. The gain of G_C is thus given by.

$$G_{\mathrm{C}} = \frac{1}{M \cdot k} \cdot \frac{f_{\mathrm{m}}}{f_{\mathrm{c}}} \tag{9.30}$$

9.5 Summary

In this chapter, two different control strategies for the distribution of the load current in a system consisting of parallel connected DC-DC converters were developed and investigated.
A droop-based and communication-based control approach were proposed, which both offer the possibility to change the distribution factors during active operation.
The droop-based strategy is characterized as a communicationless method based only on local measurements. This allows load sharing without communication between components, without the need for a total current measurement or knowledge about the total number of available DC-DC converters. By using a virtual droop resistor, the current limiting and gain factor is adjustable, e.g., depending on the actual battery state. The droop-based control in general presents a compromise between accurate voltage control or load sharing. A limited accuracy of the load sharing is shown in

this case, since a permanent control deviation and fluctuations within a defined range can occur.
A novel communication-based load sharing control is proposed and developed. This method allows automatic adjustment of the current according to the specified distribution factor. The proposed load distribution control is independent of the voltage control. This is advantageous because even if the load sharing specification is incorrect or in case of errors in the total current measurement, the voltage setpoint is achieved. During the measurements, spurious signals due to the switching edges were noted, which could be possibly reduced by switching to a quasi-resonant converter in future work. Furthermore, it is pointed out that the implementation of zero-current switching or zero-voltage switching could positively influence the efficiency, depending on the topology chosen.
The obtained results show that the given controller specifications were met. Nevertheless, there remains options to further improve the proposed control method. One possibility for further improvement is to use higher order controllers instead of the PI-controllers. Also, taking measurement errors and disturbances into account could provide further insight and increase the robustness of the control strategies.
In summary, the two controller approaches realize battery state dependent load sharing in heterogeneous battery systems while satisfying the requirements for robustness, reliability and availability.

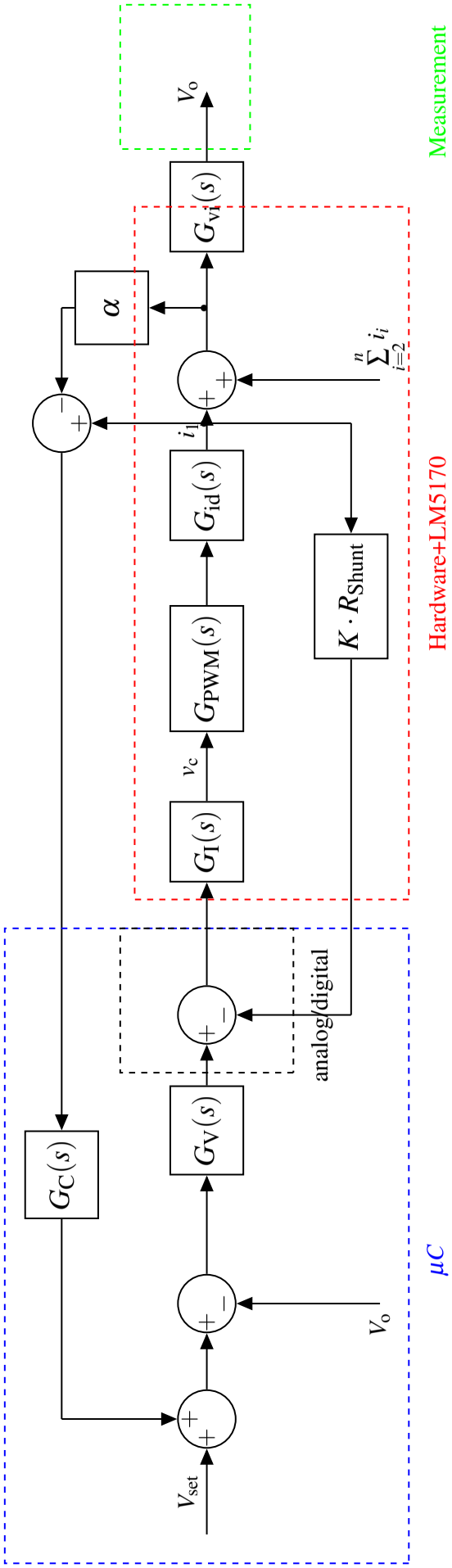


Figure 9.18: Control loop of the Direct Duty Cycle Control (DDCC) for voltage control of the bidirectional DC-DC converter.

10

Battery Fitness for the State Evaluation of Heterogeneous Batteries

The integration of batteries with high energy and power density, as well as of reused second-life batteries, plays a crucial role in the increased use of renewable energy and the electrification of the transportation and heating sectors, taking into account sustainability and efficient use of resources. The different allowable Safe Operating Areas (SOA) of batteries pose a safety risk. To address this complexity, this chapter provides a method to establish battery state dependent current limiting factors δ and load current sharing factors α for safe operation and load current sharing between different batteries connected in parallel. The basis for determining the two values is a system-wide unambiguous battery state assessment of a variety of heterogeneous batteries, taking into account the three battery operating states of charging, discharging and storage. In addition, the proposed method offers the possibility to choose between safe and optimized battery operation. To achieve this, a generic software template is presented that allows flexible and dynamic limit adjustments during operation. The presented method does not focus on setting limits for individual battery parameters, but rather presents an approach that considers different parameters to enable safe and optimized operation in heterogeneous systems.

10.1 Motivation

The integration of batteries with high energy and power density as well as the reasonable use of second life batteries are essential for the electrification of the transport sector and for ensuring grid stability with an increasing share of renewable energies. Nevertheless, safety risks are a major challenge especially in heterogeneous battery systems, where batteries with varying cell chemistries, residual capacity, State of Charge (SoC) and State of Health (SoH) are combined.
Different cell chemistries have varying Safe Operating Areas (SOAs) in terms of temperature, SoC, maximum (dis)charge current and open collector voltage. The combination of batteries based on different cell chemistries in one system offers

the possibility to optimally combine the various battery properties determined by the materials such as high energy or power density, stable operation over a wide temperature range or safe operation in the marginal areas of the SoC. Furthermore, heterogeneous battery systems allow the combination of batteries with different nominal and residual capacities and second life batteries can be effectively integrated.

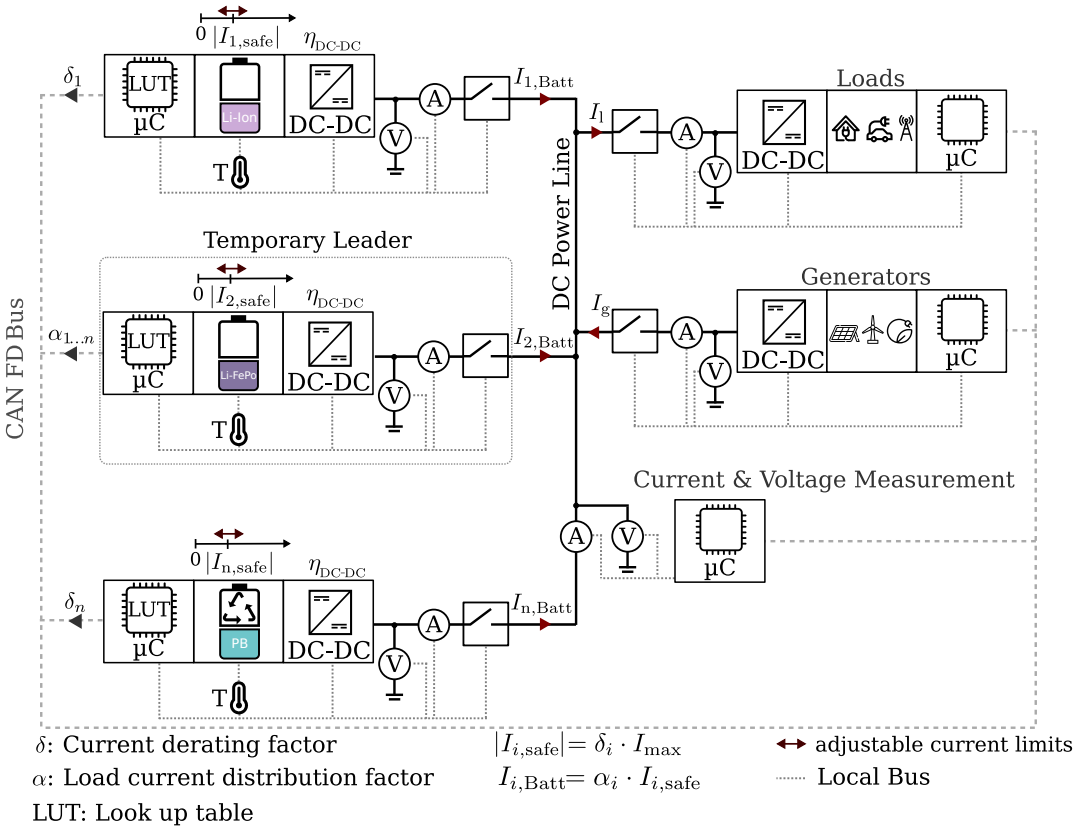


Figure 10.1: For the safe operation of heterogeneous battery systems, it is necessary to limit the battery currents ($I_{i,\max}$) according to the deviating Safe Operating Areas (SOAs). The total current is divided among the batteries connected in parallel according to the distribution factors (α_i). The distribution factors can take into account additional system aspects such as low power dissipation by considering the switching losses of the DC-DC converters.

Due to the differences in the SOAs, the open collector voltage levels and the capacities, safe and reliable operation of heterogeneous battery systems is challenging (Fig. 10.1). The interaction of electrochemical, thermal, and mechanical processes, which vary depending on the chemistry, the used materials (anode, electrode, separator, electrolyte) and the shape of the battery cells, influence the safe operation. To operate such systems safely, it is necessary to monitor the battery states and limit the operating current according to the different SOAs.
Therefore, a method is proposed for battery-state-dependent limiting (δ) of (dis)charge currents and for battery-state-aware load distribution (α) among batteries equipped with DC-DC converters and connected in parallel.
Battery state assessment is thereby affected by various parameters. For example, operation at high temperatures in lithium-ion batteries leads to the growth of the Solid Electrolyte Interphase (SEI) on the graphite electrode, which in turn leads to irreversible capacity loss [474, 475]. Operation at low temperatures, especially in combination with high currents and high SoCs leads to lithium plating on the anode.

In addition to capacity loss and impedance rise, lithium plating also poses a serious safety risk. The resulting lithium dendrites can cause an internal short circuit in the cell. [476–478]
Electrolyte decomposition occurs at the cathode interface, when lithium-ion batteries are operated at high SOCs. This results in heat accumulation and consequent oxygen release from the cathode. The separator may be damaged and, in the worst case, a thermal runaway occurs. [479]
Varying battery chemistries lead to different behaviors. For example, lithium-ion batteries with nickel-based anodes (Li-NMA) exhibit high thermal stability and can be operated safely over a wider temperature range [480]. For lithium titanium oxide (LTO) anodes, operation at high temperatures does not result in SEI growth in contrast to the operation of lithium-ion batteries based on a graphite-based anode. Furthermore, they show efficient charge acceptance at low temperatures [481]. These are just two examples of the significant differences in SOAs that already occur when anode or cathode materials are varied.
The different SOAs in combination with varying capacities pose a major challenge when combining different batteries. Generalizing approaches, such as avoiding battery operation only at extreme temperatures, high SOC, or high (dis)charge current, do not address the varying characteristics of different battery chemistries and limit the available storage capacity without taking advantage of the benefits of heterogeneous battery systems. Furthermore they are not sufficient in order to guarantee safe operation and high system availability. SoH or SoC based approaches are not sufficient for determining the distribution factors as the capacities of the batteries vary (Fig. 10.2).

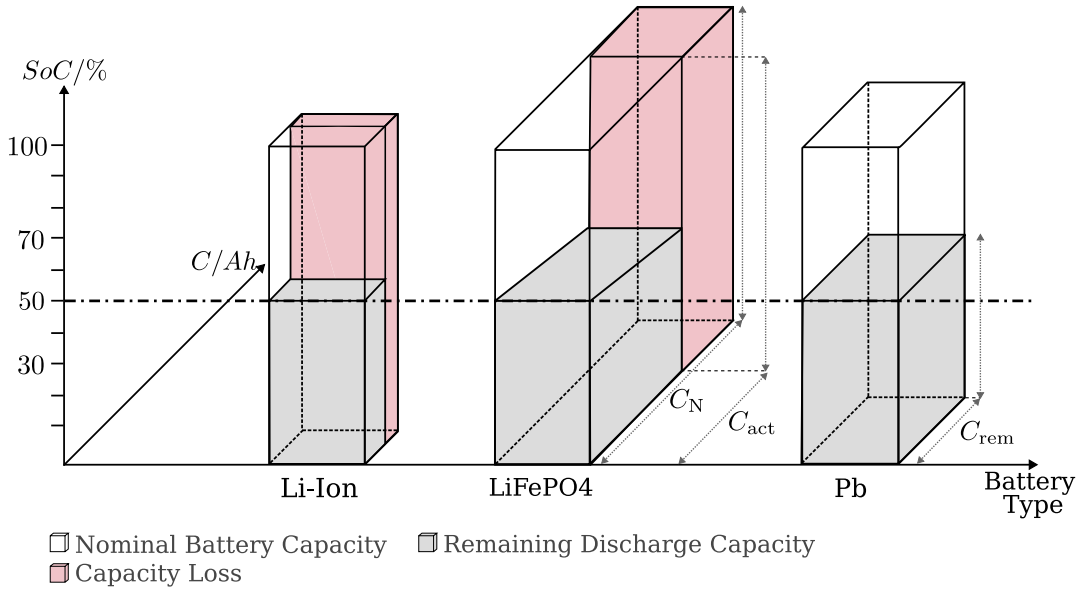


Figure 10.2: The three different batteries all exhibit a SoC of 50 percent. Different nominal (C_N) and actual capacities (C_{act}) show that distribution factors based simply on the SoC are not sufficient. The SoC itself is not indicative of the remaining discharge (C_{rem}) or charge capacity ($C_{act} - C_{rem}$).

Therefore, an approach is required that evaluates the battery state based on different parameters for the corresponding battery chemistry, the design and material selection (anode, cathode, separator, electrolyte, etc.) and limits the (dis)charge current taking into account the SOAs.

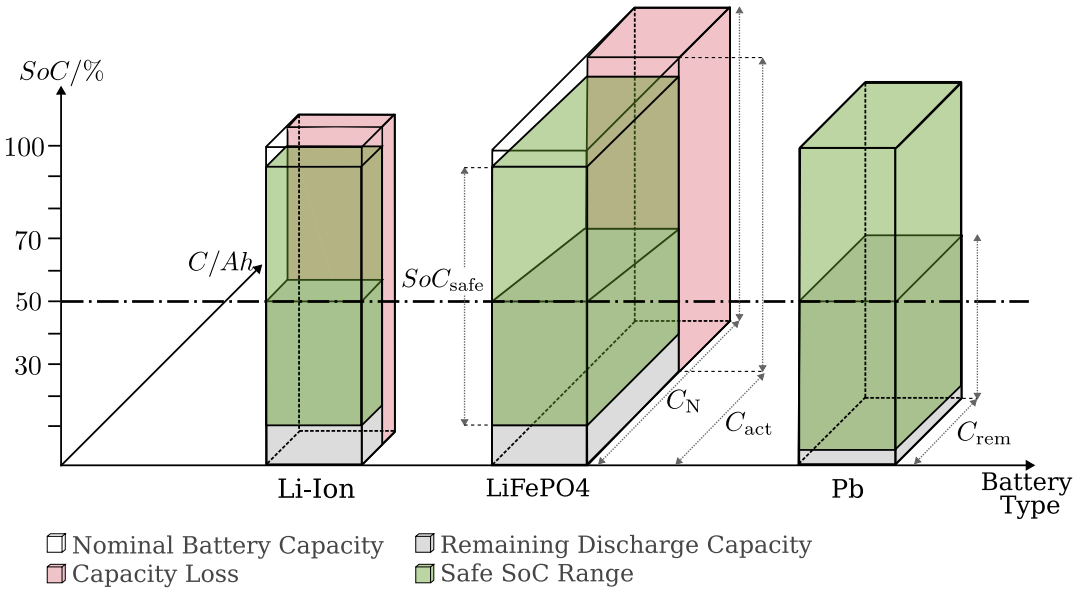


Figure 10.3: Considering additionally the battery cell dependent safe operating areas, in this example the safe SoC ranges, shows that a more sophisticated load distribution factor taking into account several battery characteristics is required.

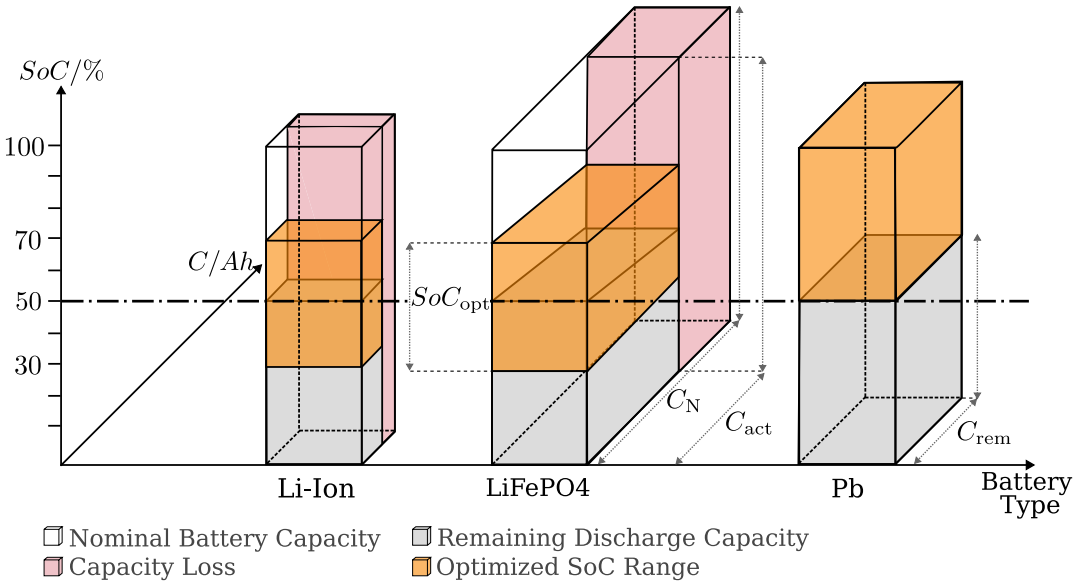


Figure 10.4: For optimized battery operation in terms of degradation reduction, the safe operating area is further restricted to the optimized operating area. The further limitation of the SoC is shown. The optimized operating areas differ depending on the battery chemistry and design.

After determining the allowable battery currents considering the different SOAs, it is necessary to divide the total load current between the batteries. The temporary leader is responsible for specifying the load distribution factors. The determination of the distribution factors also influences the battery degradation, the effective lifetime of the system and the overall efficiency. The determination of the distribution factors and the consideration of additional objectives such as the reduction of power losses caused by the DC-DC converter are presented in the following.
In the proposed current derating strategy, a generic software template is used, whereby the limits are flexibly adjustable and can also be changed during active

operation. Thus, additional optimization possibilities arise by further restricting the SOA. Operation within the Optimized Operating Area (OOA) is only possible if sufficient battery capacity is available in the system (Fig. 10.4). The main research questions in this regard are the following:

- How can a heterogeneous battery system including second life batteries be operated safely?
- How can additional objectives like
  i) prolonging battery life by avoiding degrading operating states,
  ii) optimizing performance by the exploitation of different characteristics,
  iii) achieving a system wide common end of life or
  iv) increasing the system efficiency by considering losses of the power electronics

  be achieved by choosing respective load distribution factors?

The primary objective is the safe, reliable operation of a heterogeneous battery system. The key contributions can be summarized as:

- Method for determining derating factors δ and distribution factors α for a heterogeneous battery system consisting of batteries with differences in cell chemistry, SoC, nominal C_{N} and remaining capacity C_{act}.
- Consideration of multiple parameters and the interaction of these for determining derating factors.
- Operation-state-dependent determination of the derating and distribution factors and subdivision into safe and optimized operation.
- Adaptive adjustment of the limits during operation in response to changing battery parameters such as SoH and internal resistance R_i.
- Approach to account for the losses of the power electronic components in order to increase the system efficiency.

The aim of this work is not to define the limits of individual battery parameters such as SoC or temperature for battery-extending operation. Rather, this approach offers the possibility to consider different parameters and their limits for safe or optimized battery operation of heterogeneous systems.

In the following, existing work on battery derating and distribution approaches is analyzed first. Subsequently, the battery parameters required for the evaluation of the battery condition and the definition of the derating factor are specified and their determination is briefly discussed. The procedure for determining the battery fitness value as a basis for derating the (dis)charge current is shown and the object-oriented software framework is demonstrated. Several options for determining the distribution factors as well as their definition are presented. Finally, an example of a derating factor for limitation of the charge current for a battery is shown.

10.2 Related Work

In the following, existing works on current derating and load distribution control strategies in battery systems are reviewed.

10.2.1 Current Derating Strategies

Current derating describes the operation of batteries at lower currents than the maximum possible with the objectives to ensure safety, to reduce degradation mechanisms and to avoid shutdown.
In [482], an extensive literature review on derating methods with the objective to increase the lifetime of lithium-ion batteries is presented. Existing work is thereby divided into static and dynamic derating methods. Static derating methods are characterized by the fact that their limits are constant and do not change over the operation time. Dynamic derating methods, in contrast, change the limits in accordance with battery aging, e.g., by taking into account capacitance loss and internal resistance increase. Furthermore, both derating methods are further divided into parameter-based and model-based approaches. In parameter-based derating strategies, temperature, SoC, terminal voltage, internal resistance or a combination of temperature and voltage (hybrid) is taken into account to limit the discharge current. Model-based approaches use electrical equivalent circuits, electrochemical, mechanical or thermal models and combinations of these. The paper motivates the use of derating strategies and states that a battery lifetime extension between 41 and 400 percent can be achieved. This statement is based on the investigation of existing derating strategies which have been experimentally validated. Furthermore, a derating framework based on digital twins was presented to identify the dominant aging stress factors. Based on the results, it is recommended to consider temperature, SoC and voltage and the use of dynamic derating methods is recommended. It remains open how the operation limits are determined, especially considering battery degradation.
A dynamic, aging-aware derating strategy for lithium-ion cells is presented in [483]. A calendar and cycle degradation model is used, which determines the degradation rates offline and in advance. The results are then stored as look up tables that provide the maximum allowable battery current estimated using the actual SoC, the temperature, and the cycle degradation rate limit, defined as capacity loss per cycle.
Static parameter-based derating strategies using temperature, SoC, internal resistance, desired charge termination voltage, voltage ranks, and critical error are presented in [484]. Simulations show the effectiveness of the derating strategies. The disadvantage of these strategies is that battery aging is not considered.

10.2.2 Load Distribution Factor Strategies

In a system consisting of several batteries connected in parallel, it is necessary to divide the total load between the batteries in order to avoid excessive stress on individual components.
The paper [485] gives an overview of relevant aging mechanisms, degradation modeling approaches, and methods that aim to increase the lifetime of batteries by taking degradation effects into account. Thereby common lithium-ion cells are considered. The operational methods are further divided into rule-based and optimization-based, whereby the latter determine the optimum of an objective function. Mixed integer linear programming is most commonly used in this context.

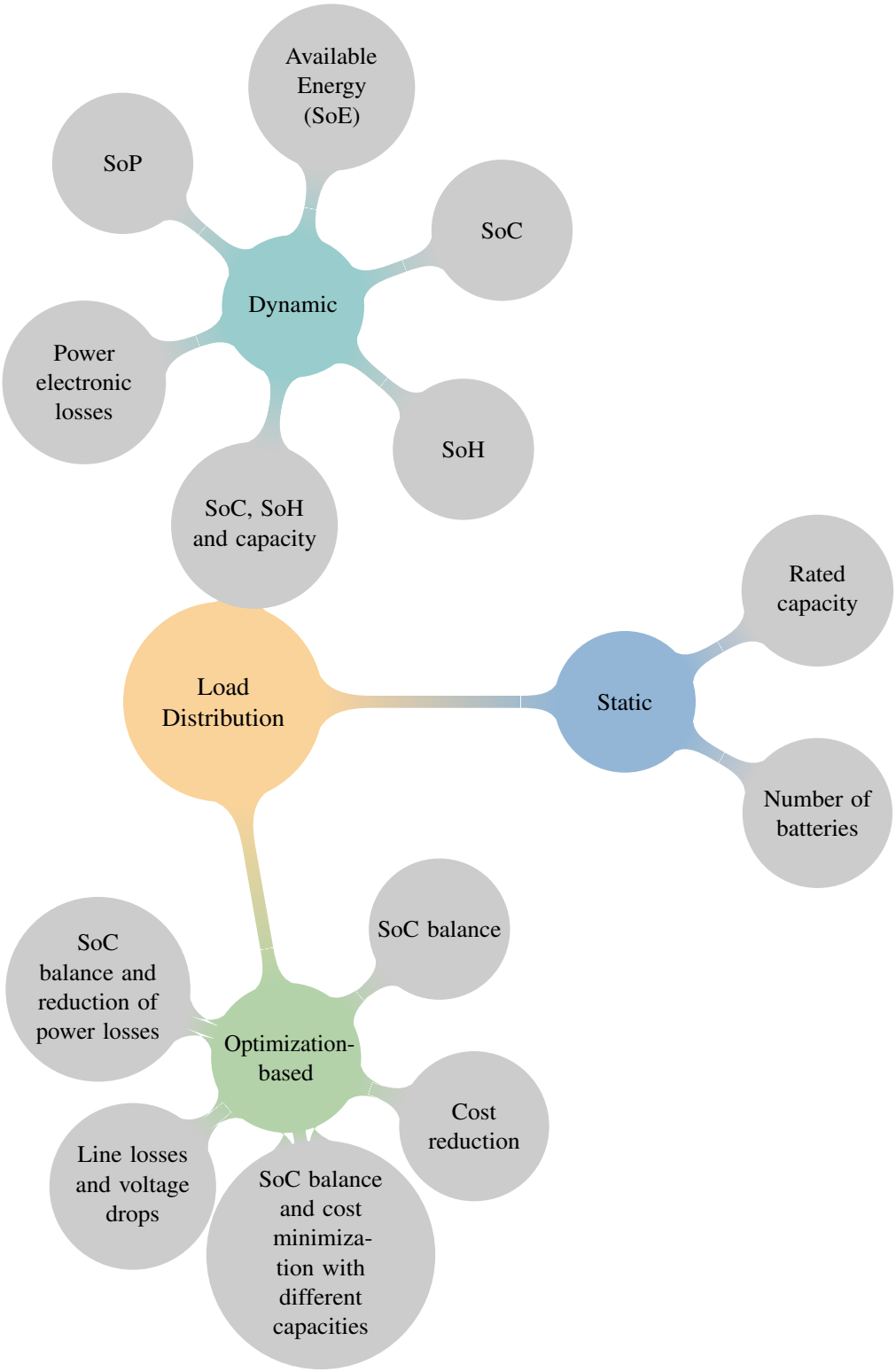


Figure 10.5: Overview of negative electrode materials of lithium-based cells.

Most publications rely on a cost-based approach. Costs associated with battery degradation are used as part of the objective function, as they affect the economic profit from the battery application. The degradation models under investigation generally do not account for the rapid capacity degradation and the change in the aging mechanisms toward the EOL. As a further development, an adjustment of the end-of-charge and end-of-discharge voltage or a further limitation of the C-rate towards the EOL is suggested in [485] for possible lifetime extension for future

developments. Furthermore, it is recommended to consider not only the capacity loss but also the increase of the internal resistance in the battery degradation models.
In [486], existing power flow control strategies are divided into static, dynamic and optimization-based ones. In static power flow control strategies, the distribution factor remains constant and is based on the number of batteries or rated capacity, for example. Dynamic approaches change the distribution factors, for example depending on the State of Health (SoH), State of Power (SoP), Depth of Discharge (DoD), available energy, power electronic losses or a combination of SoC, SoH and capacity. In the optimization-based approaches, the distribution factor is adjusted according to the output of specified objective functions. The objectives are, for example, SoC balance, cost reduction, and combinations of SoC balance with reduction of power losses, minimization of line losses and voltage drops, or minimization of costs for different capacities and SoCs. In addition, in [486] dynamic power flow control strategies based on SoC and SoP for heterogeneous battery systems are investigated. A sequential approach is also proposed.
While a variety of derating current strategies already exist, single parameters are primarily considered for homogeneous battery systems. In the following, a dynamic hybrid derating strategy is presented based on SoC, SoH, nominal capacitance and temperature. The differences in the operating states charging, discharging, short term storage and long term storage are thereby taken into account. A rule-based load current distribution strategy is presented, which is suitable for battery state dependent load distribution in a heterogeneous battery system.

10.3 Requirements

Additional requirements arise for using the derating and load distribution strategy in the Decentralized Battery Management System (DBMS). The factors are determined directly on the microcontrollers of the LCUs. Since the microcontrollers also perform additional computing, control and communication tasks, it is necessary that the derating and load distribution factor determination involves as little computing effort as possible. The calculation depends on parameters that change during operation, which requires that the factors are recalculated repeatedly. The factors are necessary for the control and therefore it is required that their calculation is performed within a reasonable time. Furthermore it is necessary that the limits can be adjusted, for example in accordance to the battery age or the actual degradation state.

10.4 Implementation

The decentralized battery management system consists of several different batteries connected in parallel with variable loads and renewable energy generators. The aim of the control is to regulate the voltage of the DC power line stably to $24\,V$ with variable load (I_l) and generator (I_g) currents. Compensation of deficient or surplus power is done by discharging or charging the batteries. Obtaining the control objective, the following applies to the total battery current:

$$I_\mathrm{Batt,total} = I_\mathrm{g} - I_\mathrm{l} \tag{10.1}$$

Table 10.1: Most common battery hazards, their consequences and parameters to be monitored in order to avoid them.

Battery Hazard	Consequences	Prevention
Thermal Abuse	thermal runaway, explosion	Monitor temperature, C-Rate and I (internal temperature cannot be measured directly)
Electrical Abuse	Explosion	Monitor V, I, T, SoC, C-Rate, I
Chemical Abuse	Dendrite Growth (large current density, low SoC)	C-Rate, I, SoC

The following must be taken into account for safe battery operation:

$$I_{\text{Batt,total}} = \sum_{j=1}^{j} a_j \cdot I_{\text{safe,j}} \tag{10.2}$$

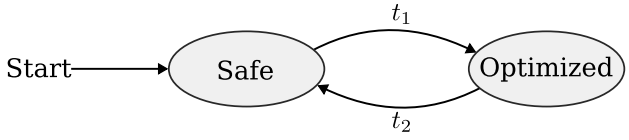
Where n is the total number of batteries $B = B_1, B_2, \ldots B_n$ and A is a subset of B ($A \subseteq B$) and represents the batteries selected for active operation, i.e. $A = B_{i1}, B_{i2}, \ldots B_{ij}$. Here, the number of selected batteries is described by j and $1 \leq j \leq n$ applies.
The safe battery current ($I_{\text{safe,i}}$) is the nominal battery current ($I_{\text{Batt,N}}$) limited by the actual current derating factor (δ_{i}):

$$I_{\text{safe,i}} = \delta_{\text{i}} \cdot I_{\text{Batt,N}} \tag{10.3}$$

In the following, the approach to determine the derating and the distribution factor is described as well as the determination of the subset A.

10.5 Hybrid and Dynamic Battery Current Derating Strategy

The objective of the derating factor is to reduce the battery current in order to prevent catastrophic failures, e.g., thermal runaway, high temperature, high (dis)charge rates or over(dis)charge.



$$t_1 = (E_{\text{d,available}} > E_{\text{d,required}}) \vee (E_{\text{c,available}} > E_{\text{c,required}})$$
$$t_2 = (E_{\text{d,available}} \leq E_{\text{d,required}}) \vee (E_{\text{c,available}} \leq E_{\text{c,required}})$$

Figure 10.6: The safe operating area of the batteries must be maintained at all times for reliable operation and high system availability. If more battery charging or discharging energy is available than required, the operating area of the batteries can be further restricted (OOA) and the degradation due to the operation can be taken into account.

For safe battery operation, it is necessary to limit the maximum possible battery current ($I_{\mathrm{b}i,\mathrm{max}}$) according to the safety-relevant parameters:

$$I_{\mathrm{b}i,\mathrm{safe}} = \delta_{i,\mathrm{safe}} \cdot I_{\mathrm{b}i,\mathrm{max}} \tag{10.4}$$

Further reducing the limits of operating parameters that are connected to battery degradation, e.g. SoC and T gives the optimized battery current:

$$I_{\mathrm{b}i,\mathrm{opt}} = \delta_{i,\mathrm{opt}} \cdot I_{\mathrm{b}i,\mathrm{max}} \tag{10.5}$$

Furthermore, separate current derating factors must be determined for the corresponding operating states charging ($\delta_{i,\mathrm{c}}$) and discharging ($\delta_{i,\mathrm{d}}$) (Fig. 10.7).

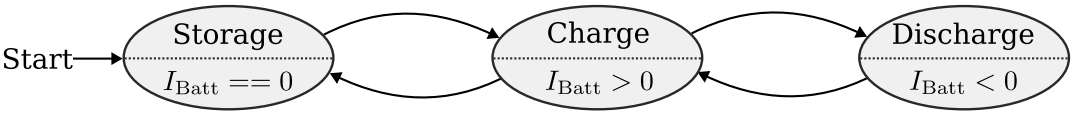


Figure 10.7: State diagramm of the battery operation

The determination of the derating factors is based on look up tables in order to fulfill the analyzed requirements regarding computation effort and duration (Fig. 10.8).

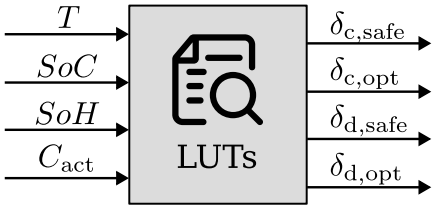


Figure 10.8: The derating factors are determined based on look up tables (LUTs) on the micrcontollers of the LCUs. For a first implementation, temperature, SoC, SoH and the current capacity are used as inputs. Derating factors are defined for charging δ_{c} and discharging δ_{d} and for safe and optimized operation.

In a first implementation of the derating strategy, the temperature T, the SoC, the SoH and the actual capacity C_{act}) are considered.

$$\delta_i = f(T, SoC, SoH, C_{\mathrm{act}}) \tag{10.6}$$

Accurate determination of the SoC and SoH as well as the actual capacity are own research works and are not considered in detail within this thesis. For a first implementation, the Coulomb Counting method is proposed for the determination of the SoC, SoH and C_{act}.
The sequence for determining the safe derating factors for charging and discharging is described below. The flow chart in Figure 10.9 shows the sequence of the required actions. First, the current operating parameters are determined and the derating factor is initially set to 100 percent, which corresponds to the maximum possible value. Afterwards, the current operating parameters are compared with the look up tables to determine the derating factor. Figure 10.10 shows exemplary the process for determining the derating factor according to the actual temperature value. The procedure for the other factors is analogous. The figures 10.11–10.19 show the look up tables for a lithium-ion battery [487]. According to the data sheet, the permissible temperature range differs according to the operating states charge

(Fig. 10.11), discharge (Fig. 10.12), short term storage (Fig. 10.13) and long term storage (Fig. 10.14). The latter two operating states do not affect the current limitation except for recharging processes, but are already stored. Active cooling or heating mechanism of the batteries can be added in future work and it can be activated depending on the operating state and the measured temperature.
For the state of charge, initial values for the derating factor for charging and discharging were defined in order to keep the SoC in the medium range around 50 percent (Figs. 10.15, 10.16). The actual battery current is additional limited depending on the SoH in order to take into account the increased aging state of second life batteries when limiting the current (Fig. 10.18). In heterogeneous battery systems, batteries of different capacities are combined in one system. To account for these capacity differences, the system-wide normalized capacity is introduced (Fig. 10.19).
Thereby the following applies:

$$C_{\mathrm{Norm,i}} = \frac{C_{\mathrm{act,i}}}{\sum_{i=1}^{n} C_{\mathrm{act,n}}} \tag{10.7}$$

The SoH and normalized capacity parameters are not tightly linked to safe battery operation, but are required in heterogeneous battery systems with the integration of second life batteries for battery state-aware current derating.
With the presented sequence and the LUTs, the derating factor can be determined together with the actual operating parameters. For optimized operation, additional LUTs with limited operating range are stored. The selection of the limits for battery degradation aware operation must be determined individually for each battery cell chemistry and design. Effective adjustment of the LUTs is, in any case, already considered in the design.
After determining the derating factors, the battery nodes send CAN FD messages containing the safe and optimized battery currents for charge and discharge (Fig. 10.20). Sending all derating factors is required as the operating state can change quickly and re-sending the derating factors could lead to significant delays and consequently to control deviations or battery operation outside the currently permissible range.
Based on this information, the temporary leader determines the distribution factors.

10.6 Load Current Distribution Strategies

The temporary leader is responsible for defining the load distribution factors. Various approaches for distributing the load current are proposed hereafter together with their advantages and challenges.

10.6.1 Load Distribution According to the Derated Battery Currents

A straight forward approach is to divide the load current according to the derated currents.

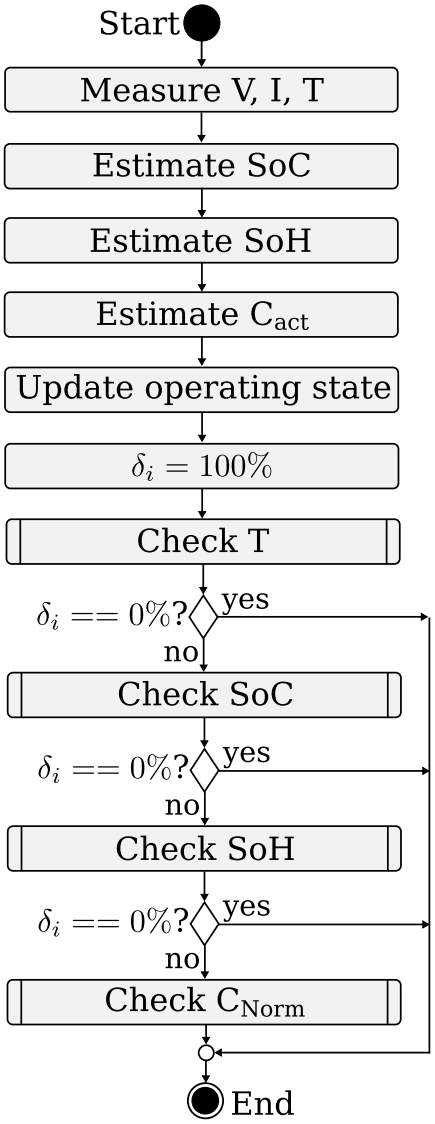


Figure 10.9: Activity diagram for determining the derating factor.

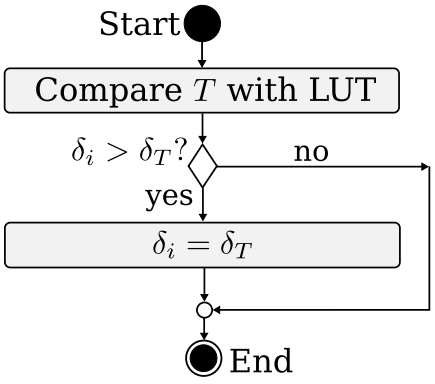


Figure 10.10: For all battery parameters, the current value (in this case the measured temperature) is compared with the look up table (LUT) of the current operating state and the individual derating factor (δ_T) is determined.

$$\alpha_{\mathrm{i}} = \frac{I_{\mathrm{b}i,\mathrm{safe}}}{\sum_{k=1}^{n} I_{\mathrm{b}k,\mathrm{safe}}} \tag{10.8}$$

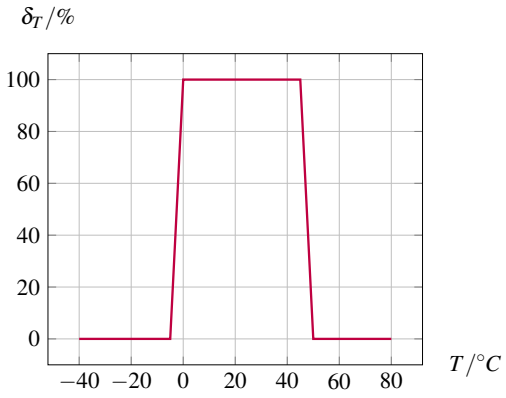


Figure 10.11: Safe operating area of the temperature for the operating state charging for a lithium-ion battery [487].

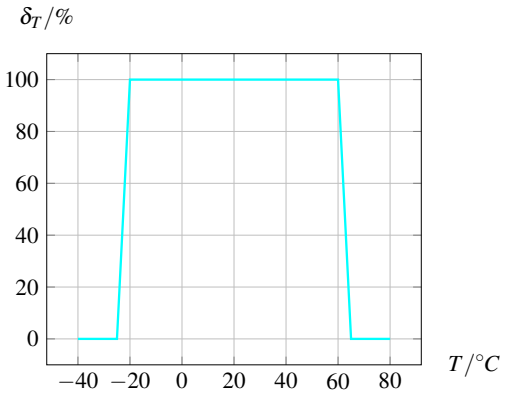


Figure 10.12: Safe operating area of the temperature for the operating state discharging for a lithium-ion battery [487].

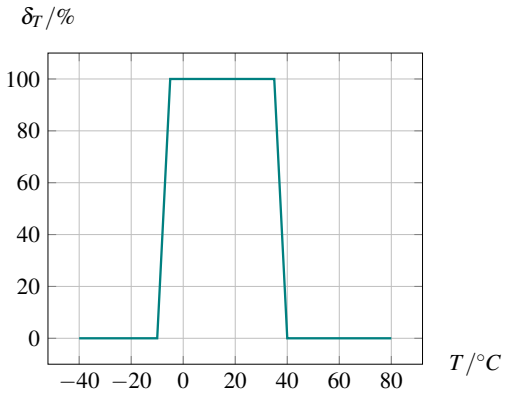


Figure 10.13: Safe operating area of the temperature for the operating state short term storage for a lithium-ion battery [487].

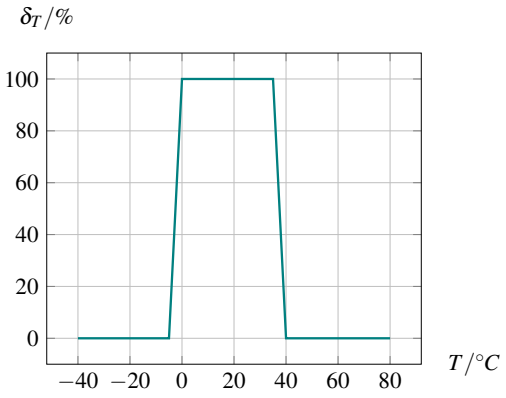


Figure 10.14: Safe operating area of the temperature for the operating state long term storage for a lithium-ion battery [487].

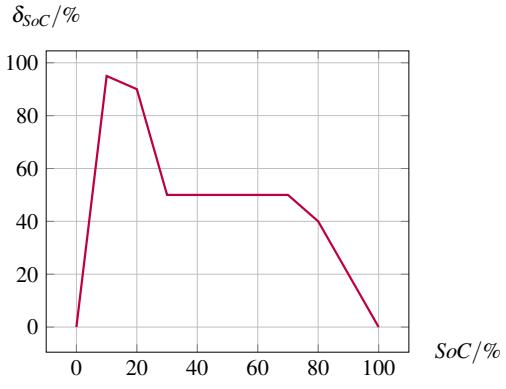


Figure 10.15: Safe operating area of the SoC for the operating state charging for a lithium-ion battery [487].

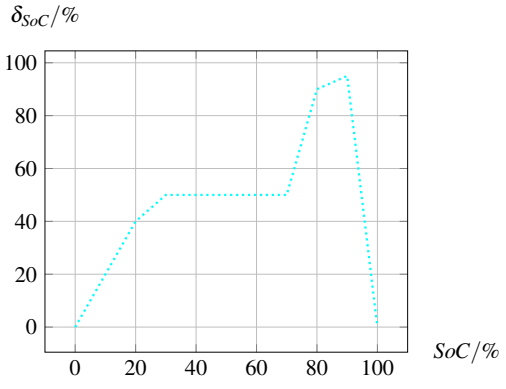


Figure 10.16: Safe operating area of the SoC for the various operating state discharging for a lithium-ion battery [487].

As a result, each of the currently usable batteries is involved in the control. Depending on the number of batteries, this means that only small battery currents flow. In terms of battery degradation, this is advantageous. Considering the load current dependent

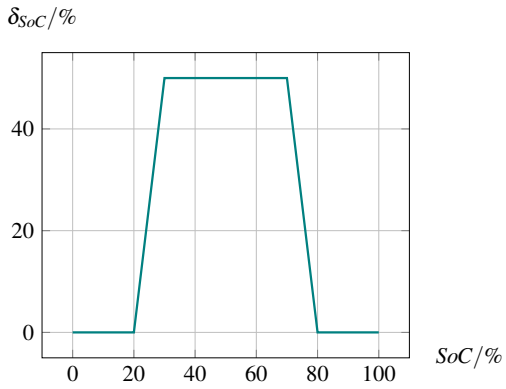


Figure 10.17: Safe operating area of the SoC for the various operating state storage for a lithium-ion battery [487].

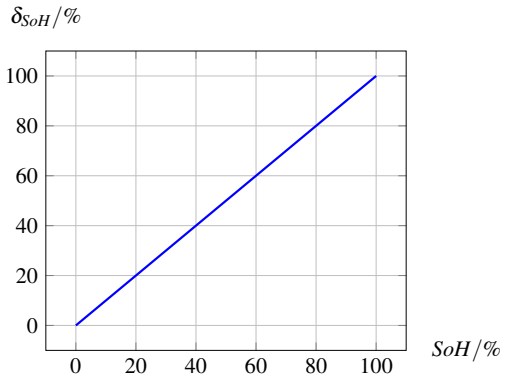


Figure 10.18: For battery state aware current derating in a battery system with new and second life batteries, consideration of the SoH is required.

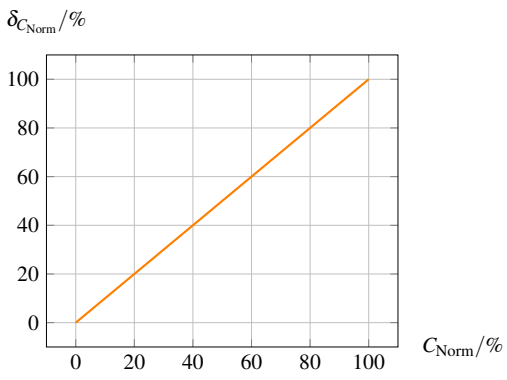


Figure 10.19: In order to take into account the different capacities of the batteries, the normalized capacity in percent is introduced.

Data ID	Node ID	$I_{\mathrm{c,safe}}$	$I_{\mathrm{c,opt}}$	$I_{\mathrm{d,safe}}$	$I_{\mathrm{d,opt}}$

Figure 10.20: The CAN message contains the current derating factors for safe and optimized operation for the operating states charging and discharging.

efficiency of the DC-DC converters and thus the overall system efficiency, various DC-DC converters operating with low currents is disadvantageous.

10.6.2 Load Distribution Considering Power Electronic Losses

A further possible approach is to store the efficiency over the output current curve of the DC-DC converters used (Figs. 10.21, 10.22) as LUTs on the microcontroller of the LCUs. The battery nodes determine the current efficiency in dependence of the derated currents and send this as well. The temporary leader sorts the received messages according to the actual efficiency and selects a subset of the battery nodes that have the highest efficiency. The distribution factor is subsequently determined according the efficiency of the DC-DC converter:

$$\alpha_i = \frac{\eta_i}{\sum_{k=1}^{j} \eta_k} \tag{10.9}$$

In this case, it is important that the battery nodes send a notification to the temporary leader if the maximum allowable (dis)charge current value is reached. In response to this notification, another battery node is activated and the load distribution factors are reassigned. For improved system efficiency, it is also conceivable to take the internal resistance into account in addition to the efficiency of the DC-DC converters when dividing the currents.

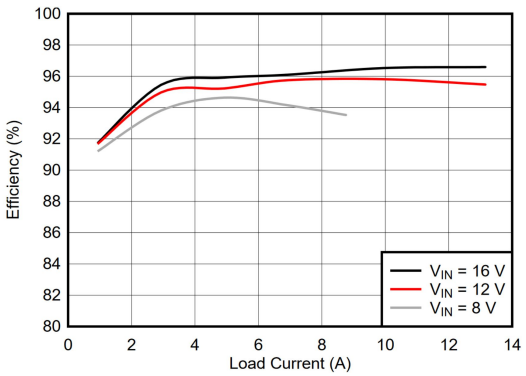


Figure 10.21: The efficiency of the DC-DC converter operating in boost mode with the higher $V_{\text{out}} = 50.5V$ at the high voltage side [388].

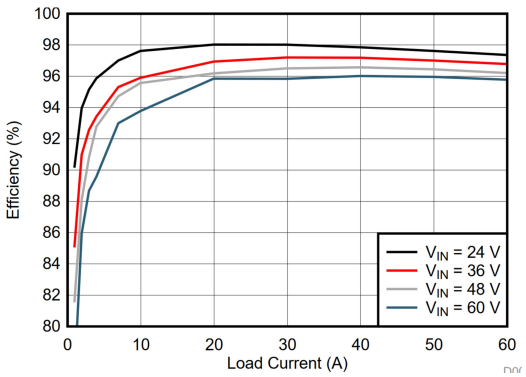


Figure 10.22: The efficiency of the DC-DC converter operating in buck mode with the lower $V_{\text{out}} = 14.5V$ at the low voltage side [388].

10.6.3 Reaching a Common End of Life

In a system consisting of batteries with differences in SoH, reaching a common end of life is essential for the longest possible system operation. One way to take into account the different aging states is the SoH aware distribution of the load currents. For this, the battery nodes send the SoH in addition to the derated currents. The temporary leader sorts the messages by SoH and selects a subset to be actively used. The load current is divided according to the SoH, and newer batteries are used more compared to aged ones.

$$\alpha_i = \frac{SoH_i}{\sum_{k=1}^{j} SoH_k} \tag{10.10}$$

10.7 Summary

In this chapter, a current derating and a load current distribution method for heterogeneous battery systems have been proposed. The hybrid, dynamic current derating strategy considers different battery parameters. The comparison of the current operating parameters with LUTs stored on the microcontrollers enables an efficient determination of the derating factors. The limits for the evaluation of the individual battery parameters can be effectively adjusted during operation. Furthermore, derating factors are proposed for safe and optimized operation, the latter further limiting the operating range to minimize battery degradation. The presented current derating strategy enables safe battery operation in a heterogeneous battery system.

Concepts for load current sharing considering battery degradation, power electronics losses or SoH of the batteries were presented. The hardware and control strategies presented in the chapters 6, 7, 8, 9 enable load current sharing and current limiting that can be adjusted during operation.
Further research is required in this case to answer the stated research questions. The limits for safe and optimized battery operation still need to be defined. One possible way to efficiently do this is to simulate the batteries using PyBamm and cycle them with different limits.
Furthermore, it is necessary to implement battery models on the microcontrollers for improved state estimation. There exist already a number of papers dealing with this topic [488–491]. Another possibility is to port the PyBamm models to the microcontrollers. The advantage of this approach, is that the models are electrochemical and have a higher accuracy, especially with regard to aging and degradation.
The aim is to take into account all the presented objectives in the load current distribution, i.e. battery-optimized operation with the highest possible system efficiency and the achievement of a common end of life. For this, multi objective optimization strategies are required.

11

Switching and Averaging Models of the Bidirectional, Half-Bridge Based DC-DC Converter with Load Distribution

Bidirectional DC-DC converters are vital for the integration of batteries, for the power conversion during (dis)charge and the battery management. Modeling of these is helpful, especially for the design of larger, more complex systems consisting of multiple DC-DC converters in parallel. Due to the high switching frequencies, the simulation of DC-DC converters is associated with increased computational time and effort. In this section, three models of different complexity and accuracy are proposed for a bidirectional DC-DC converter consisting of two phase-shifted half-bridges. Two switching models, which differ mainly in the way the MOSFETs are driven, account for the individual switching operations and exhibit high accuracy. An averaging model replaces the switching elements with current and voltage sources providing the mean values. The dynamic behavior of the models is analyzed using the step responses of the load current. For validation, these are compared with the theoretical transfer function. The three models are analyzed comparatively in terms of computational time and effort. The calculation time of the averaging model has been reduced by two thirds compared to the strictly complementary switching model and by 96% relative to the model with diode emulation mode. Recommendations for the use of the models are given and a possible use case is shown. Two parallel connected DC-DC converters with load current sharing between them are simulated using the averaging model.

11.1 Motivation

Heterogeneous battery systems combine batteries with differences in cell chemistry, nominal capacity, state of health, state of charge, safe operating area and terminal

voltage. They offer advantages such as increased energy density, improved efficiency, enhanced safety and flexibility compared to homogeneous systems. Furthermore, they provide second life batteries a further application with lower requirements regarding dynamics, remaining useful capacity and internal resistance. Due to the heterogeneity, it is challenging to ensure reliability, robustness and safety of the system. Specific requirements arise for the control of the DC-DC converters: Adjustable current limits are required and the different input voltages have to be converted to a common DC output voltage and vice versa. The (dis)charge current has to be limited according to the battery state and the safe operating area in order to realize reliable simultaneous operation of varying batteries. The total current is divided among the batteries depending on their state, which reduces the burden and enables additional possibilities such as state of charge balancing in active operation without recharging or state of health balancing with the goal of achieving a common end of life.

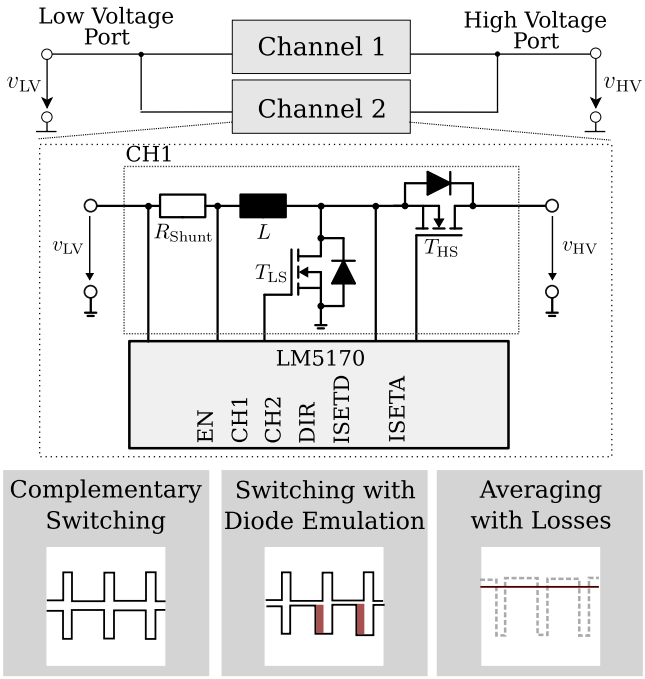


Figure 11.1: The bidirectional, half-bridge-based DC-DC converter is emulated by three different models of varying accuracy.

The model of the bidirectional DC-DC converter is valuable for the analysis of its behavior and performance. It is the basis for the development of suitable control strategies and enables initial tests of these in parallel operation of several DC-DC converters. The robustness, safety and reliability of the system can be investigated. Robustness is defined as the stability in the presence of disturbances, safety as the behavior in the event of a fault and reliability as the system availability in the event of breakdown of individual components.
In order to consider varying time scales, different abstraction levels are required. Three models of a bidirectional, multiphase DC-DC converter based on two half-bridges are presented (Fig. 11.1). The behavior of the DC-DC converter is thereby primarily determined by the power semiconductors and the passive components. Two switching models of the DC-DC converter are proposed for detailed analysis of the switching behavior and are suitable for relatively short simulation duration. For the

system simulation, an averaging model is proposed which neglects the individual switching processes.
The different models are described and compared with the calculated transfer function of the bidirectional DC-DC converter. They are compared in terms of computational effort and time. Two averaging models are subsequently connected in parallel as an exemplary use case and the load current sharing between two DC-DC converters is simulated.

11.1.1 Related Work

Existing works on the simulation of DC/DC converters also propose averaging models, while concentrating on other aspects, i. e. parameterization of the electrical components, reduction of the simulation time, temperature dependency and losses or testing of control strategies.
The paper [492] focuses on the system identification of inverters and proposes a novel model of a bidirectional 48/12 V DC/DC converter which is valid for different frequency ranges. Three models are presented: a switched, an averaging and a steady-state one. While the switched one accurately models each switching operation, the intermediate one neglects the switching frequency and the steady-state one replicates the behavior of the converter only after the transient operations have decayed. For the averaging model the state space modeling approach is used. The focus in this case is on the identification and parameterization of the electrical components.
In article [493], a continuous-time linearized model of a non-isolated bidirectional half-bridge DC-DC converter corresponding to the state-space averaging method is proposed. The key contribution is the reduction of the time complexity, which can be lowered by up to 1/4450 compared to the time required by the switching model.
In the paper [494] an electrical-thermal model of a DC/DC boost converter is developed, validated by comparison with real measurements. It focuses on the analysis of the temperature dependence of the efficiency and on the losses of the converter. Another goal is the identification of the most important factors influencing the losses. Compared to existing models, it allows the determination of the converter temperature and higher accuracy at lower computing power.
In contribution [495], a simplified averaging model of a synchronous half-bridge converter is presented, which shows the losses and the dynamic behavior without the need to simulate every switching process of the power semiconductors. For validation, the proposed model is compared with a SPICE simulation and shows a deviation of only 1.5%.
An averaging model of a half-bridge converter, more precisely a two-stage DC/AC voltage source converter, is proposed in [496]. The key topic is the test of different control strategies and their effects on the model behavior. The paper demonstrates that averaging models can lead to control parameters which cannot be successfully transferred to real power electronic components.

11.1.2 Main contributions

Two switching models with different accuracy levels and varying control of the MOSFETs and an averaging model of a half-bridge based, multiphase DC-DC converter are proposed. A novel model with diode emulation is developed. The averaging model is based on the circuit averaging technique and uses equivalent circuits. Another novelty is the possibility of efficient switching between the

three proposed models. Thus, the diverse behavior of the models according to the simulation objective, e.g. testing of control strategies, can be taken into account. The simulation especially focuses on testing the control strategies and load sharing between DC-DC converters connected in parallel.

11.2 Bidirectional DC-DC Converter

A bidirectional, multiphase DC-DC converter is used for the implementation of the power flow in (dis)charge direction. Depending on the direction of the current flow, it operates in boost or buck mode. The utilized DC-DC converter consists of two half-bridges (Fig. 11.2) connected in parallel, between which the current is symmetrically divided. This decreases conduction losses, which in turn has a positive effect on the thermal behavior of the components. Additionally, it allows a larger power range with significantly smaller devices. The two signals for driving the half-bridges are phase-shifted by 180°. This considerably lowers the current ripple that has to be smoothed by the output capacitance [497, 498]. The LM5170 module is used for current control, which implements the gate drivers, operational amplifiers for current control, current measurement, and a sawtooth generator for average current mode control (Fig. 11.1). The frequency response of the current controller can be determined by the external circuitry. The magnitude of the setpoint current value is specified for digital setting via a pulse width modulated signal to the pin ISETD or for analog adjustment via a reference voltage at the pin ISETA. The direction of the current flow is defined by a voltage reference at the direction pin DIR. At voltages above 2 V at the DIR pin, the converter operates in buck mode and the current flows from the High Voltage (HV) port to the Low Voltage (LV) side. At voltages below 1 V, the converter operates in boost mode and the current flows in the opposite direction.

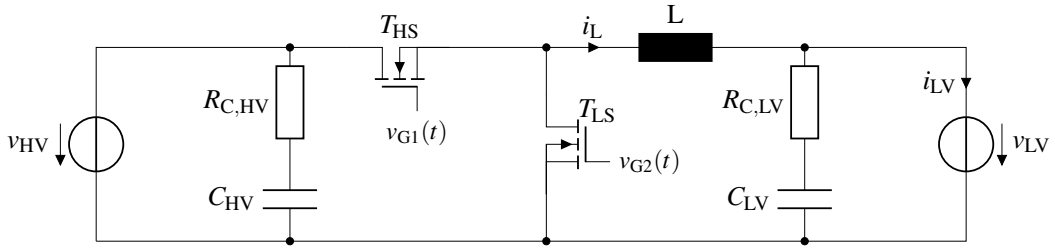


Figure 11.2: One of the two half-bridges of the multiphase DC-DC converter under investigation. Table 11.1 lists the properties of the components.

Table 11.1: Component dimensioning of the two half bridges [499]

L	R	C_{HV}	C_{LV}
4.7 µH	1 mΩ	100 µF	470 µF

According to the two function modes buck and boost, one of the two MOSFETs works as the main and one as the sync MOSFET. In boost mode, the main one is the High Side (HS) MOSFET T_{HS}, whereas in buck mode the main one is the Low Side (LS) MOSFET T_{LS}. The other one, in each case, is the sync MOSFET.

They are switched complementary: When the main MOSFET is on, the sync one is off and vice versa. While the main MOSFET is driven, the current across the inductor increases. The instantaneous value of the inductor current is measured by a shunt resistor. Each channel has a real-time zero-crossing detector to monitor the instantaneous shunt voltage V_{CS}. When a zero crossing of V_{CS} is detected, the gate drive of the sync MOSFET is turned off. In this way, negative currents are prevented and the efficiency is improved at low load. Figure 11.3 shows the main waveforms of the described switching behavior as a function of the inductor current. The red dashed curve shows the diode emulated mode.

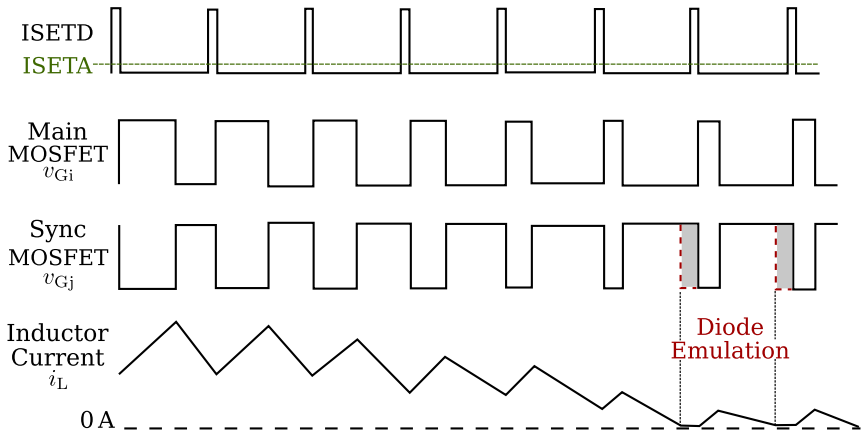


Figure 11.3: Switching signals of the MOSFET in diode emulation mode: If the current through the inductor reaches the value zero, the sync MOSFET is switched off and negative currents are avoided. [499]

$$G_{\text{theoret.}} = \frac{1.0715\text{e}15 + 1.141\text{e}11 \cdot s + 5.584\text{e}5 \cdot s^2}{2.697\text{e}13 + 7.061\text{e}4 \cdot s + s^2} \tag{11.1}$$

The models given in the following are compared with the theoretically determined s-transfer function (Eq. (11.1)) according to the data sheet [500]. This is a generalized, approximated transfer function which neglects the high frequency behavior. For a first validation, this transfer function is sufficient. For future comparisons, the defined transfer functions for the different operating modes from a previous work [501, 502] will be used.

11.3 Strictly Complementary Switching Model

The strictly complementary model reproduces the switching behavior of the MOSFET without diode emulation. It allows a detailed analysis of the operating principle of the circuit, taking into account the individual switching steps. Figure 11.4 shows an overview of the hierarchically structured classes. The `ControlledBuckBoost` model forms the top level and unites all submodels to simulate the current-controlled, bidirectional DC-DC converter with strictly complementary switching of the MOSFETs. Furthermore, the overall model can be subdivided into the physical, electrical simulation of the circuit (`TwoCHBuckBoost`) and its control (`TwoCHController`).

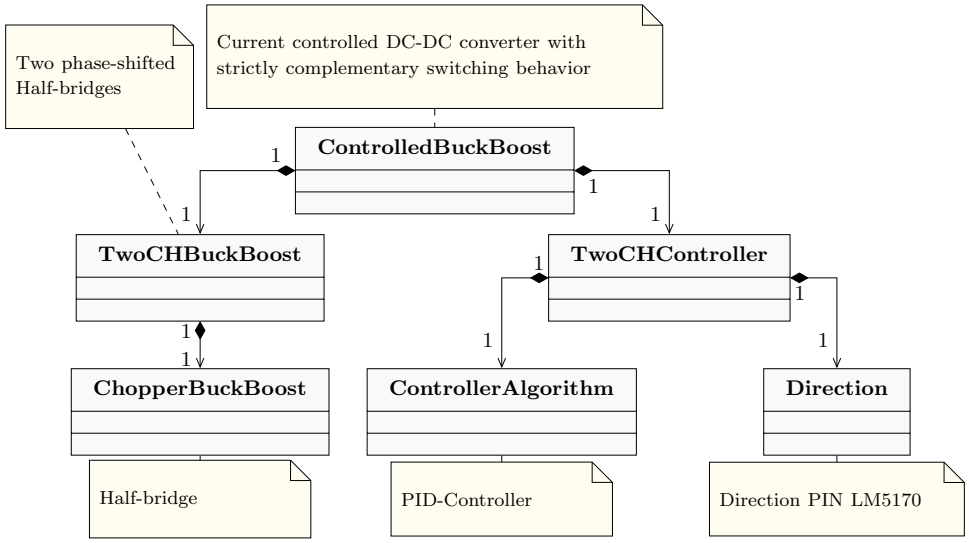


Figure 11.4: UML class diagram and overview of the composition of the various subclasses of the strictly complementary switching model `ControlledBuckBoost`.

11.3.1 Electrical Simulation

There are used two models `ChopperBuckBoost` and `TwoCHBuckBoost` to represent the behavior of the circuit of the bidirectional DC-DC converter. The innermost level is the `ChopperBuckBoost` model for the simulation of one half-bridge (Fig. 11.5). The HS and LS MOSFET are substituted by a combination of a transistor and a diode to simulate the switching behavior.

`ChopperBuckBoost`: Description of the Half-Bridge Model

The model has nine interfaces: The electrical connections for the power flow are realized by the four interfaces `dc_p1, dc_p2, dc_n1` and `dc_n2`. With the `heatPort` the thermal behavior can be observed and first conclusions about losses can be drawn. The three logic ports are used to control the transistors. With `fire_p` and `fire_n` the transistors are switched. The interfaces are logically and connected with the parameter `enable`, so that the DC-DC converter can be switched on and off. The blocks `logicDelayLV` and `logicDelayHV` are custom developed. The block is used to delay a signal by a selectable time by setting the parameter `delayTime`. When an event occurs at the input port `u`, the variable `tSwitch` is set to the actual time. The switching edge is transmitted to the output `y` as soon as the actual time is greater than `tSwitch + delayTime`. The parameter `enable` allows (de)activation of the half bridge. External control of the model is possible with the parameter `extenable`. It overwrites the local settings for `enable`. The current through the inductor, dimensioned according to Table 11.1, is measured by the current sensor `currentSensor`. Using the `zeroOrderHold` block, the signal is sampled with half of the switching frequency. Thus only the average value is obtained. The measured current value is passed on to the real interface `ILV`.
Between the inductor and the electrical interface `dc_p1` there is a resistor. It combines the shunt resistance and the ohmic resistance of the inductor. The thermal connection of the resistor is connected together with the other ones to the `heatPort`. The capacitor `CHV` connecting the HV side to ground is used for voltage smoothing.

`TwoCHBuckBoost`: Electrical Model of the bidirectional DC-DC Converter

The model `TwoCHBuckBoost` on the next higher hierarchy level simulates the bidirectional DC-DC converter and combines two half bridges, i.e. two instances of the model class `ChopperBuckBoost`, which replicate the two channels and are labeled as CH1 and CH2 (Fig. 11.6).
The electrical connection is analogous to the one of the half-bridge and consists of four interfaces `dc_p1, dc_p2, dc_n1` and `dc_n2`. At Channel 2 (`CH2`) only the pin `dc_n1` is connected to the other n-pins. A connection of `dc_n2` would form a loop of the ground which in turn cannot be calculated by the simulator and would lead to an abort of the simulation. On the LV side there is used a capacitor `CLV` for voltage smoothing. The interfaces `ILV` of the two channels which contain the averaged current measurement values of the inductance current are passed to `ILVCH1` and `ILVCH2`.
The two half bridges are controlled by phase-shifted PWM signals: The duty cycle of the Channel 1 is defined by the interface `dutyCycleCH1`. The real value is limited between the values 0 and 1 and the signal is transferred to the block `pwmCH1`. This block compares a voltage level with a sawtooth signal or a triangle signal and generates a complementary PWM signal from it according to Table 11.2. The same model blocks are used for Channel 2. These are identically constructed, with the only difference that the switching signal is shifted by half a period.

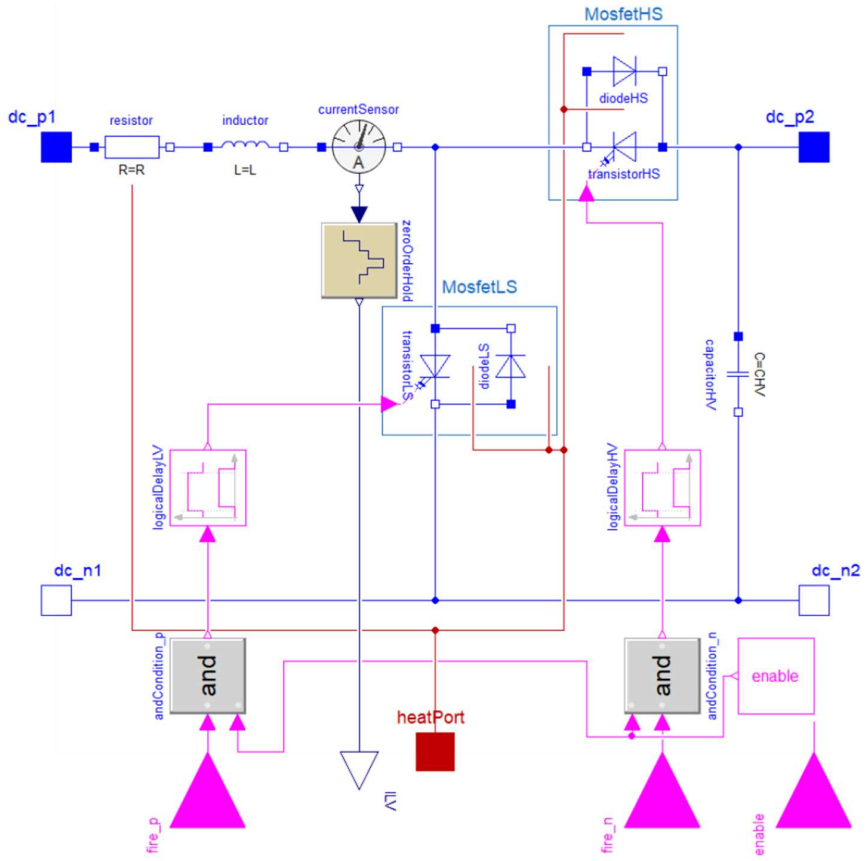


Figure 11.5: The `ChopperBuckBoost` model forms the switching level of the physical model and represents one of the two half-bridges.

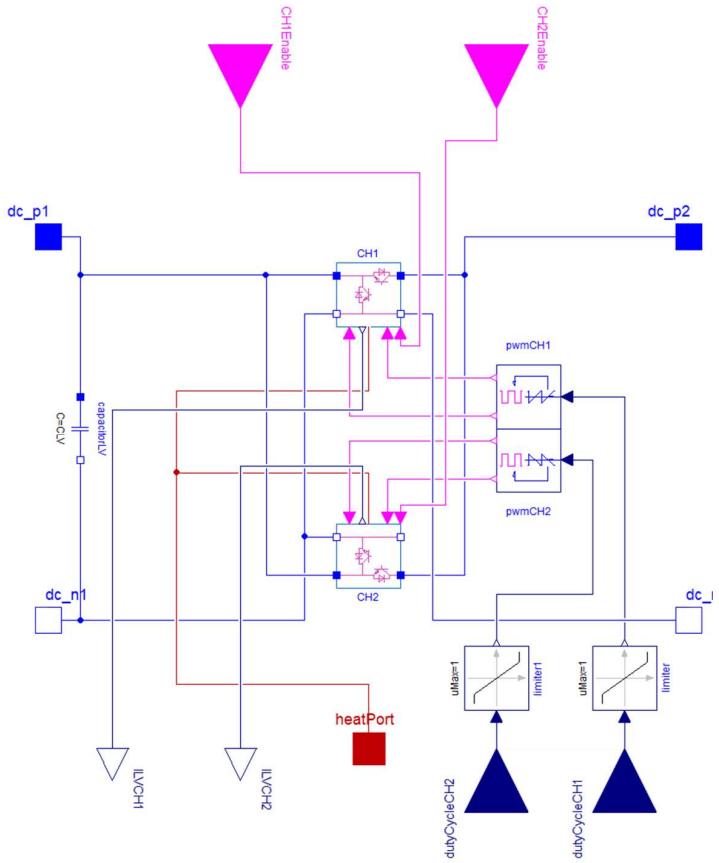


Figure 11.6: Overview of the model for the bidirectional DC-DC converter together with the interfaces.

11.3.2 Simulation of the Control

The control of the bidirectional DC-DC converter is simulated by the model `TwoCHController` (Fig. 11.7). The model consists of the controller implemented by the model `controllerAlgorithm` and the specification of the operating mode (buck or boost) simulated by the model `Direction`.
In this case a PID controller with a constant gain setting of 40 and an output limiter is used (Fig. 11.8). The parameter `DirectedISETA` is controlled considering the feedback of the actual current measurements provided via `measuredCurrentCHx`, $x \in 1 \ldots n$. If the parameter `Enable` is false, the voltage output VLV/VHV is set to a fixed value. The fixed value is only required using the averaging model, but does not interfere with the switching model as the MOSFETs only switch if `Enable` equals true. The direction pin of the LM5170 which determines if the DC-DC converter operates in buck or boost mode is simulated by the model `Direction`. The model checks if `Direction` is either less than the value 1 or greater than 2 and adjusts the ISETA signal accordingly. If the value of `Direction` is less than 1, ISETA is not changed.

Table 11.2: Relation between duty cycle and the control signals of the transistors

Duty Cycle	Control `fire_n`	Control `fire_p`
0	100 %	0 %
0.5	50 %	50 %
1	0 %	100 %

If `Direction` is greater than 2, ISETA is multiplied by -1 in order to change its sign. The corrected value is set in the output parameter `DirectedISETA` which is further processed in the controller. If one of the two valid conditions (`Direction` <1 or >2) is fulfilled the parameter `Enable` is set to the value true.

11.3.3 Validation of the Strictly Complementary Switching Model

The model `ControlledBuckBoost` simulates the behavior of the current-controlled DC-DC converter with strictly complementary switching behavior (Fig. 11.9). The aim of this model is to achieve a high degree of accuracy in simulating the functionality, taking into account the individual switching processes of the MOSFETs. The channels of the bidirectional DC-DC converter can be activated individually. For a correct setpoint current control with two active channels, the required setpoint current is halved (bottom part of Fig. 11.9).
Figure 11.10 shows the test setup for the validation of the models. For validation, the DC-DC converter model is connected via a 0.01 Ω resistor to an ideal voltage source of 12 V at the LV side and via a 0.02 Ω resistor to an ideal voltage source of 24 V at the HV side.
Initially, a voltage of 2 V is supplied to the ISETA pin. Between 0.01 s and 0.02 s the DC-DC converter operates in boost mode and between 0.03 s and 0.04 s in buck mode. The curve of the current over the inductor and the averaging of it over one period (mean PWM) are compared with the theoretical transfer function (Eq. (11.1)) (Fig. 11.11). Only small deviations between the modeled and the theoretical transfer function occur. Therefore, the first jump is analyzed in more detail (Fig. 11.12). The theoretical transfer function exhibits an overshoot, but it is below the targeted 80 A and corresponds to a PT2-behavior. The transfer function of the model also has an overshoot and reaches the 80 A faster than the theoretical one. The averaged transfer function over two periods is similar to the original data. The deviations of the model are within an acceptable range and the model has been successfully validated.

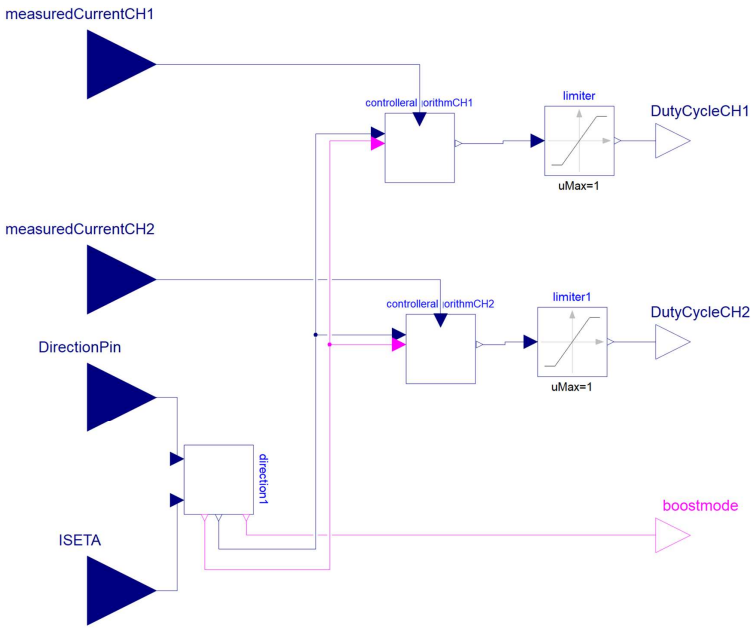


Figure 11.7: Overview of the model `TwoCHController` for modeling the entire control of the DC-DC converter.

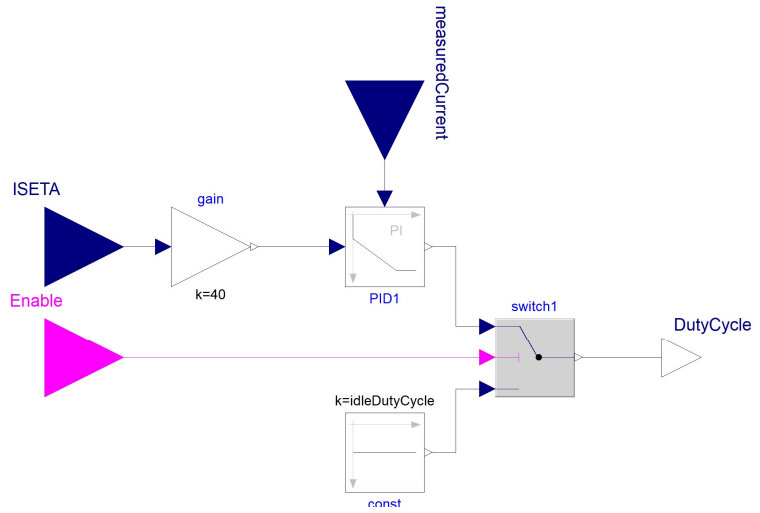


Figure 11.8: The model `controllerAlgorithm` simulates the PID-controller.

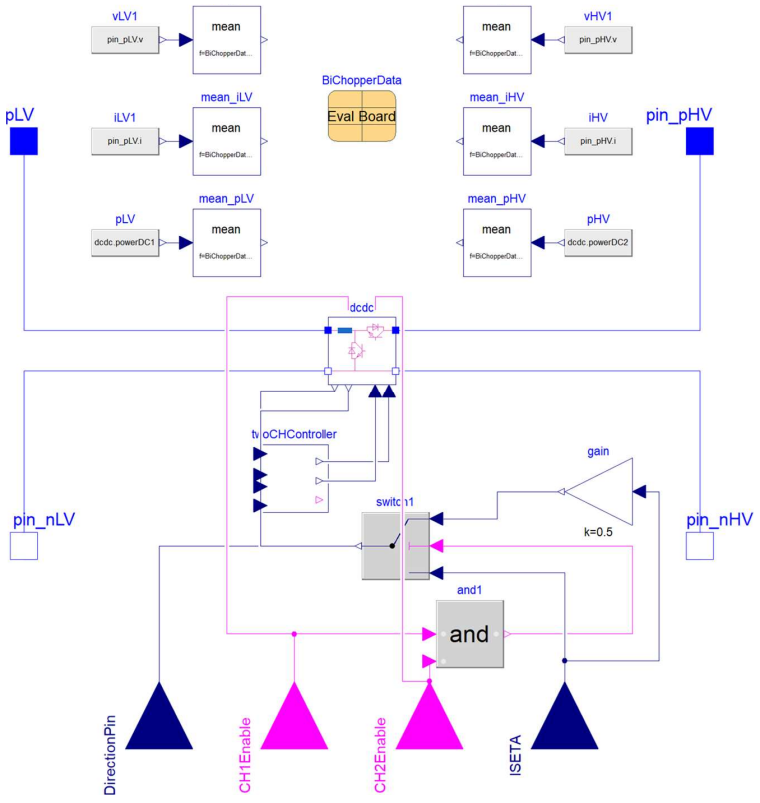


Figure 11.9: The model `ControlledBuckBoost` simulates the current controlled DC-DC converter with strictly complementary switching behavior.

11.4 Switching Model with Diode Emulated Mode

The switching model with diode emulation mode differs from the strictly complementary model only slightly in the control mode of the MOSFETs (Fig. 11.3). Figure 11.13 shows a hierarchical overview of the submodels and can also be divided into the simulation of the physical components and the control.
For the diode emulation, an additional model for changing the current direction (`CurrentDirectionCorrection`) and one for generating the control signals of the MOSFETs (`DiodeModeGen`) are added.

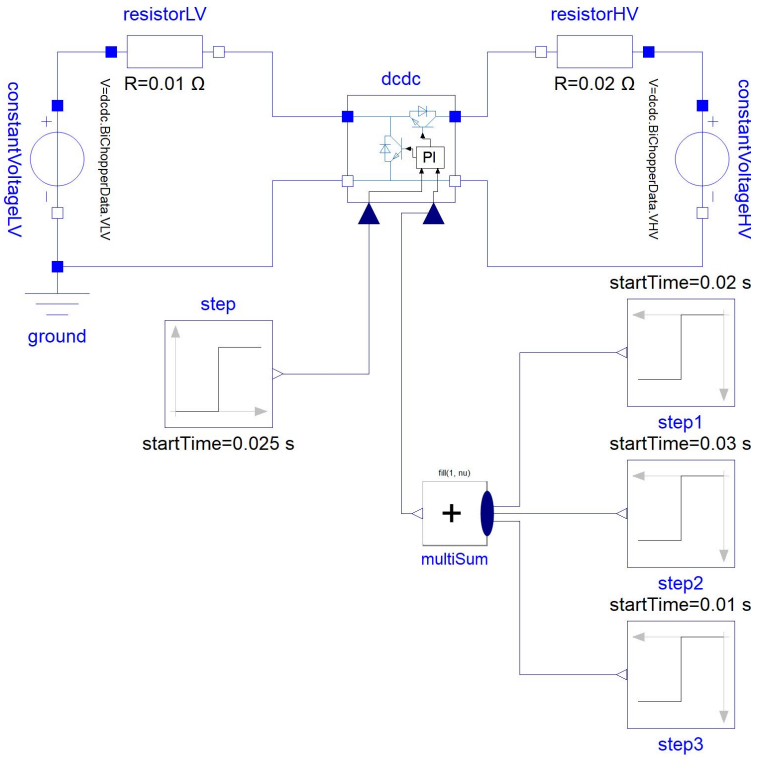


Figure 11.10: To verify the model, in this case `ControlledBuckBoost`, the step response is simulated and compared with the theoretical transfer function.

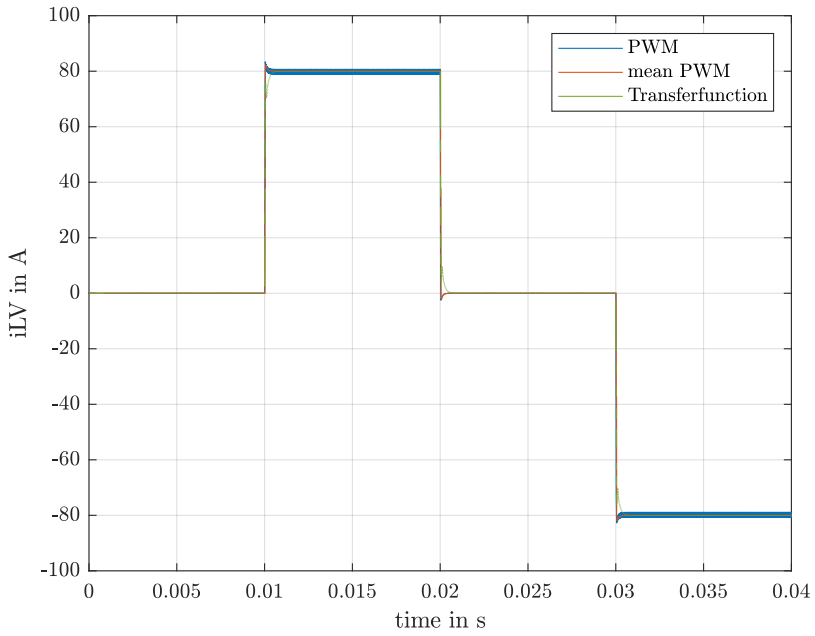


Figure 11.11: Comparison of the inductor current over time of the strictly complementary switching model and the theoretical transfer function.

11.4.1 Additional Control Models

In `CurrentDirectionCorrection`, the current through the inductor is compared with the set direction. If the current is positive or zero in relation to the mode of the

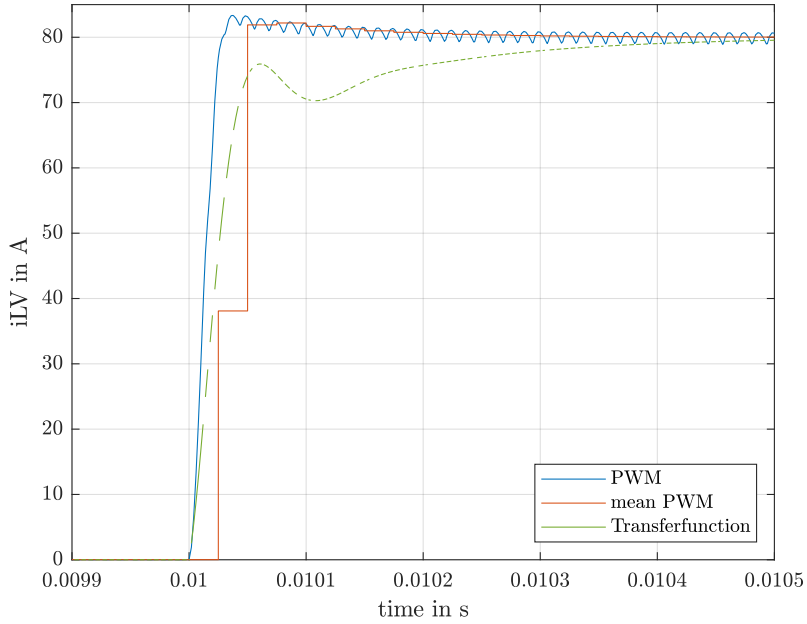


Figure 11.12: Step reponse of the strictly complementary switching model and the theoretical transfer function,

DC-DC converter, the output value is one, otherwise it is zero. The output is further processed in `DiodeModeGen`.
The model `DiodeModeGen` uses the duty cycle, the direction and the measured current through the inductor as inputs to define the switching signals for the two MOSFETs. The real signal `dutyCycle` is sampled over one period in `zeroOrderHold` and compared to a triangle signal. The compared signal is passed to the switches `logicSwitch` and `logicSwitch1` as an input. The inverse signal from the comparison between the PWM and the rectangular signal is passed to a logical-and block. The output signal from `currentDirectionCorrection` is the second input. The output signal of the logical-and block is one of the inputs of the switches. The direction is a further input of the switches in order to change between primary and secondary switching behavior of the respective MOSFET. The leading signal in `DiodeModeGen` corresponds to the hundredfold of the switching frequency and starts at the beginning of the simulation.

11.4.2 Validation of the Switching Model with Diode Emulation

The comparison with the theoretical transfer function shows only minor deviations (Fig. 11.16). A more detailed analysis of the step response shows that the model responds faster and with a higher accuracy compared to the transfer function (Fig. 11.17). Figure 11.18 shows a permanent control deviation caused by the `zeroOrderHold` element. This delays the measured current by a hundredth of the period of the switching frequency. Due to this delay, a zero crossing is detected belated and consequently the Sync-MOSFET is also switched off late. The deviation can be reduced by increasing the sampling frequency. This, however, increases the computational effort significantly. The jump at 0.025 s (Fig. 11.18) is caused by a change at the direction pin. As the measured current is multiplied by -1 due to the differing polarity of the direction, the sign of the deviation changes.

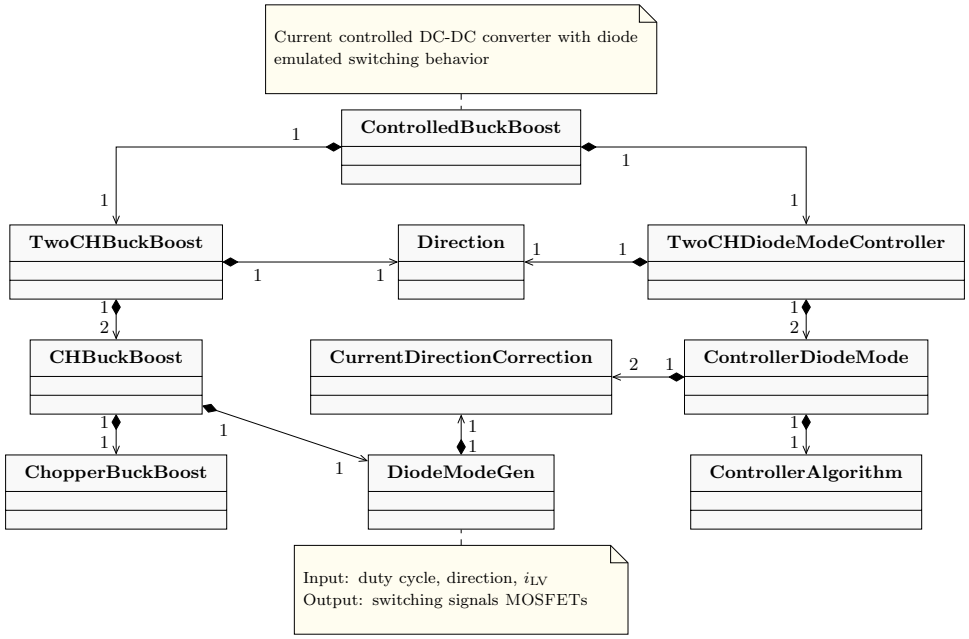


Figure 11.13: UML class diagram and overview of the composition of the various subclasses of the switching model with diode emulated mode `ControlledBuckBoost`.

Changing the switching threshold of the Sync-MOSFET from 0 A to 0.4 A shows only a minor deviation and the desired value of 0 A is maintained over the entire range (Fig. 11.19).

11.5 Averaging Model

Time-invariant devices, such as switching transistors, are very complex to simulate. They lead to a significant increase in computational effort and thus limit the number of components to be simulated simultaneously as well as the performance. To realize, e.g. a simulation of the behavior of a battery connected to the bidirectional DC-DC converter over several charging processes in order to make statements about aging processes, a suitable model is required [503]. In the following, a model is designed which neglects the single switching processes but still reproduces the behavior of the switching model as accurately as possible.

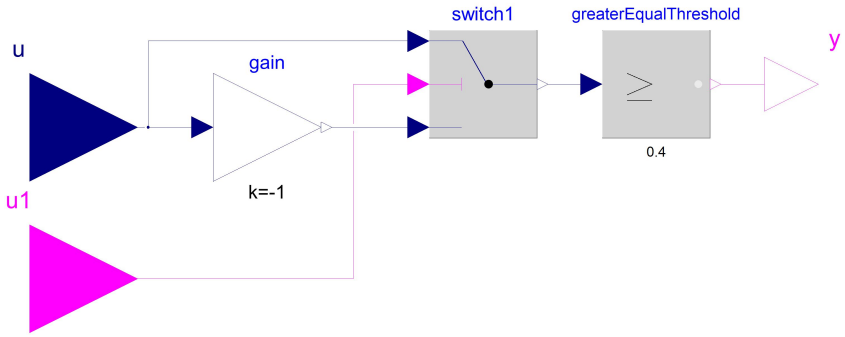


Figure 11.14: Overview of the model `CurrentDirectionCorrection` for the diode emulated mode. In this case, the switching threshold for diode emulation is 0.4 A instead of 0 A in order to reduce the deviation.

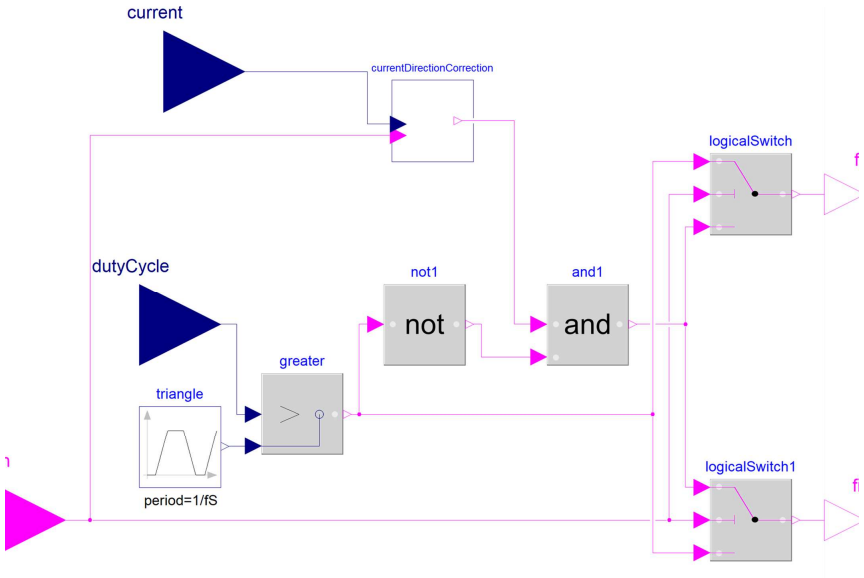


Figure 11.15: The model `DiodeModeGen` generates the switching signals for the MOSFETs according to the diode emulated mode (Fig. 11.3).

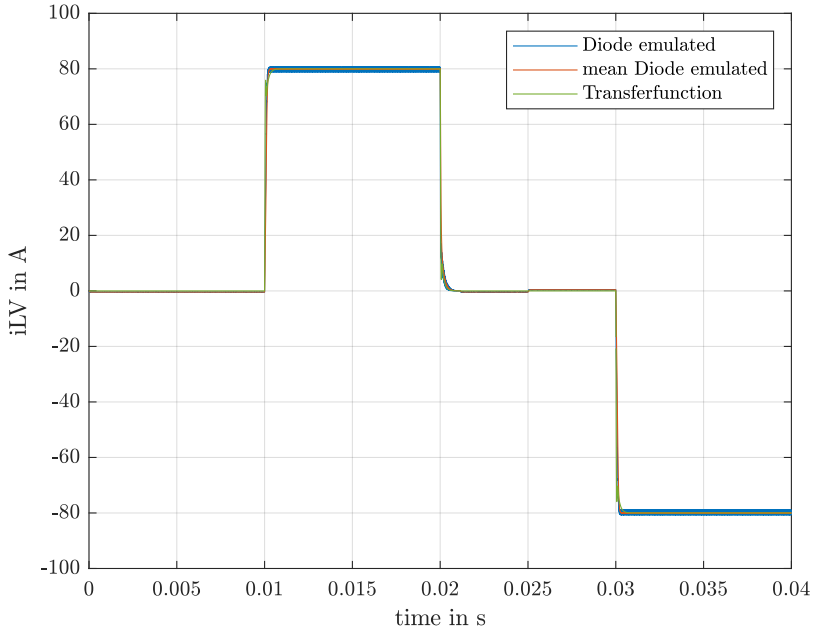


Figure 11.16: Comparison of the inductor current over time of the switching model with diode emulated mode and the theoretical transfer function.

The accuracy is lower compared to the switching models, but allows longer simulation duration with several components to be simulated simultaneously.
Without taking losses into account, the averaged output voltage in buck mode is given by:

$$V_{\text{av,ideal}} = (1 - D) \cdot V_{\text{HV}} \tag{11.2}$$

D describes the duty cycle. The following applies to the output current:

$$I_{\text{av,ideal}} = (1 - D) \cdot I_{\text{L}} \tag{11.3}$$

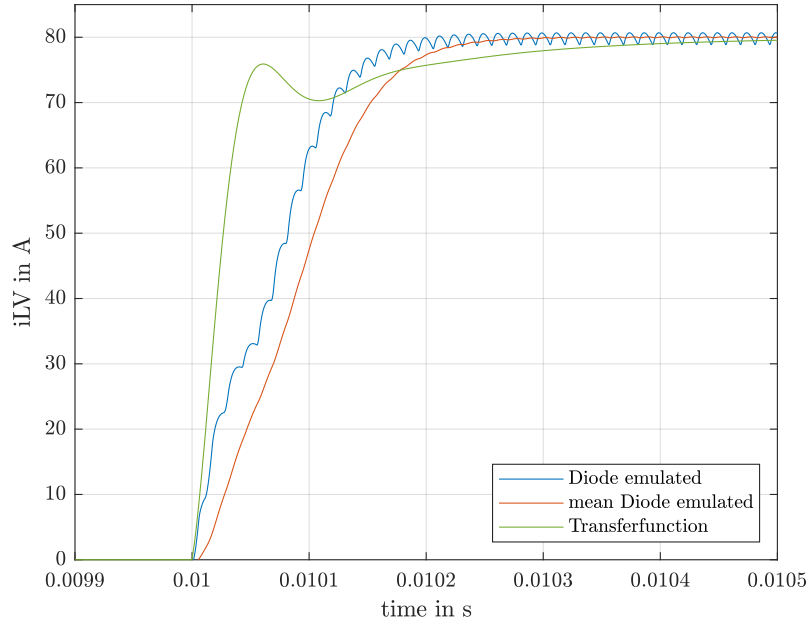


Figure 11.17: Step response of the switching model with diode emulated mode and the theoretical transfer function.

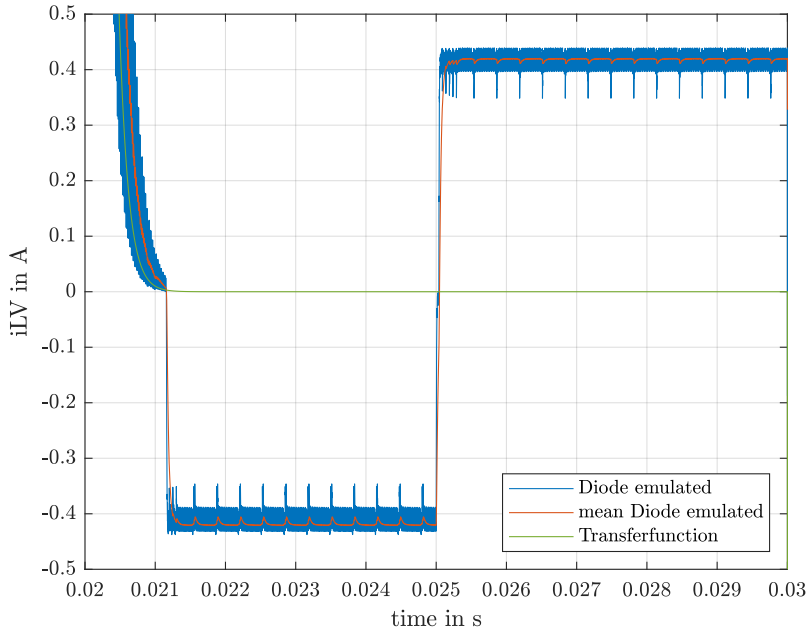


Figure 11.18: Detailed analysis of the step response showing significant deviation of the model using diode emulated mode. There is a deviation of approximately 0.4 V with the sign depending on the PWM phase.

In order to consider the ohmic losses of the MOSFETs, the voltage required by them is subtracted from the generated voltage. This results in:

$$V_{\text{av,real}} = (1-D)\cdot V_{\text{HV}} + \frac{P_{\text{V,Rds(on)LV}} + P_{\text{V,Rds(on)HV}}}{I_{\text{L}}} \tag{11.4}$$

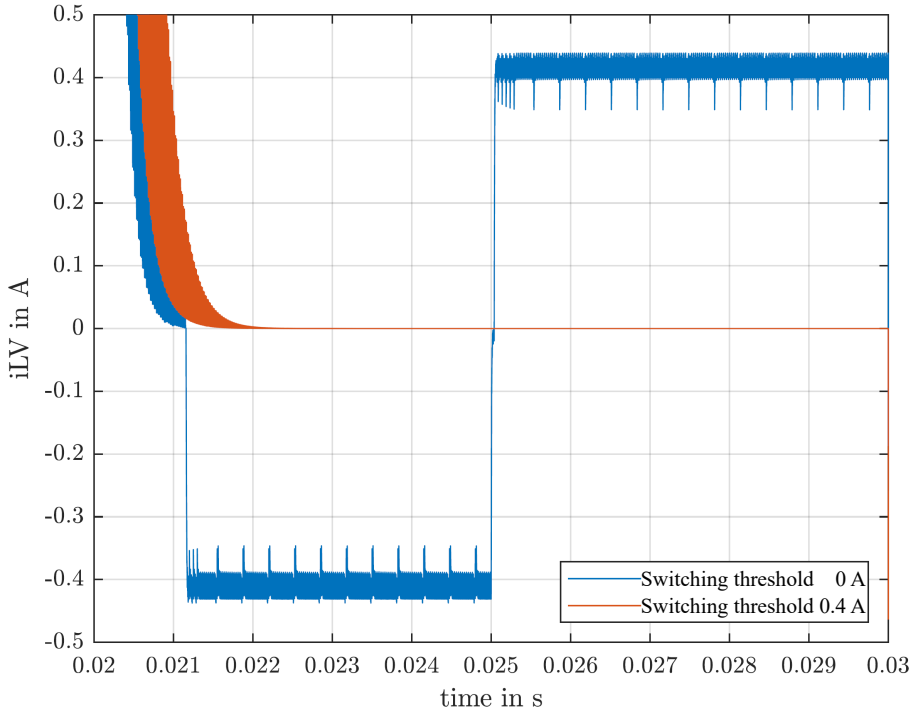


Figure 11.19: Reduction of the deviation by adjusting the current thresholds.

Assuming that the two MOSFETs are identical, the equation can be simplified to:

$$V_{\text{av,real}} = (2-D)\cdot V_{\text{HV}} + 2\cdot I_{\text{L}}\cdot R_{\text{on,Transistors}} \tag{11.5}$$

The averaging model is also hierarchical and is divided accordingly into physical and control simulation (Fig.11.20).

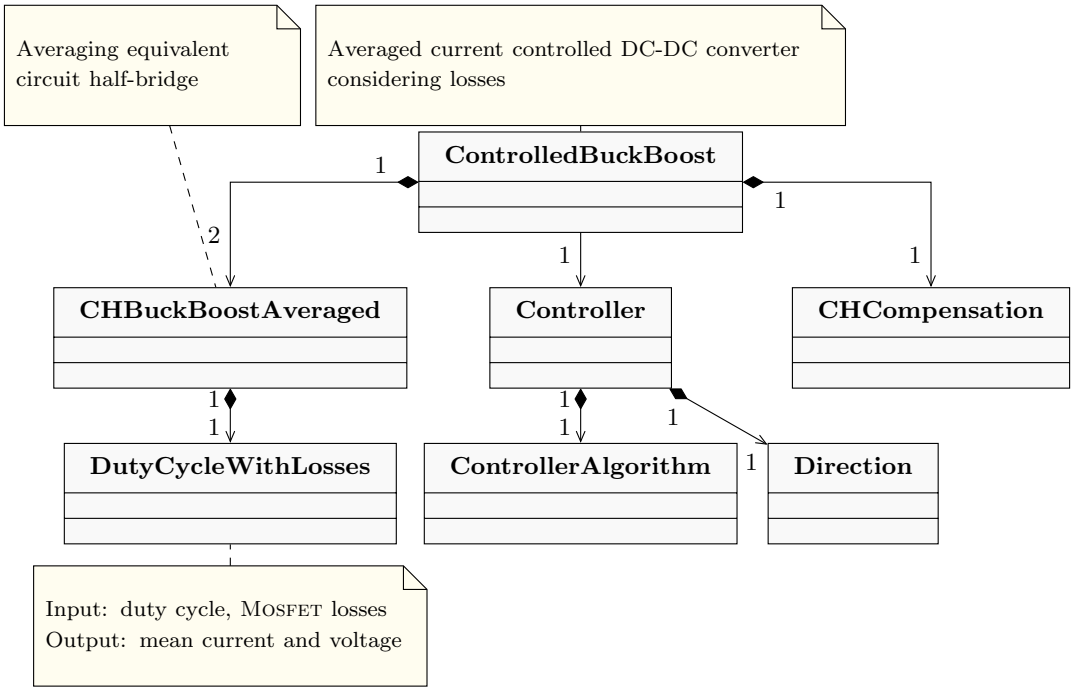


Figure 11.20: Hierarchical overview of the classes of the averaging model.

11.5.1 Physical Simulation

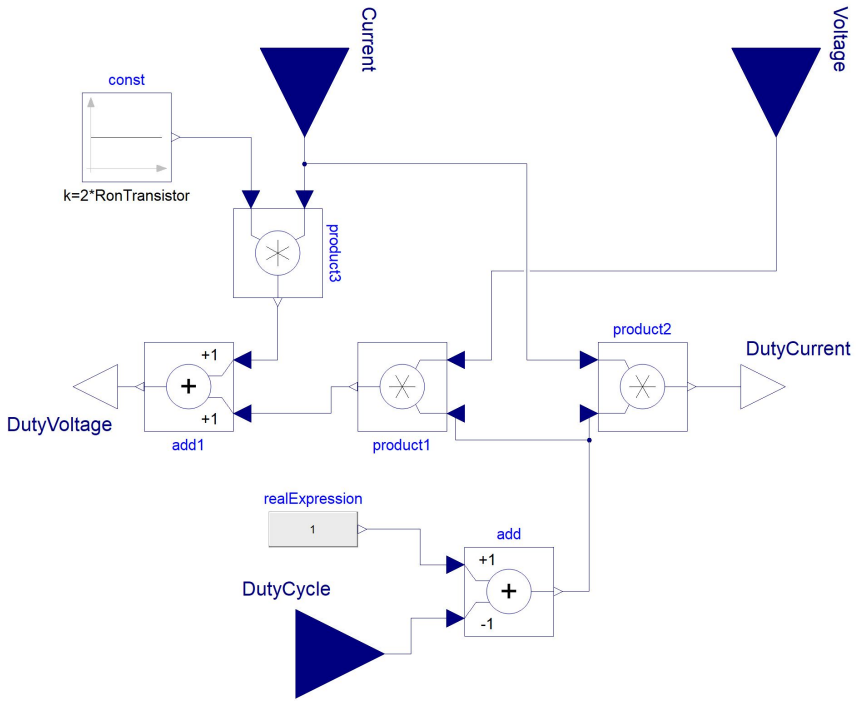


Figure 11.21: The model `DutyCycleWithLosses` determines the averaged output current and voltage according to the equations (11.3) and (11.4). `DutyVoltage` corresponds to $V_{\text{av,real}}$ and `DutyCurrent` to $I_{\text{av,ideal}}$

At the lowest level of the physical simulation, the averaged output currents and voltages are determined in the model `DutyCycleWithLosses` as a function of the input voltage or inductor current, the set duty cycle and the power losses of the MOSFETs (Fig. 11.21). The block `add` exchanges the `DutyCycle` so that the behavior of the averaging model corresponds to the one of the switching model. The corrected duty cycle is used together with the measured current and voltage to determine the averaged values, which are passed by the pins `DutyVoltage` and `DutyCurrent` to the model `CHBuckBoostAveraged`.
In this model, the MOSFETs are replaced by current and voltage sources which provide the average values (outputs `DutyCycleWithLosses`). Consequently, the inductor is charged by the voltage source `signalVoltage` and discharged via the current source `signalCurrent`. Since there are no ripples in the circuit, no smoothing capacitors are required. Another significant difference to the switching models (Fig. 11.5) is that the measured current is delayed via a PT1-element instead of a `zeroOrderHold` element. The reason for this is that it is interpreted as a switching element and thus delays the measured value used in the control algorithm.

11.5.2 Simulation of the Control

The controller blocks are almost identical to those of the switching variants, only the operating mode of the DC-DC converter via the `Direction` pin is not determined. The additional model `CHCompensation` adjust the ISETA signal depending of the activated channels. The parameters `EnableCH1` and `EnableCH2` are the boolean

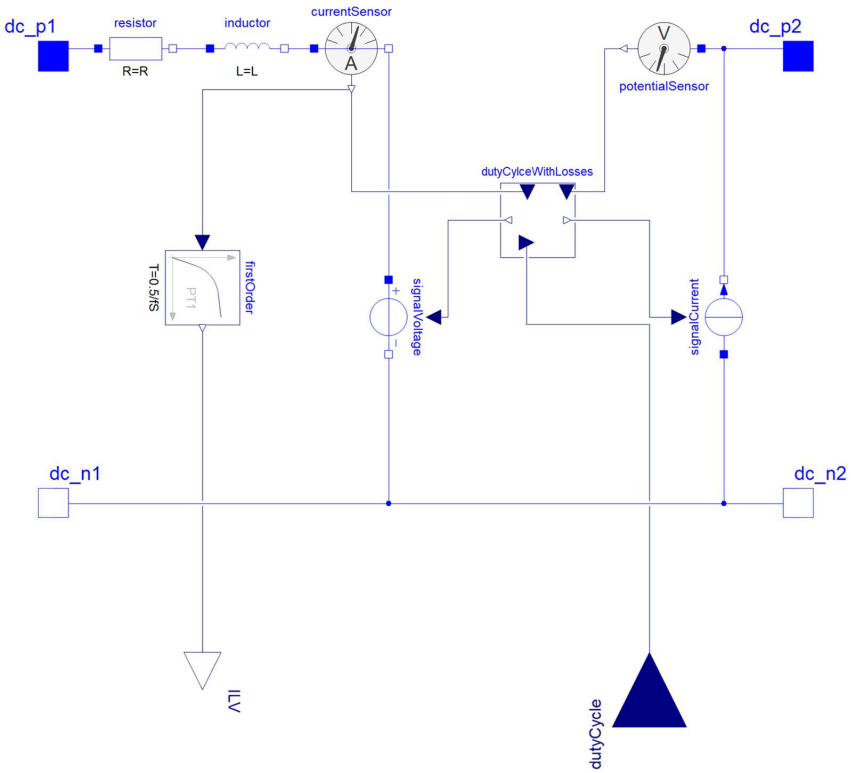


Figure 11.22: The model `CHBuckBoostAveraged` is the averaging model of one of the two half bridges. The MOSFETs are replaced by current and voltage sources which provide the average values.

inputs. If both channels are activated, the signal ISETA is halved other it is passed on without change.

11.5.3 Validation of the Averaging Model

A first comparison between the transfer function and the averaging model shows barely any deviations (Fig. 11.23). A more detailed comparison shows that the averaging model reacts faster to the jump, but takes longer to compensate the control deviation (Fig. 11.24). After 0.013 s (Fig. 11.24) the averaging model reaches the set point of 80 A, while the transfer function has a permanent control deviation of 0.0075 A. One possible reason for the remaining deviation could be that the theoretical transfer function is also an approximation.

11.6 Comparison of the Models

For the comparison between the models, the simulation processes (Fig. 11.10) are performed and the results are compared in terms of the computational time and effort. The simulations are executed on an Intel i5-4690K with 3.5 GHz. The experiment is performed at the same interval length of 2E-7 s and the tolerance of 1E-7 s in each case. The high resolution is required for the accuracy of the model with diode emulation mode. As expected, the averaging model is the one with the shortest computation time and only requires 3.829 s (Fig. 11.25). The strictly complementary switching model takes 13.708 s and the one with diode emulation mode 107.906 s. For the latter, a difference can be seen between the test conditions. If no zero

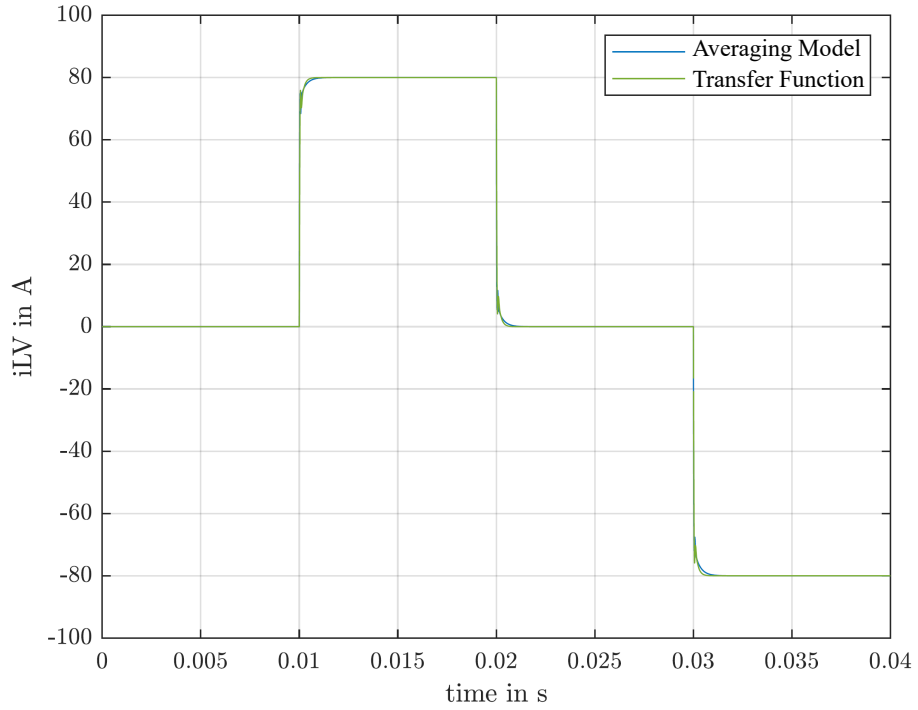


Figure 11.23: Comparison of the inductor current over time of the averaging model and the theoretical transfer function.

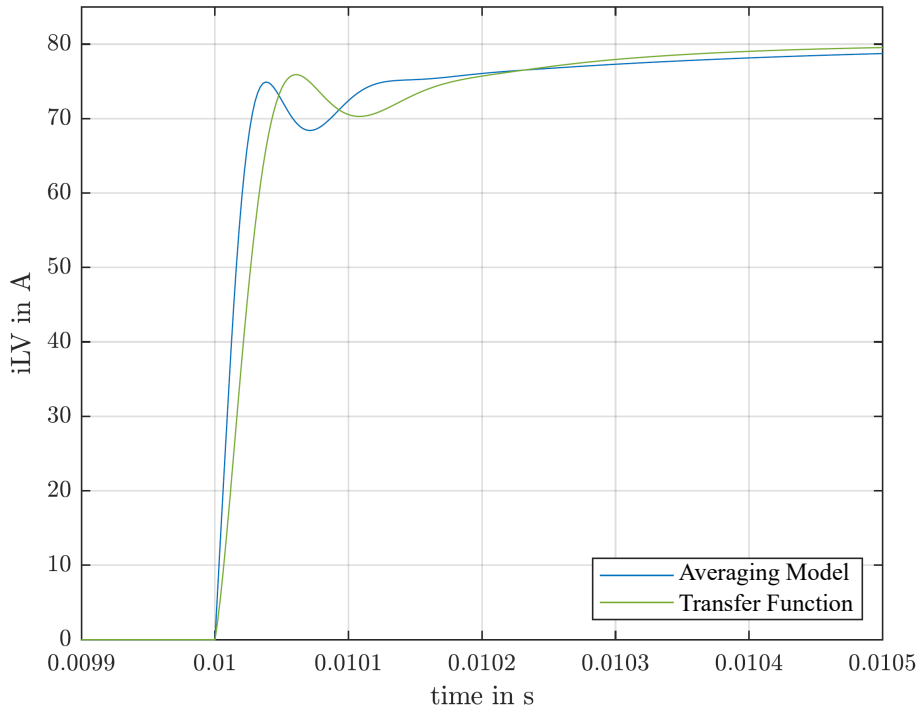


Figure 11.24: Step response of the averaging model and the theoretical transfer function.

crossings occur (Fig. 11.25: between the simulation time 0.01 s and app. 0.0215 s) , the performance of the model is significantly better compared to the segments with zero crossings and diode emulation (Fig. 11.25: between the simulation time 0 and 0.01 s) . The averaging model requires only 3.5% computation time of the duration of the model with diode emulation and less than a third (27.9%) of the computation time of the strictly complementary switching model. The computation time depends on the equations to be calculated. The diode emulated model requires the most

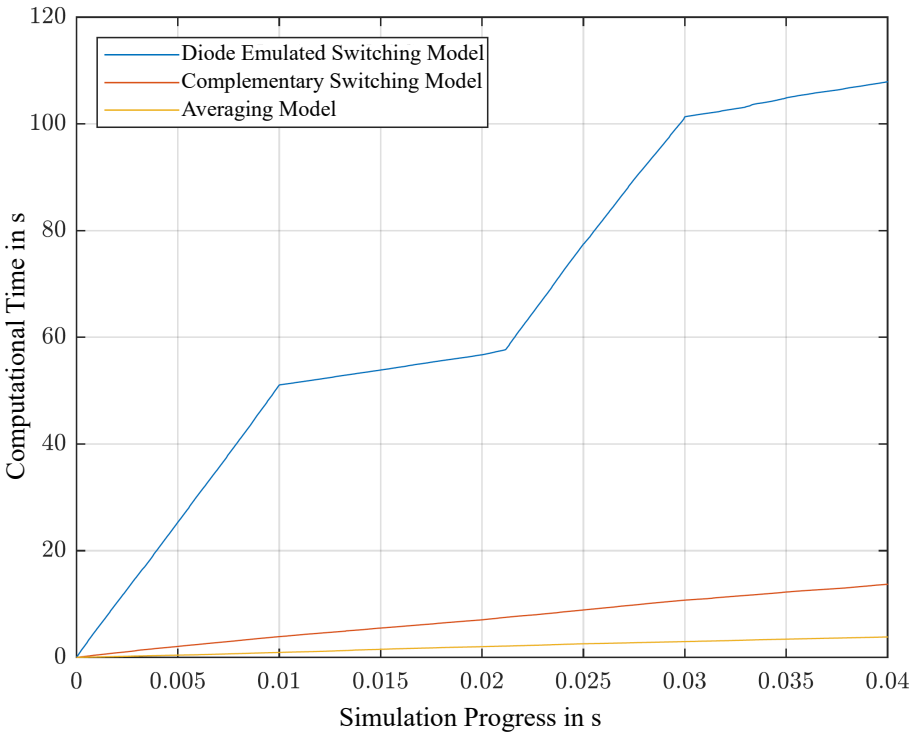


Figure 11.25: Comparison of the required computation time in relation to the simulation progress of the three proposed models.

equations with 503370 in total. The strictly complementary switching model uses 25963 equations and the averaging one only 7 equations.
This comparison shows, that the averaging model significantly reduces the computational effort and time. As long as individual switching processes are not relevant, the averaging model is the preferred choice. The strictly complementary switching model can be used if only the rippling signal is necessary, If information about the exact switching processes of the MOSFETs is required, the diode emulated model has to be selected.

11.7 Parallel Connection of two DC-DC Converters with Load Distribution

As an exemplary use case, the load sharing between two DC-DC converters connected in parallel is simulated. The averaging model with a PI controller is used (Fig. 11.26). The load sharing is realized in this case for a first test via the two gain blocks. These divide the drive signal between the two DC-DC converters by 70% and 30%.
The result in Figure 11.27 shows that the load current is distributed as demanded. The set point of 80 A is reached 1.51 ms later compared to Figure 11.24. The reason for this is the used PI controller. Parallel connections of the switching models show the same behavior and therefore are not shown.

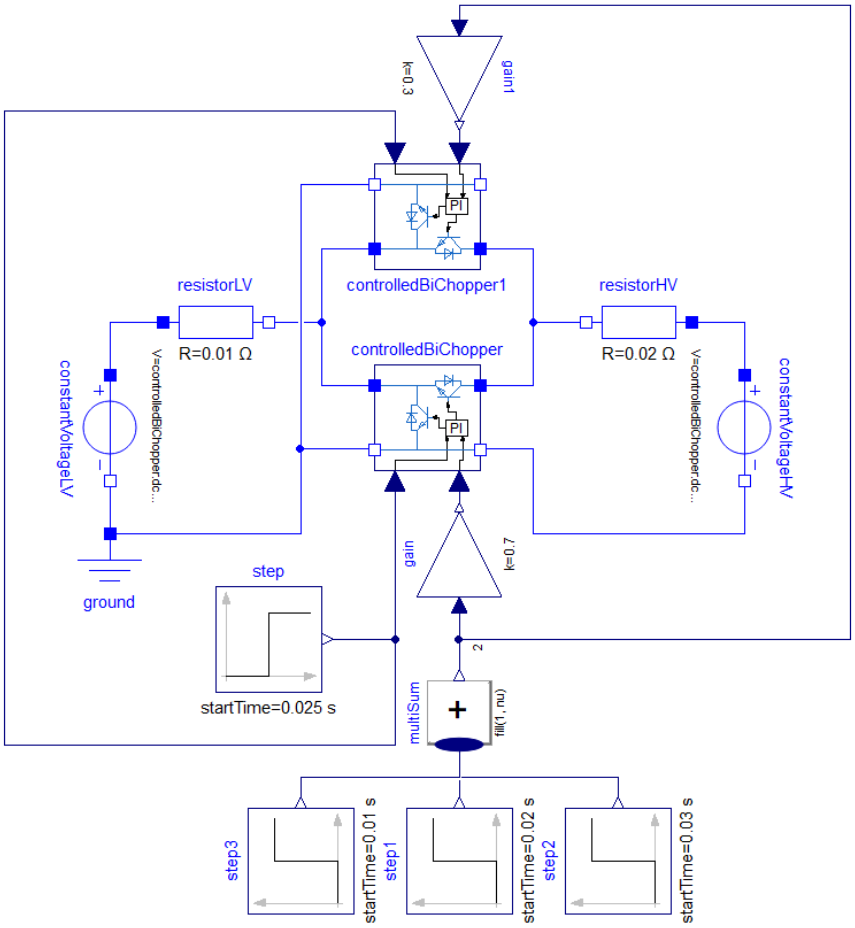


Figure 11.26: Possible use case of the averaging model: simulation of load sharing between two DC-DC converters connected in parallel, where one (`controlledBiChopper1`) consumes 30 percent of the charging current and the other one (`controlledBiChopper`) 70 percent.

11.8 Summary

Three different models of varying complexity have been proposed to simulate bidirectional DC-DC converters. Two switching models reproduce the individual switching operations and thus provides high accuracy. They differ essentially in driving mode, one of which switches the MOSFETs in a strictly complementary manner while the other one uses diode mode emulation. The strictly complementary switching model emulates current ripples and is suitable for simulation durations up to a few seconds. The model with diode mode emulation switches off the MOSFETs at currents lower than zero. This model is only suitable for simulations for less than one second, as the model requires high accuracy to provide precise values. For longer simulation durations, an averaging model was proposed. Here, the switching components are replaced with the average values. The model shows clear advantages in terms of computational effort and calculation time, but offers lower accuracy. All three models were successfully validated by comparisons with the theoretical transfer function. The proposed models are the basis for more extensive system simulations. Especially the averaging model offers the possibility to realize longer simulation durations.

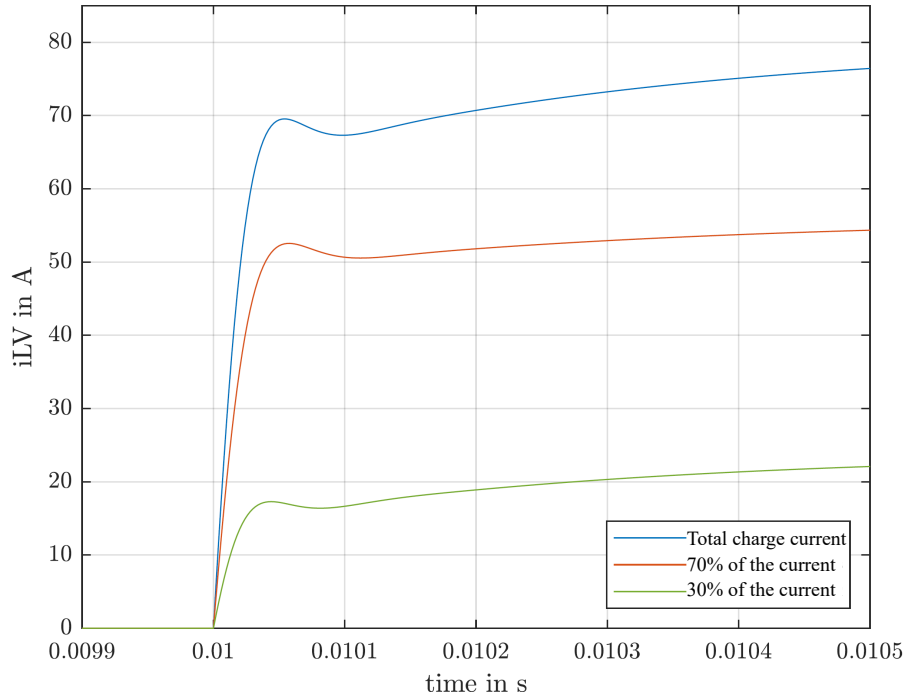


Figure 11.27: Step response of the parallel connection of two DC-DC converters with load current sharing using the averaging models.

In future work, a more detailed consideration of the losses is planned. Separate heat ports for the individual components will be added to analyze the individual losses. Another extension is to make the load sharing between the DC-DC converters changeable during the simulation. The transfer functions of the DC-DC converter were defined in previous work. These will also be integrated into the simulation environment and compared with the averaging models in terms of computational effort and accuracy.

12

Framework for Testing and Evaluating Communication-based Controlled DC-DC Converters

DC-DC converters control the power flow and thus the power distribution between the components on different voltage levels. They are essential for (dis)charging batteries and influence the safety and stability of the entire battery management system (BMS). Therefore, testing the functionality and the reliability of DC-DC converters is crucial. This is especially true for decentralized battery management systems (DBMS), where multiple nodes communicate to collectively control the system. The used DC-DC converters are modified to parameterize them during operation via microcontroller interfaces. Integrating the communication into the control loop requires an analysis of the control behavior due to additional delays. Therefore, this chapter proposes a framework to test DC-DC converters considering the control and communication perspectives. The response time, the control accuracy and stability of these DC-DC converters, e.g., under continuous and abrupt load changes, are measured in automated tests. The dedicated software framework simulates the DBMS and stimulates the hardware components (e.g. electronic loads, data acquisition) via respective interfaces (CAN, RS232). This allows the test of various DC-DC converters with flexibly adaptable load and power generation profiles. An initial application validates the test framework by verifying the aforementioned aspects and thus the applicability of a DC-DC converter within the DBMS.

12.1 Motivation

Battery management systems (BMS) administer system control and management with regard to energy storage and transmission [504]. Decentralized BMS (DBMS) are characterized by autonomous and locally operating control units attached to each battery. They offer significant advantages including scalability, easier maintenance and integration. By placing the sensing and control units closer to the battery and

avoiding the dependence on a central master controller, potential single points of failures are minimized. An own approach of a DBMS was proposed [315], which also involves electrical sources and loads in addition to the batteries, in contrast to existing approaches [224, 225, 231]. All components are connected by a power line and at least one global communication line (Fig. 12.1).
For distributed control, each component is equipped with its own Local Control Unit (LCU), which includes:

- Current, voltage and temperature sensors,
- communication interfaces for local and global data exchange,
- a microcontroller for calculation and data management,
- a DC-DC converter with adjustable current and voltage limits by a microcontroller interface and
- a relay which is opened in case of failures or for maintenance.

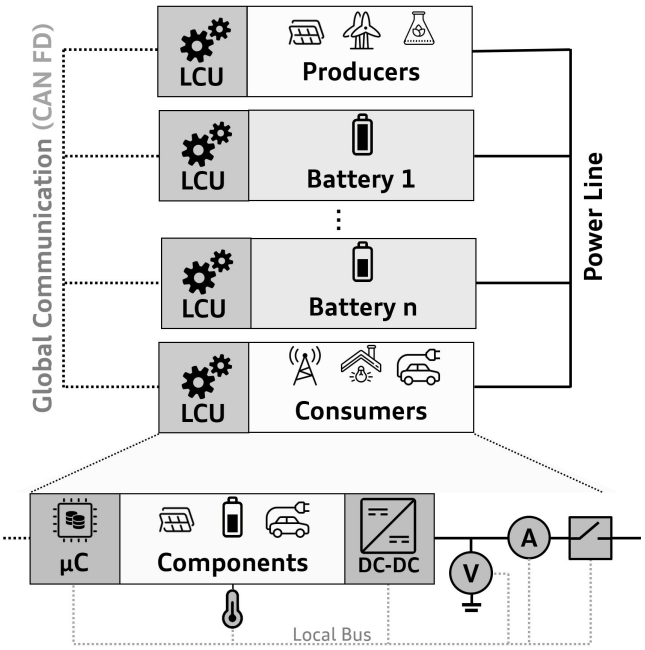


Figure 12.1: Overview of the decentralized battery management system (top) and detailed presentation of a component with a local control unit (LCU) (bottom).

One of the battery nodes coordinates the global control. It specifies the required (dis)charge power of the remaining battery nodes, which manage their local control loops.
The DC-DC converters work as actuators and provide the power distribution between the components at different voltage levels [505]. They are essential for the (dis)charge of the batteries and influence the control stability of the overall system [506]. The DC-DC converters operating in this DBMS need to be validated under a range of conditions to ensure safety and reliability [506, 507]. They have to achieve a stable output voltage and a precise load current distribution. The response time is crucial for the global control and has to be tested. It is composed of

- the transmission of the setpoints via CAN (FD) messages,
- the adjustment of the control variables of the DC-DC converter by the microcontroller and
- the propagation delay of the DC-DC converter.

Comparison to Related Work

While there are numerous DC-DC converter test frameworks, it is difficult to find one that encompasses the aspects of networked control. Delays in the global control messages and possible data dropouts have a significant impact on the functionality and reliability. Consequently, the cooperatively control has to be considered. Application and hardware-specific additional interfaces are required to connect the hardware [508, 509]. Existing test approaches often need dedicated hardware-in-the-loop platforms such as dSPACE [510–512], where the underlying models are programmed in MATLAB/Simulink [513] or LabVIEW [514]. In contrast, Python, an established object-oriented open-source language, integrates the capabilities of simulation and testing of hardware components in one system.

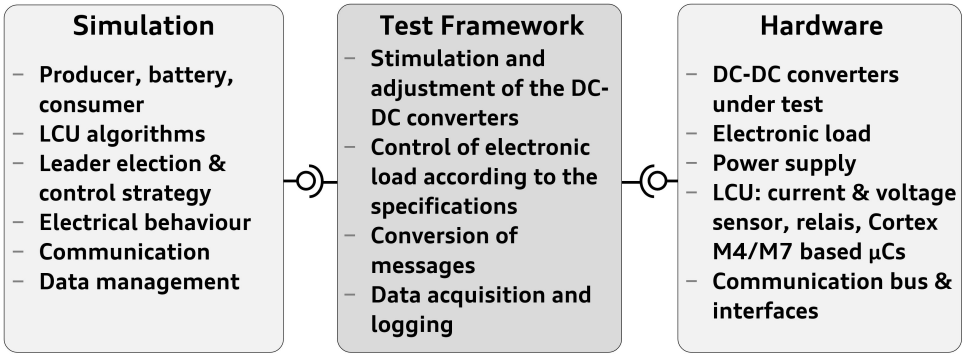


Figure 12.2: Functional description and correlation of the simulation [237], the test framework and the hardware.

Contributions

In order to address the challenges, a test framework fulfilling the following requirements is needed. It considers the coupled control and communication perspectives to determine

- the response time,
- the control accuracy and
- the stability

of the DC-DC converters in various test scenarios including continuous and abrupt load changes realized by an electronic load. The support of automated tests is required to realize the comparison between different DC-DC converters and to evaluate their usability within the DBMS. Due to the digital control via the microcontroller and the customizable test framework, it is possible to apply different and multiple DC-DC converters simultaneously to investigate the interaction and load distribution among them.

Within a previously developed simulation [237], the DBMS can be effectively modified corresponding to various applications. The test framework has to provide the stimulation of the test case simulation hardware, including the electronic load and the DC-DC converters under test (DUT), according to the simulation data (Fig. 12.2). The proposed Python-based test framework combines the flexibility of a software simulation [237] with the improved results by using real hardware components to test networked and digitally controlled DC-DC converters within a DBMS.

Organization

The requirements of the test framework are analysed in Section 12.2. In Section 12.3, the architecture including the used hardware components, the developed software design and the applied test algorithm are described. To validate the proposed test framework, initial test results are shown and discussed in Section 12.4. The control stability and accuracy under load changes and the reaction speed of a DC-DC converter are thereby investigated. Finally a conclusion is drawn and possible future extensions and further developments are discussed.

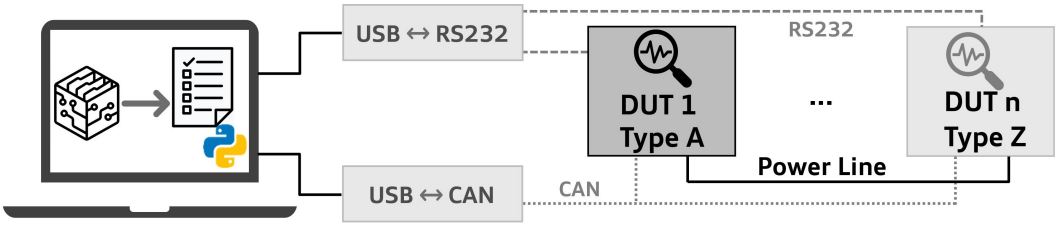


Figure 12.3: Test architecture for several DUTs, possibly of mixed types.

12.2 Requirements Analysis for the Test Framework

In the following the requirements of the test framework are analyzed.

12.2.1 Hardware Control According to the Simulation Data

For validation and verification of the DC-DC converters, a previously developed DBMS simulation [237] is used: The electrical behavior, the data communication and the LCUs of the DBMS are simulated and provide different test scenarios. A connection between the BMS simulation software and the hardware under test is required, driving the actuators and recording measured physical values (Fig. 12.2).

12.2.2 Scalability and Flexibility of the Test Framework

For different use cases and test scenarios, application-specific load profiles are required and the load sharing between DC-DC converters of the same or of different types has to be supported (Figs. 12.3 and 12.4). Comparing response time, control accuracy and stability enables the evaluation of the DUT in terms of its usability within a DBMS.

12.2.3 Various Test Scenarios for Improved Testability with Adjustable Profiles

In order to validate and verify the function of the DC-DC converters for a wide range of applications and operating modes, variable test scenarios are required. For an initial design, the response time and the control stability of the DC-DC converter are tested under continuous and abrupt, transient load changes (Fig. 12.8). The number and magnitude of the load changes depends on the properties of the DUT. Therefore, the test framework needs to apply adjustable load profiles while managing, processing and analyzing the measured physical values.

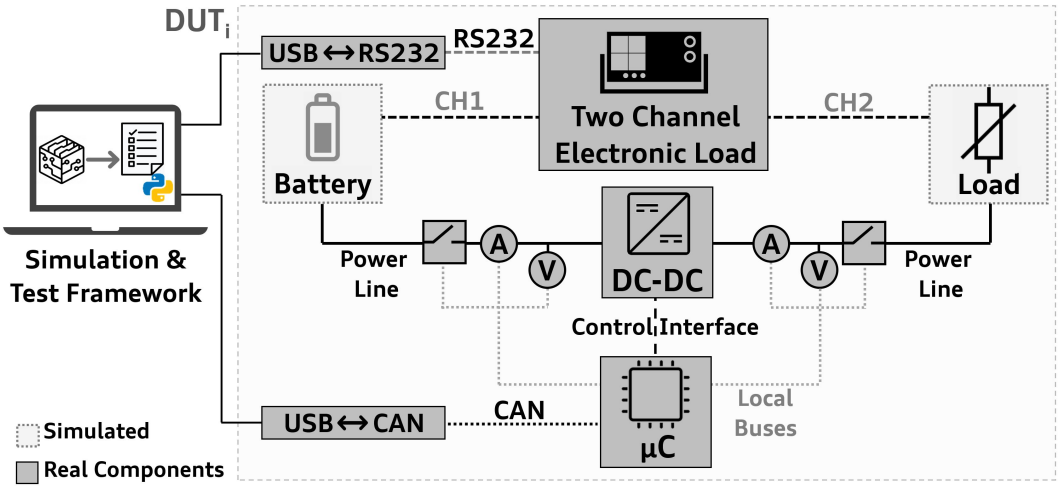


Figure 12.4: Connection of a hardware DUT_i to the software simulation.

12.3 System Architecture of the Test Framework

The proposed test framework consists of hardware and software components (Fig. 12.4).

12.3.1 Hardware Components

The hardware components of the test framework are described in this section.

1) Local Control Unit and Communication Interface

The LCU provides current and voltage sensors, a relay, a communication interface and a microcontroller (Fig. 12.1). The microcontroller receives the current and voltage target values via the communication line, controls the DC-DC converter according to the specifications and records the actual status by reading out the sensors. To verify the accuracy and stability of the current and voltage control of the DUT, corresponding sensors are located at both sides (Fig. 12.4). For the logging and evaluation of the results, the microcontroller sends the raw data with a time stamp back via the global communication interface.
The proposed framework implements testing of several DC-DC converters communicating over the network and controlling the system in a collaborative manner. Communication-based load sharing is a non-trivial task which requires a holistic testbed to ensure the safe and reliable operation of DC-DC converters within the DBMS. To realize the communication between test software (PC) and the microcontroller with a CAN bus a commercial USB-to-CAN interface [515] is used (Figs. 12.3 and 12.4). CAN (FD) messages enable the interaction between the LCUs (Fig. 12.1) and between the test software and the DUTs (Fig. 12.7) [303]. This enables the investigation of the condition-dependent, communication-based load sharing among the DUTs. The microcrontroller provides a wide range of control interfaces, including SPI, UART, I^2C and PWM signals, enabling effective adaptation to different DUTs and thus test scenarios for various applications (Fig. 12.4).

2) Programmable, Electronic Load

A programmable electronic load is used to test DC-DC converters under real conditions (Fig. 12.4) by working as power drain or source, depending on the test case. Each of the two channels provides a power (producer) and a load (consumer) mode. The operating modes *load* and *power* are adjustable via software commands and can be changed during operation. Associated Standard Commands for Programmable Instruments (SCPIs) (Fig. 12.6), a specific language for the control of programmable instruments standardized by IEEE 488.2 [516], are sent via the serial interface RS232 to the electronic load.
The dual power flow direction allows the testing of bidirectional DC-DC converters. Limiting DC-DC parameters (max. voltage/current) according to the DC-DC specifications are observed. The electronic load offers sequence functions to create individual voltage or power supply profiles. Pre-programmed templates can be used, whereby parameters for maximum and minimum limits, starting point and duration can be adjusted. Additionally individual points of the sequence can be set and arbitrary curves can be composed. For the effective generation of load and charge profiles an own special library (`eLoadLib`) is developed (Fig. 12.7). Every DUT requires such an electronic load, but there is no restriction in attaching additional DUTs.

12.3.2 Software Design

The software of the test framework bridges the simulation and the hardware components (Fig. 12.7). Fig. 12.5 shows an overview of the implemented and used classes.

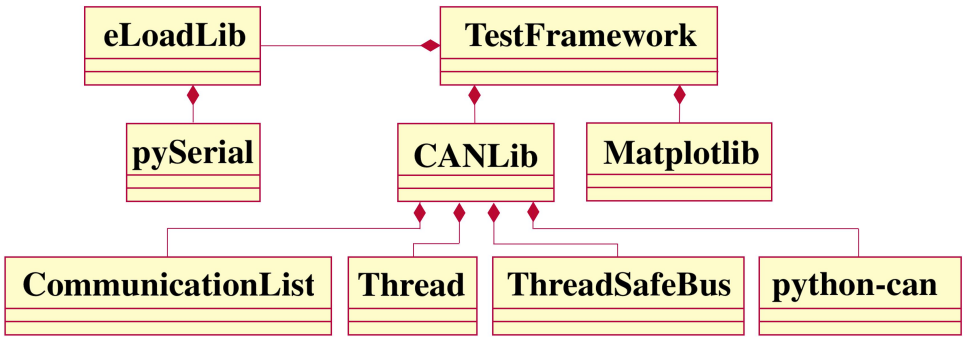


Figure 12.5: Software design of the test framework.

1) eLoadLib: Library for Controlling the Programmable, Electronic Load

In order to effectively control the electronic load, the library `eLoadLib` was implemented, which converts the specifications from the simulation or a measurement series into SCPI (Fig. 12.6). For example, the command `:MEAS2:VOLT?` is used for the output voltage measurement on channel 2. For the efficient use of the electronic load, the library `eLoadLib` provides a number of functions including set, get, add and measure functions and in addition to that error handling mechanism. According to the call of the function and the optional parameters, the corresponding SCPI instructions are generated and sent. Addressing a COM port is thereby implemented with the

Python library `pySerial` [517]. Error handling ensures valid parameter setting and correct command reception. Functions of the library `eLoadLib` allow the setting and querying of parameters of the electronic load.

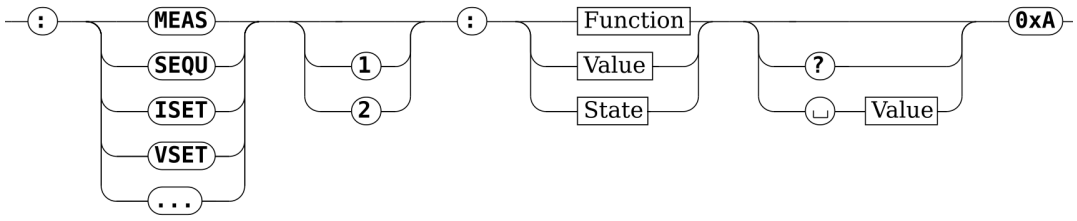


Figure 12.6: Extract and syntax example of the SCPI to configure the electronic load

2) CAN Library for the Implementation of a Communication Interface to the Local Control Unit

CAN (FD) is used for communication with the LCU in the initial tests, whereby also additional communication interfaces are provided. The developed library `CANLib` establishes a connection between the test environment and the USB-to-CAN interface and organizes the sending and receiving of CAN messages. It provides the communication of the current and voltage target values to the LCUs and the actual current and voltage values at the input and output side of the DUTs to the test framework.
It contains two objects of the class `CommunicationList` to extend the receive and transmit FIFOs (Rx-, Tx-FIFOs) within the CAN controller to avoid data overflow. Separate thread objects send, receive and process messages. This ensures that the Rx- and Tx-FIFOs are regularly and independently updated.
The library `python-can` allows several threads to access an object and manages multiple accesses to global variables [518]. The use of threads optimally coordinates the timing and the exchange of messages. Additionally, the `CANLib` offers an error tracking function to check if the message was received correctly, taking into account the expected value, parameters and processing.

3) Use of Real or Simulated Data

Besides data from the simulation of the DBMS also load data of real consumers and batteries can be imported to test the DUT. Files in a .txt format are used for an efficient data exchange e.g., the actual load value or the (dis)charge power of the components. An own transmission protocol is defined (Tab. 12.1). It contains the functions of the electronic load and the setting options of the DUTs in a compact manner.
For example, the instruction `DCDC 1 24 1.5 True` activates the DC-DC converter with the ID 0x01, sets the output voltage to 24 V and the output current to 1.5 A. Based on the custom defined syntax, corresponding functions are called. The respective SCPI commands are generated and executed. The class `TestFramework` contains objects of the class `eLoadLib` and `CANLib` (Fig. 12.5). It provides the interaction between the simulation and the hardware components (Fig. 12.7).

Table 12.1: Instructions and examples of the transmission protocol

Instruction	Description
PWR	Current (C) and voltage (V) setting with optional over voltage (OVP) and over current (OCP) protection for each channel (CH) Example: CH V C OVP OCP
LOAD	Load setting with optional OVP and OCP Example: CH MODE VAL OVP OCP
SEQ POINT	Setting of individual points in the sequence Example: CH NR V C TIME
SEQ TEMP	Parameterization of templates Example: OBJ CH START POINTS TIME MIN MAX TYPE INV/RATE SYM WIDTH
DCDC	Setting of output voltage and current of the DC-DC converter Example: ID V C OUT

12.4 Test Scenarios for an Initial Validation and Verification of the DC-DC Converters

In the following, two different DC-DC converters are tested and the functionality of the test framework is demonstrated.

12.4.1 Test algorithm and Processing of the Results

In this section, the framework is verified and validated with test scenarios. In order to achieve this, both independent measuring units of the electronic load and of the LCU record the actual sensor data using the corresponding `measure` functions. The LCU periodically polls the current and voltage sensors by default and reports all results with time stamps via CAN messages. Selected parameters to be additionally measured can be individually adapted and extended. After completion of a test run, the data are summarized in graphs to display the results and saved in a .csv file [519].

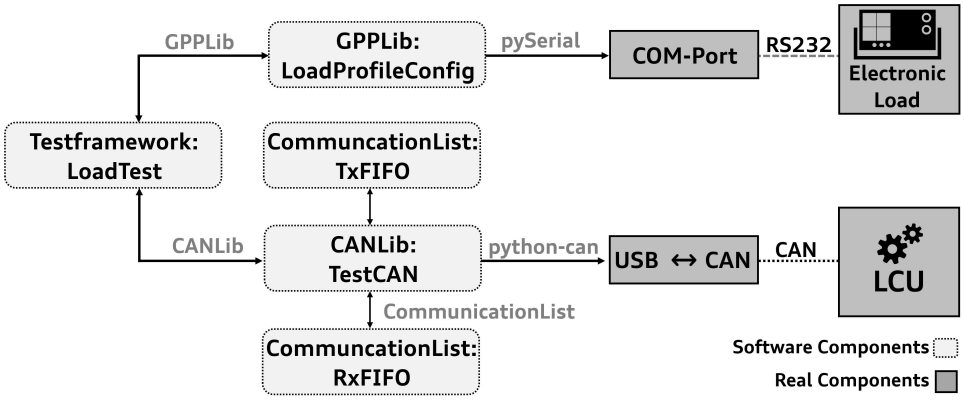


Figure 12.7: Overview of the software and hardware components of the test framework

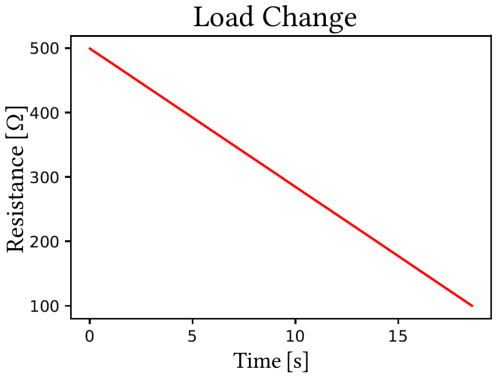


Figure 12.8: Load test with continuous load change

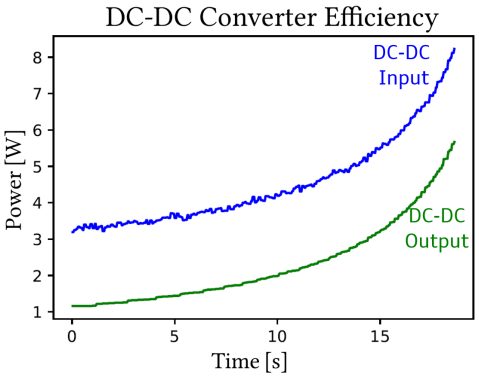


Figure 12.9: Efficiency of the DC-DC converter [520]

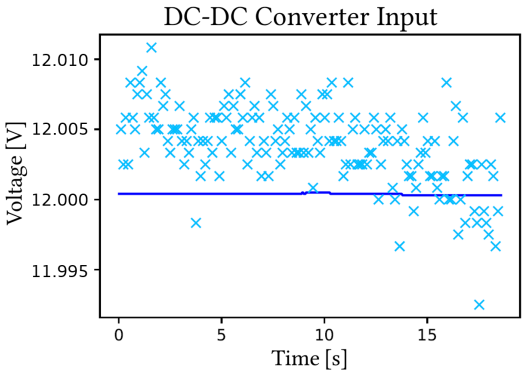


Figure 12.10: Voltage at the input of the DUT [520]

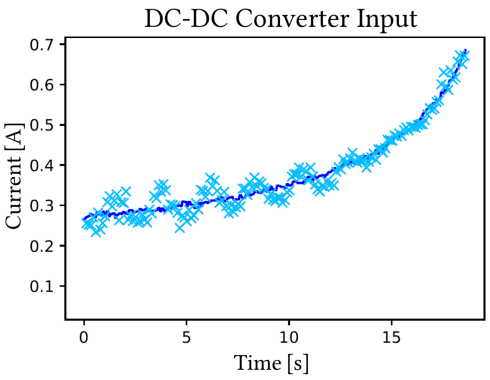


Figure 12.11: Current at the input of the DUT [520]

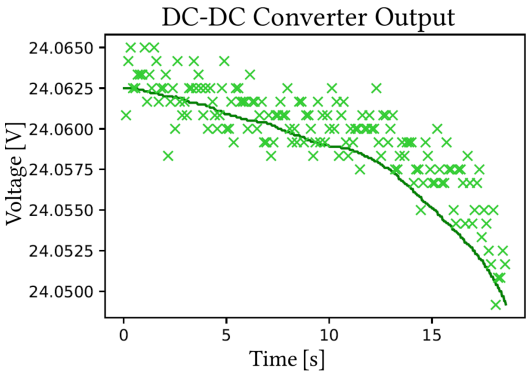


Figure 12.12: Voltage at the output of the DUT [520]

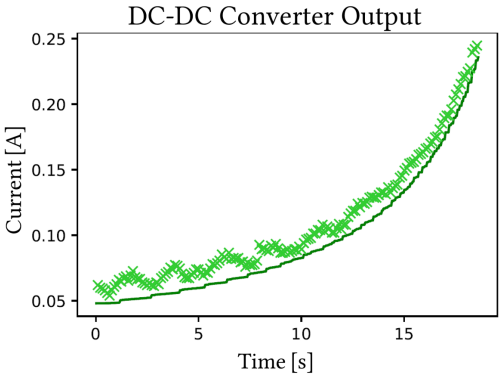


Figure 12.13: Current at the output of the DUT [520]

12.4.2 Implemented Test Scenarios

In order to evaluate DC-DC converters regarding their usability in a DBMS three different test scenarios were developed initially. In order to fully validate DC-DC converters within the DBMS, comparative tests have to be performed for all operating modes, including system startup and safe shutdown, and for various load profiles. However, since the scope of this chapter is to introduce the setup itself capable of testing multiple DC-DC converters cooperating over a communication network, complete testing results will be provided in a future work.

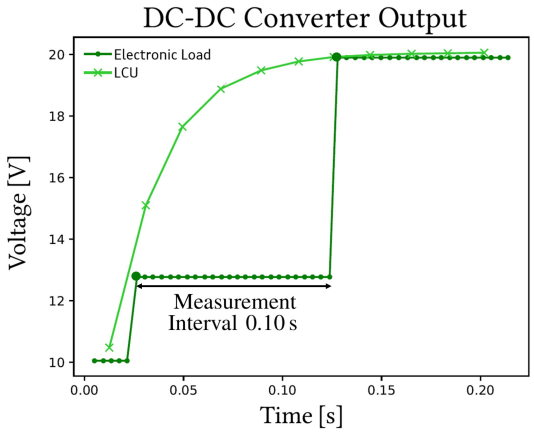


Figure 12.14: Measurement of the response time considering the networked control of the DC-DC converter[520] .

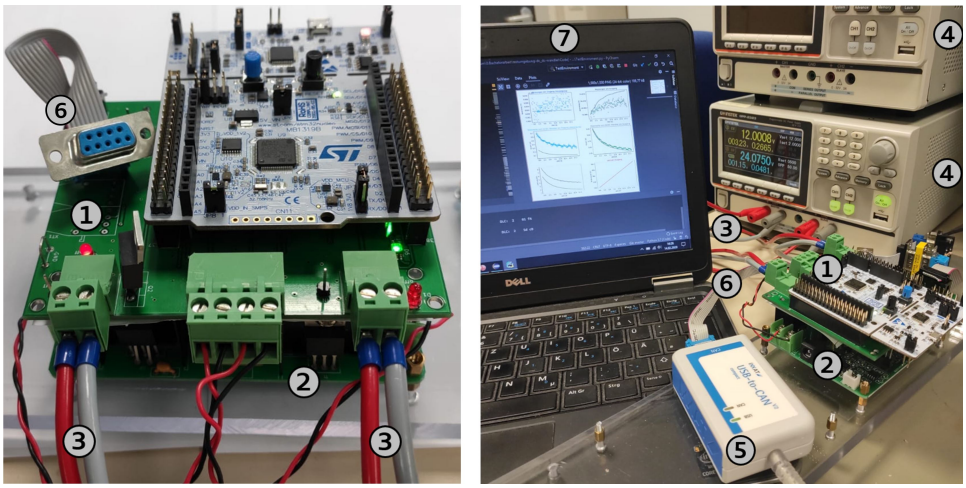


Figure 12.15: The test setup consists of the LCU using a Cortex-M4 microcontroller ①, the DC-DC converter to be tested [520] ②, which is connected to the electronic load [521] ④ via power lines ③. A CAN-to-USB interface ⑤ and a CAN line ⑥ are used for data transfer between the PC ⑦ and the DUT ① – ④.

1) Response Time Test

The reaction speed of the DC-DC converter directly influences the control within the DBMS and is therefore a relevant evaluation criterion. It is tested how fast the DC-DC converter reacts to a command transmitted via the CAN line and how long it takes to reach the desired output power. The generation, transmission and processing of CAN messages were measured in a previous work [303].

2) Load Test

The stability and accuracy of the power control by the DC-DC converter is a prerequisite for a fair, condition-based power distribution. Neither abrupt nor continuous load changes should influence the control of the DC-DC converter. Therefore, the control behavior is tested with abrupt and continuous load changes.

3) Supply Voltage Tests

Drops in the input voltage may also affect the stability and accuracy of the control and the output voltage. Therefore, the control of the DC-DC converter is investigated in case of supply voltage changes. Also in this case continuous as well as abrupt changes are considered.

12.5 Validation of the Test Framework

Initial tests to validate the framework have already been performed. The overall setup of the first test consists of the DC-DC converter to be tested, in this case a unidirectional, combined buck and boost converter [520], the LCU designed as a plug-on board, the electronic load, power lines, a CAN line with CAN-to-USB interface and a PC (Fig. 12.15). The DC-DC converter under test was adapted according to the requirements of the networked, communication-based control and is steered by PWM signals.
Figs. 12.8 - 12.13 show the test results for a load test with continuous load change. Fixed setpoints are specified via the CAN line: 24 V output voltage and a current limitation of 1 A. It is tested whether the DC-DC converter regulates to the specified target values and whether the control remains stable even with load changes. The control of this DC-DC converter remains stable, with output voltage values fluctuating in a range between 24.06 V and 24.05 V (Fig.12.12). Current and voltage measurements include both the electronic load measurements (solid line) and the LCU measurements (marked by crosses). Fig. 12.9 compares the input and output power, each calculated from the current and voltage values measured by the LCU, to determine the efficiency of the DC-DC converter.
Fig. 12.14 shows the measurement of the response time of the voltage control considering the networked control. The DC-DC converter is supplied with a constant voltage of 12 V and a current of 2 A during the entire test. The load is constantly set to 150 Ω. Initially, the target voltage of the DC-DC converter is set to 10 V and the current limit to 0.5 A. To measure the response time, a new target voltage of 20 V is specified via the CAN line. Fig. 12.14 shows that the DC-DC converter has regulated to the new target voltage approx. 0.12 s after the start of the transmission of the respective command via the CAN line. The solid line shows the measurements of the electronic load, and the crosses show the ones of the LCUs. It is clearly shown that the LCUs measure more frequently and more precisely and also detect short-term changes, enhancing functional safety. The measuring units of the electronic load scan the values less frequently and send previous values, which leads to partly considerable deviations between the measured values of the LCUs and the electronic load.
Furthermore, another DC-DC converter [522], a unidirectional buck converter, was tested (Fig. 12.18) under an abrupt load jump from 150 to 200 Ω (Fig. 12.16). The DC-DC converter was also adapted to the communication-based control, with output current and voltage adjustable via UART (Fig. 12.18). The input voltage of the DC-DC converter during the test was 20 V and the input current 1.5 A. The output voltage was set to 10 V and the output current to 1 A. After the load jump occurred, the voltage increased slightly with a maximum change of 0.01 V (Fig. 12.17). This voltage change barely influences the control and therefore this DC-DC converter passed the load jump test. Furthermore, only the measurement results of the LCU

were used in this test due to the high measurement interval of the electronic load and the resulting limited significance of these measurements.
The results show that the framework is capable of validating all essential functionalities of different DUTs including the control accuracy, the control stability under changing load and the response time considering the networked control. The consideration of the mentioned criteria enables an evaluation of the respective DC-DC converter regarding the reliability and the usability within the DBMS. Furthermore, the results confirm the communication, the adjustment of the LCUs' target values, the stimulation of the hardware components including the DUTs and the electronic load, and the acquisition and evaluation of the actual current and voltage values. This forms the basis for automated, comparative testing of several different DC-DC converters and for testing the communication-based power distribution among several DC-DC converters.

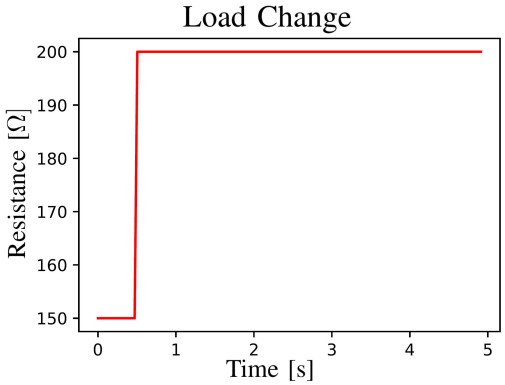


Figure 12.16: Load test with abrupt load jump

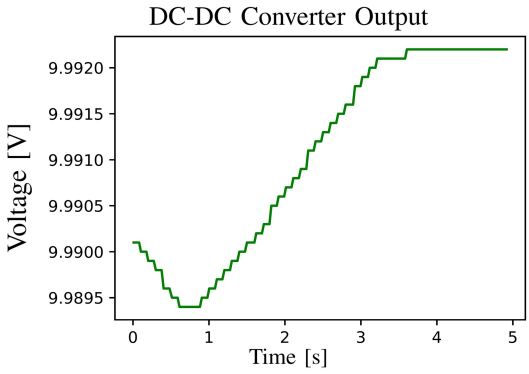


Figure 12.17: Voltage at the output of the DUT [522]

12.6 Summary

DC-DC converters form the basis for the decentralized control of the DBMS by controlling the flow and distribution of power. Therefore, a customized framework to test DC-DC converter for the DBMS was proposed, which takes into account the aspects of the communication based, digital control among the DUTs. The test framework combines software simulation and real hardware components, which are stimulated according to the simulation data. The software simulation enables the adaption to various applications by supporting a variable number of batteries, different battery technologies, adjustable electronic loads and sources. The test framework evaluates the response time, the control accuracy and the stability of the DUTs and allows to assess the reliability and usability of the DUTs within the DBMS. Initial test scenarios validated and verified the test framework, successfully proving the communication, the interaction between software and hardware as well as the acquisition and analysis of the actual data. In further tests the simultaneous testing of several and different DC-DC converters will be validated. As a future work, the test framework is extended for testing a DC-DC converter with serial interface and a bidirectional DC-DC converter [336].

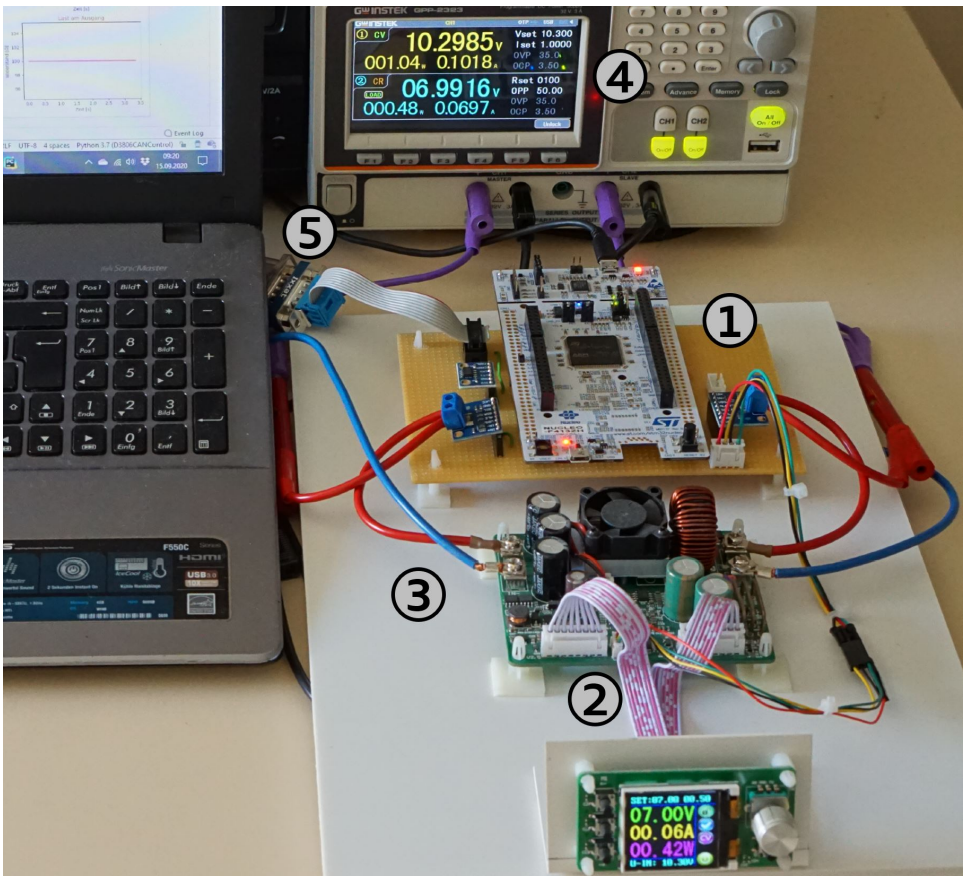


Figure 12.18: The Cortex-M7 based LCU ① is attached to the DC-DC converter [522] under test ②.

13

Hardware Implementation of the Decentralized Battery Management System

This chapter provides an overview of the hardware test setup implemented to evaluate the functionality of the control and coordination strategies. Furthermore, it serves to verify the developed models for the distributed battery management system . Implementation details of the various hardware and software modules used in the system are discussed. The hardware components consist of customized commercially available hardware that has been adapted to meet the system requirements, as well as custom designed printed circuit boards that have been implemented using commercially available components. Key hardware components include the local control unit with power electronic circuitry, explicitly the bidirectional DC-DC converter, control circuits, measurement units, and communication interfaces. In addition, a DC-DC converter which corresponds to a buck converter is used for lower input voltage loads. A display shows the current operating parameters including current, voltage, temperature as well as power flow direction and leader selection results. A load box controllable via CAN FD allows stepwise load switching. A logger collects CAN data and stores it in a database that allows analysis of bus utilization, long-term evaluation of battery usage, and load and generation forecasts. The operation and implementation details of these hardware components are discussed in more detail in this chapter. An overview of the software used in the microcontrollers is also provided. This hardware test setup serves as a test bed for functional testing and validation, as well as a proof of concept of the decentralized battery management systems proposed in this thesis.

13.1 Motivation

The proposed decentralized battery management system has significant advantages over centralized, homogeneous ones due to its ability to support heterogeneous battery types and different loads while increasing the system reliability. Nevertheless, there are special requirements for the control and coordination of the system, as well as

for the hardware and software components. The system goals include scalability, reconfigurability, flexibility, reliability, and fault tolerance, and all of them affect the implementation. To achieve these goals, control and coordination strategies have already been introduced. The following chapter describes the hardware and software implementation of the test setup of the decentralized battery management system.
Thereby, several significant considerations were made in the design of the system in order to meet the requirements. The decentralized architecture requires functional equality and independent functionality for each node. Reliability requirements demand the reduction of potential single failures in system coordination, communication, and measurement. For the proposed control strategy and for safe battery operation in a heterogeneous system load sharing based on the individual battery state, (dis)charge current limiting and regulation of the DC link voltage to the predefined setpoint is needed. For the feedback part of the control and the batter state assessment, measurement of the operating parameters such as current, voltage, and temperature are required as well as battery state determination, such as SoC and SoH. The latter two parameters are only marginally considered in the context of this thesis. In addition, the system must be able to handle heterogeneity by accommodating different batteries with a wide input voltage range on the low voltage side and variable current limits. It is also required to support different loads and generators, which demands adjustable DC link voltage levels.
The chapter focuses on describing the key components of the DBMS (Fig. 13.1). First, the components of the local control unit are described, with special attention to the DC-DC converter. The timeline and steps of the development are briefly outlined without addressing specific earlier approaches. Subsequently, the final design of the local control unit is described. It is integrated on a single PCB that contains the power and control circuits, the computation unit, the communication interfaces and the measurement modules.
Next, the display unit is presented, which provides valuable information about the power flow direction, the operating parameters (such as current, voltage, temperature), and the battery data (including SoC and SoH). It also displays the results of the leader election process.
The functionality of the load box is described. It is equipped with a CAN FD interface that enables step-by-step switching of the loads. This feature can be beneficial during the system start-up or shutdown, as it allows loads to be individually activated or deactivated. It also allows load deactivation, when the available power in the system is limited.
In addition, the CAN FD Log, a logger system, is introduced. It logs CAN FD messages on the bus and stores them in a database. The CAN FD log provides system information in real time via a web interface. Furthermore, it allows long-term evaluations of the data. These evaluations are valuable for load and generation forecasts. The battery operation data can be used in the future to gain a better understanding of battery degradation. This can also serve as a basis for deriving optimization strategies for battery degradation aware load current distribution in heterogeneous battery systems.

13.2 Local Control Unit

The local control unit is an essential part of the system and includes a DC-DC converter that enables the power flow in charge and discharge direction. In addition,

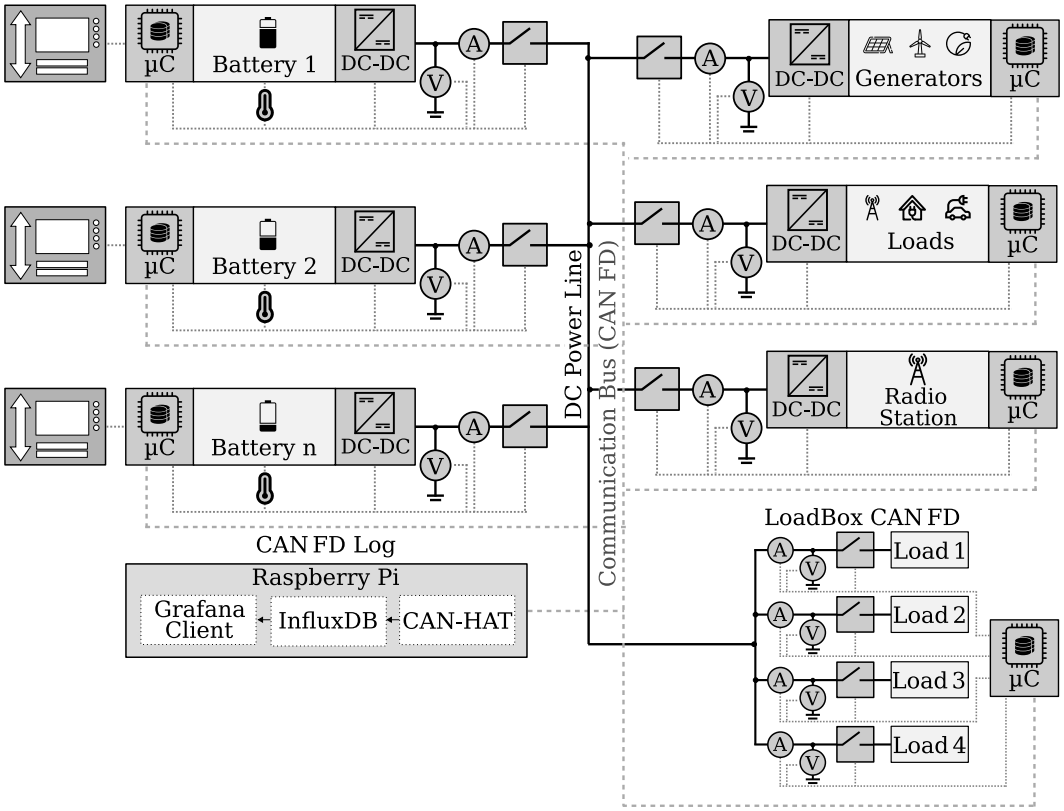


Figure 13.1: Overview of all hardware components of the decentralized battery management system.

it contains a microcontroller with local and global communication interfaces as well as sensors for measuring the actual operating parameters such as current, voltage, temperature and SoC. Furthermore, an emergency shutdown is integrated, which deactivates the unit in the event of a fault or in response to corresponding instructions, for example from the microcontroller.

One of the main tasks of the local control unit is the acquisition of the operating parameters. It records and monitors the actual operating parameters, which include the measurements of current, voltage, temperature and the determination of the SoC. Furthermore, the local control unit is responsible for communicating data relevant to the system control. These are sent to all remaining nodes via the global broadcast-based communication line. Moreover, the local control unit manages the received data relevant for the control. It collects the measurement values catergorized by node ID and uses this information for the control and leader election algorithms.

The local control unit is also responsible for the control to the setpoints. It uses the measured voltage and current and together with the received distribution factor and compensates for the control deviation in the case of communication-based control. It also communicates regularly the actual derating factor to the temporary leader. In the case of droop-based control, the instantaneous value of the voltage is also measured. Together with the stored droop resistor, it provides the reference voltage for the output current control. The local control unit is in charge for adjusting the droop resistance in dependence of the battery state.

13.2.1 Adaptation and Development of Different DC-DC Converters for the Decentralized Battery Management

The DC-DC converters are a crucial in order to fulfill the aforementioned tasks. They interconnect components of different output voltage levels and are required for providing a predefined voltage at the DC power line. They are connected in parallel and the proposed control strategies provide a balanced load distribution without overloading a single DC-DC converter. For the battery state-aware control, bidirectional DC-DC converters with current limits, that are adjustable via microcontroller interfaces during active operation, are required. The adjustable current limit is set to a range between $0A$ and $10A$ initial. The analog control allows a current maximum of $13.3A$ and the digital one of $40A$. The current limits are individually adjustable according to local battery state detection and setpoint specifications. This is necessary for safe battery operation on the one hand, and on the other hand allows charge state balancing without the need for additional recharging operations.
To combine various batteries with different terminal voltages, the DC-DC converters have to support a variable input voltage range. Voltage fluctuations on the input side, e.g., due to SoC-dependent terminal voltages, should not affect the output voltage. The input voltage range of the DC-DC converter is set between $0V$ up to $15V$ according to the common terminal voltage of batteries. The output voltage of the DC-DC converters is initially set to $24V$.
DC-DC converters with current limits that can be changed during active operation and the above described features are not available for purchase. Therefore, various DC-DC converters were adapted and their circuitry was extended in order to meet the requirements of the DBMS (Fig. 13.2, Tab. 13.1).

Table 13.1: Overview of different DC-DC converters, which have been adapted to the requirements of the DBMS [388, 520, 523, 524].

DC-DC Converter Type		Control Interface	Powerflow
D3806	Buck & Boost Converter	2·PWM	unidirectional [520]
LM5170	Buck & Boost Converter	I^2C, DAC	bidirectional [388]
DPS5015	Buck Converter	UART	unidirectional [523]
LM3150	Buck Converter	DAC	unidirectional [524]

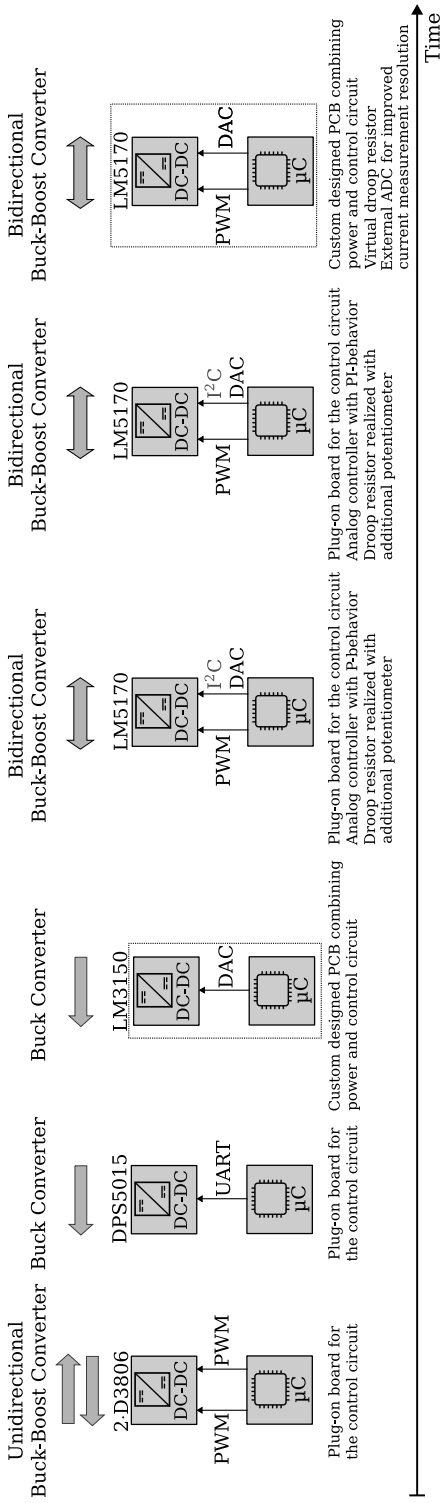


Figure 13.2: Development over time and overview of the different DC-DC converter types which can be used in the DBMS

D3806: Unidirectional DC-DC Converter Combining Buck and Boost

The DC-DC converter D3806 [520] is a unidirectional DC-DC converter and combines a buck and a boost converter (Tab. 13.2). It allows both higher and lower output voltages compared to the input voltage. Since only unidirectional power flow is provided, two converter units are required to charge and discharge the batteries. The D3806 provides adjustable current and voltage limits, whereby both are set via

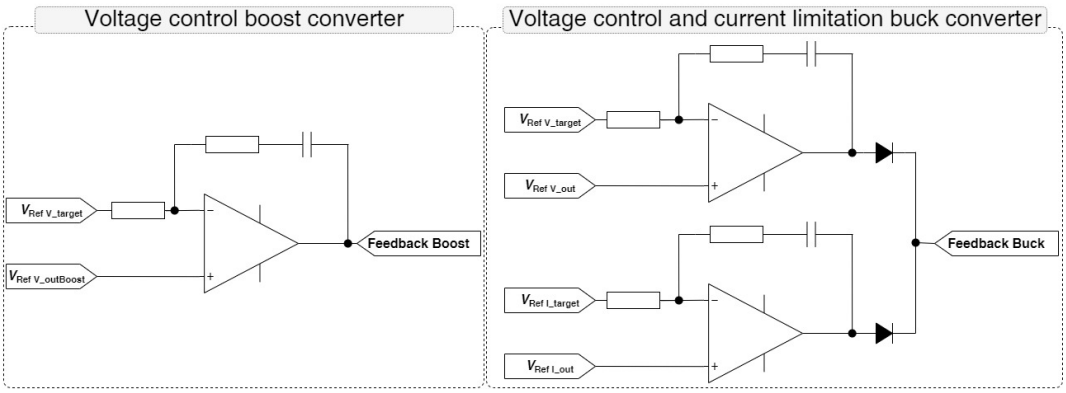


Figure 13.3: The voltage and current values are specified via PWM signals. The voltage control is two-stage while the current limitation is part of the feedback line of the buck converter.

pulse-width modulated signals. The commercial version of the D3806 consists of two boards: the power board and a plug-on board for setting the output power via push buttons. The push button setting did not meet the analyzed requirements and

Table 13.2: Electronic features of the DC-DC converter D3806 [520].

Input voltage	10 V - 40 V
Output voltage	0 V - 38 V
Output current	0 A - 6 A
Conversion efficiency	up to 92 %
Output ripple	under 50 mV
Operating temperature	-40 °C to +85 °C
Switching frequency	150 kHz
Short circuit protection	constant current
Voltage control resolution	0.01 V
Current control resolution	0.001 A

is therefore replaced by a microcontroller board, which directly generates the pulse width modulated signals to set the output power according to the specifications of the temporary leader.

DPS5015: Buck Converter for Load Side

The programmable DC-DC converter DPS5015 is a buck converter with adjustable output voltage values and output current limits [524]. This buck converter is used for the step wise switching of a load or a generator providing an output voltage higher than the DC link voltage.

In the commercially available version of the DPS5015, the target values for the output voltage and current are set via the encoder of an additional control unit. To meet the requirements of the DBMS, this plug on control unit is replaced by an own microcontroller board. The target values are specified via the UART interface in the format of the Modbus RTU protocol [525].
Fig. 13.4 shows the structure of the Modbus RTU protocol. The address code allows the control of several DC-DC converters from one microcontroller. For this purpose, different addresses for the individual DC-DC converters are defined via the control unit. The function code determines whether read or write access to a single register or to multiple registers is enabled. The data area contains the commands for setting the DC-DC converter or for reading out the measured values. For this, first the register address is specified followed by the required set point. For the voltage setting, e.g., the register address is 0000H.
In addition, it is possible to transmit the commands via Bluetooth. A separate library was developed for the control via UART, which includes functions to select the control commands, to generate the data area and to calculate the CRC code. First tests validate the function of the adapted DC-DC converter.

Figure 13.4: Structure of the Modbus RTU protocol for controlling the DC-DC converter DPS5015 [525].

Table 13.3: Electronic features of the DC-DC converter DPS5015 [524].

Input voltage	6 V - 60 V
Output voltage	0 V - 50 V
Output current	0 A - 15 A

LM3150: Buck Converter for Load Side The DC-DC Converter TI LM3150 is a pure step-down converter for supplying consumers, in this special case for supplying an amateur radio station (Tab. 13.4). For stepped load switching, adjustable output voltage levels in the range between 12 V and 14 V are required.
For the voltage control of the LM3150, the output voltage is divided by a voltage divider and compared with the reference voltage at the feedback pin. As the DC-DC converter has to provide a variable output voltage, this principle has to be adapted. In order to generate a variable output voltage, the feedback loop is adapted. For this purpose, an analog output pin of the microcontroller is used. Figure 13.5 shows the

Table 13.4: Electronic features of the DC-DC converter LM3150 [523]

Input voltage	18 V - 24 V
Output voltage	12 V - 14 V
Output current	0 A - 10 A
Switching frequency	200 kHz up to 1 MHz

circuit for adjusting the feedback voltage. Two methods are available, which can be

changed by switching the jumper. Method 1, open jumper, does not require a constant voltage from the microcontroller. With an open jumper, the output voltage V_{output} is divided across the voltage divider to V_{FB} (Equ. 13.1). If the jumper is closed, the feedback voltage V_{FB} can be increased via the analog voltage $V_{\text{STM}_{\text{analog}}}$ and thus V_{output} can be decreased. This also changes the resistance ratio, which increases the maximum output voltage (Equ. 13.2).

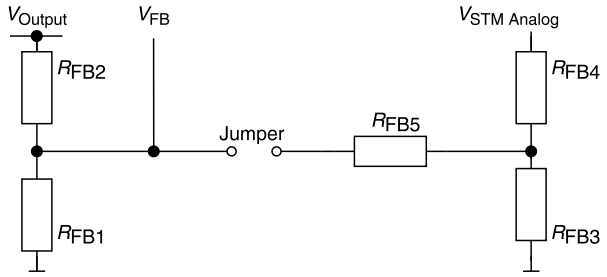


Figure 13.5: Customized feedback loop for adjustable output voltages.

$$V_{\text{FB}} = V_{\text{output}} \cdot \frac{R_{\text{FB1}}}{R_{\text{FB1}} + R_{\text{FB2}}} \tag{13.1}$$

$$V_{\text{FB}} = V_{\text{output}} \cdot \frac{R_{(\text{R}_{\text{FB3}}+\text{R}_{\text{FB5}})||\text{R}_{\text{FB1}}}}{R_{\text{FB2}} + R_{(R_{\text{FB3}}+R_{\text{FB5}})||R_{\text{FB1}}}} + V_{\text{STM}_{\text{analog}}} \cdot \frac{R_{(R_{\text{FB1}}+R_{\text{FB5}})||R_{\text{FB3}}}}{R_{\text{FB3}} + R_{(R_{\text{FB1}}+R_{\text{FB5}})||R_{\text{FB3}}}} \cdot \frac{R_{\text{FB1}}}{R_{\text{FB1}} + R_{\text{FB5}}} \tag{13.2}$$

Using method 2, the maximum possible output voltage is provided, if there is no signal from the microcontroller. If the jumper is inserted, the maximum output voltage without microcontroller signal is changed. To change the voltage, for example to the nominal operating voltage of 13.8 V for the considered amateur radio system, a constant voltage of the microcontroller at the DAC pin is necessary. The hardware

Table 13.5: Ratio between microcontroller voltage and output voltage

V_{out} in V	$V_{\mu\text{C}}$ in V
12	3
13.8	1.2
15	0

implementation was successfully implemented and showed the desired behavior of the customized feedback loop (Tab. 13.5). Adaptation of the feedback loop via the DAC of the microcontroller allows fine adjustment of the voltage in the range of 12 V – 14 V and in the usual operating range the converter efficiency is over 93%.

Bidirectional DC-DC Converter with the Current Controller LM5170

The LM5170 chip [388] is a current controller for non-isolated bidirectional DC-DC converters with half-bridge topology and it can directly drive two power stages. For

first tests the commercially available evaluation board [335] is. It is a bidirectional DC-DC converter based on two phase-shifted half-bridges with a fixed value, hardware based voltage control. The setpoint of the voltage at the low voltage port equals to 14.5 V and the setpoint voltage at the high voltage port is 50.5 V.

Table 13.6: Electronic features of the bidirectional DC-DC converter based on the chip LM5170 [335].

Voltage LV-port	3 V - 48 V
Voltage HV-port	6 V - 75 V
Maximum current LV-port	60 A
Switching frequency	50-500 kHz

The basic configuration allows to flow a current of 40 A at the LV port. It can be switched between buck and boost mode.
The given voltage and current specifications do not meet the requirements and therefore several own control boards with droop parameterization including virtual droop resistances are implemented. The control boards provide an analog circuit for the realization of the droop control. They also include the required sensors and a microcontroller. To set the parameters, the microcontroller provides the analog reference voltage via a DAC.
In a first approach, the droop resistor was realized by a potentiometer. The resistance value of the potentiometer is adjustable via an I^2C interface. So the value of the droop resistance can be adjusted via the microcontroller during active operation.
Using this approach, there are two implementations of the add on control board. One implements an analog P-controller and the other an analog PI-controller. In the final design, the ohmic droop resistor is replaced by a virtual one. This allows the droop resistor to be changed flexibly in software. The stepwise value setting of the potentiometer no longer has to be taken into account, and in addition, the power loss that occurred over the real resistor is eliminated.
With these first implementations the current controller LM5170 and the droop control could be tested successfully and proved to be suitable for the DBMS. The final version of the local control unit includes a bidirectional DC-DC converter with the LM5170 current controller and the droop control using the virtual droop resistor.

13.2.2 Local Control Unit with Bidirectional DC-DC Converter

The final version of the local control unit was realized on a single custom-made PCB with commercially available components (Fig. 13.6). The PCB includes a bidirectional, multiphase DC-DC converter with analog and digital control. The control of the DC-DC converter corresponds to an average current mode control with an outer voltage control loop, whereby the current control is integrated in the IC LM5170. In addition, the local control unit includes a microcontroller with communication interfaces and an external ADC for improved resolution of the measured values.

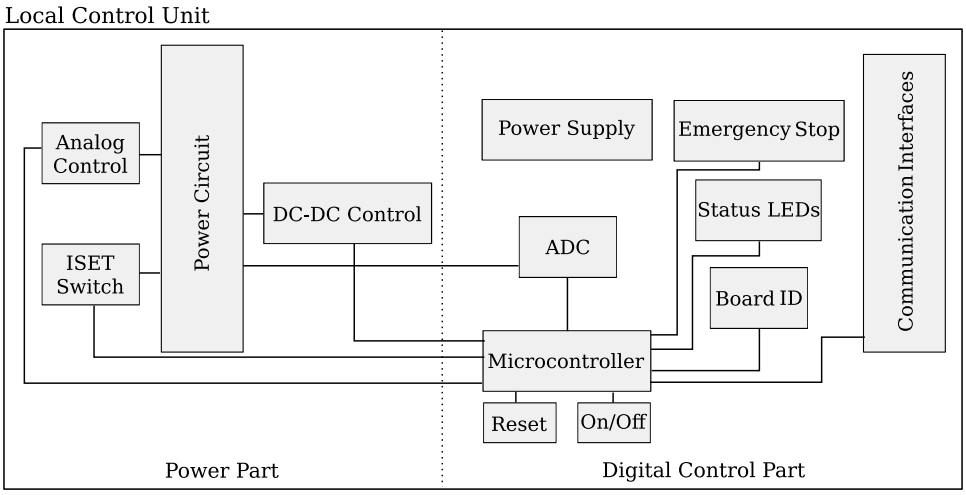


Figure 13.6: The final version of the local control unit is realized as a single PCB combining the power and control circuits. It includes a multiphase, bidirectional DC-DC converter with controller and corresponding sensor modules. Furthermore, a microcontroller with corresponding communication interfaces and an external ADC are integrated on the board.

13.2.2.1 Power Circuit of the Bidirectional DC-DC Converter

The power circuit of the DC-DC converter consists of two half-bridges connected in parallel, which are driven by a 180 degree phase shifted switching signal (Fig. 13.7). Each of the two half bridges regulates to the half of the required set current.
The current is measured by both a shunt resistor and a current sensor (Fig. 13.7, Fig. 13.8, Fig. 13.11). The voltage that drops across the shunt resistor is part of the feedback path for the current control of the DC-DC converter and serves as the input signal to the LM5170 current controller (Fig. 13.10). The shunt voltage is compared with the output reference voltage of the voltage controller and the switching signals of the MOSFETs are adjusted according to the remaining control deviation (Fig.8.7, p. 143).

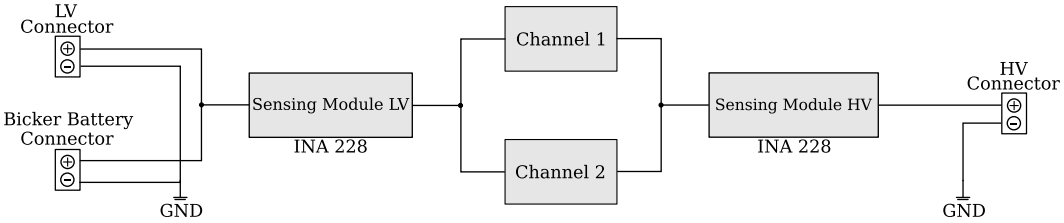


Figure 13.7: The power circuit of the bidirectional DC-DC converter consists of two parallel connected channels with measuring units on the low and high voltage side.

The current controller module enables both analog and digital control (Fig 7.2 on p. 111). Analog control is characterized by higher control dynamics and less computing effort. At the same time, it is only designed for one operating point. Adjustment to other operating points requires an adaption of the electrical components. The digital control makes it possible to adjust the controller type and the controller parameters in active operation. Different controller parameters corresponding to different load operating points can be stored and high control accuracy and dynamics can be achieved over a wide load range. The disadvantages of digital control are the increased computing effort, the lower speed and the quantization errors. Both types

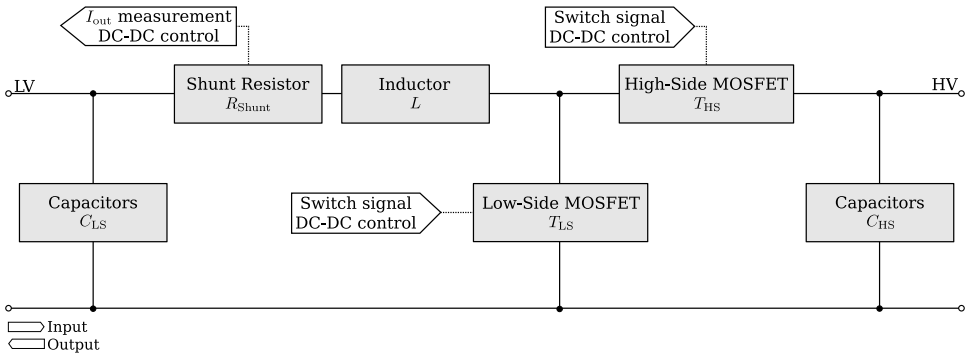


Figure 13.8: Each channel of the power circuit corresponds to a half bridge. The MOSFETs are controlled by the DC-DC converter controller (Fig. 13.10). For the feedback control the instantaneous value of the current is given by a shunt based measurement.

of control are used within the DBMS and active switching between them is required during active operation. Two analog switches (Tab. 13.7) are used for the switching process (Fig. 13.9).

Table 13.7: Function table for the analog switch of the ISET switch circuit [526].

$\overline{EN}$	IN	NC TO COM	NO TO COM
low	low	on	off
low	high	off	on
high	–	off	off

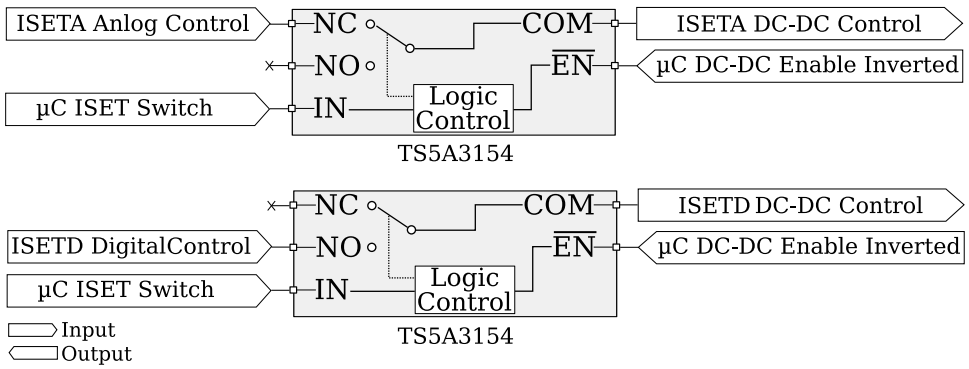


Figure 13.9: Two analog switches are used for switching between analog and digital control. According to the specification of the microcontroller, the ISETA for the analog control or the ISETD for the digital control is passed through to the controller. [526]

The current controller IC LM 5170 realizes the average current mode control for the control of the DC-DC converter output current (Fig. 13.10). The key functionalities of the current controller for the DBMS are described below, whereby details are presented in [500]. The functional diagrams of the current controller are shown in the figures 8.10 and 8.11. The functionality of the pins is described subsequently, starting from the top left one to the bottom right pin in figure 13.10.
The master enable pin is for (de)activating the current controller and is connected to the emergency stop. If this pin is low, the output current is equal to $0A$ and the DC-DC converter is inactive and can be disconnected. This pin is connected to an

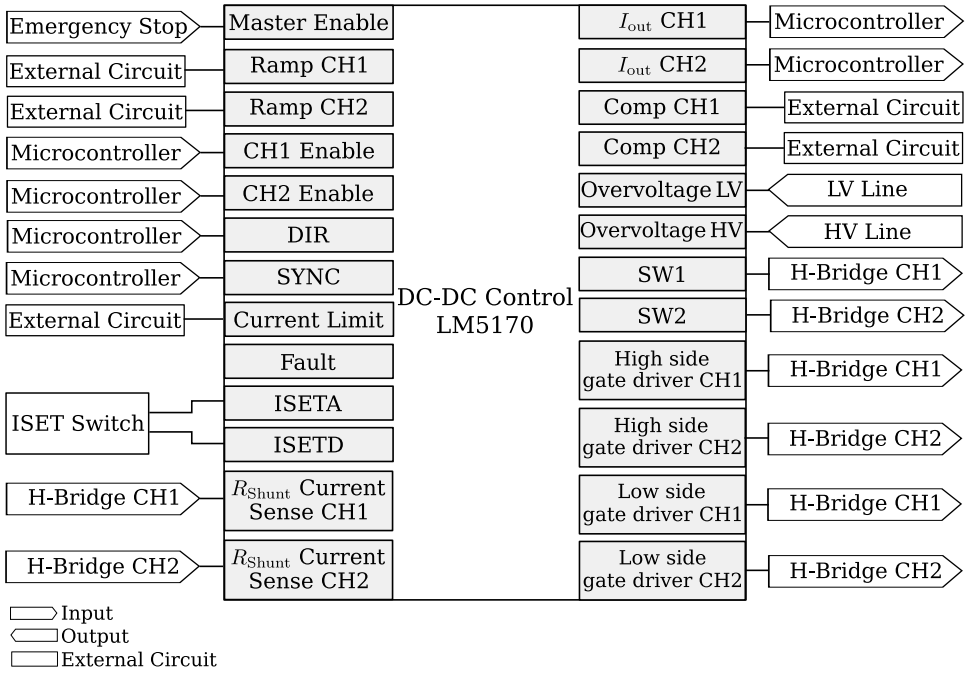


Figure 13.10: DC-DC Control with LM5170

emergency stop switch and the microcontroller and consequently the controller can be deactivated by pressing the switch or corresponding microcontroller signals.
The determination of the sawtooth signals for the internal comparison (Fig. 8.4 on p.141) is done via the corresponding external circuit (Fig 8.12 on p. 153). Details about the component dimensioning are documented in [500]. The two channels can be activated separately via the corresponding enable pins. In principle, it is also possible to use only one of the channels. In this case, a factor of two must be taken into account for the setpoint of the current control. The power flow direction and thus also the operating mode, i.e. whether buck or boost mode is used, is specified via the direction pin. An external clock can be specified via the synchronization pin. This enables external clock synchronization when using several DC-DC converters connected in parallel. To realize the limitation of the induction peak current value, a pin of the current controller is connected to a single external resistor. An internal $25\,\mu A$ current source creates a voltage drop across the resistor. This voltage is then internally compared to the voltage across the measurement shunt. If the voltage at the pin is greater than $4.5\,V$, either because of a very large resistor value, the pin is unconnected, or for some other reason, an internal monitoring shuts down the circuit. This prevents the LM5170 from operating with an erroneous peak current limit.
The fault pin corresponds to a fault flag. If a MOSFET drain source short circuit fault is detected before startup, this pin is pulled to low internally to signal the short circuit fault. The LM5170 remains in a disabled state. The pin can also be pulled low externally, in this case via the microcontroller, to disable the LM5170 and serve as a forced shutdown. During forced shutdown, all gate drivers are switched off.
The ISET pins are used to set the inductor DC current level. When using the ISETA pin, an analog reference voltage proportional to the required inductor current is used. In case of ISETD the inductor current is determined by the duty cycle of a PWM signal. Either ISETA or ISETD may be used for the current value specification. Since both variants are used in the DBMS, an additional circuit (Fig. 13.9) ensures that only one of the pins is used actively.

For current measurement, two differential current measurement input pins are used for each of the two channels. The current sense resistor is located between the two inputs (Fig. 13.8). For current control, it is necessary to feed back the actual value of the inductor current and compare it with the actual setpoint specifications. Thereby the shunt resistor forms the feedback part. The comparison with the setpoint specification is performed by a corresponding internal comparator circuit.
Additionally it is required to have knowledge about the actual output currents for the load distribution control. For this purpose, the inductor current monitoring pins of the LM5170 are used. There is a monitoring pin for each of the two channels. A current proportional to the channel inductor current flows out of this pin. Both pins are connected to a terminating resistor and a filter capacitor. Consequently, a voltage proportional to the current inductor current drops across the resistor which is further processed in the microcontroller. An internal $25\,\mu A$ offset DC current source at the two PINs boosts the active signals above the ground noise, improving the noise immunity.
The two channels have an independent error amplifier. The output of the error amplifier is internally connected to the COMP pin. Externally this pin is connected to a compensation network consisting of two capacitors (C_{COMP}, C_{HF}) and a resistor (R_{COMP}). The control loop of the LM5170 is the inner current loop of the bidirectional DC-DC converter, whose outer voltage loop is controlled by either the microcontroller or the analog circuit (Fig. 9.10, p. 184). By applying the averaged current control method, the inner loop is basically a first-order system. A compensation network consisting of a resistor and two capacitors is therefore sufficient to stabilize the inner current loop.
The LM5170 provides an overvoltage protection function for both the HV- and the LV-port. For monitoring the voltage, a comparator with an internal $1\,M\Omega$ pull up resistor and an external pull down resistor is used. When the voltage at the OVP pin exceeds the threshold of $1.185\,V$, the low and high side gate drivers are disabled. At the same time, the capacitor that provides the time base for the soft start is discharged in preparation for a restart. When the overvoltage alarm is cleared, the restart process begins. The high side voltage monitoring is used in boost mode and the low side voltage monitoring is relevant in buck mode.
Each channel provides a $5A$ half-bridge driver for driving external n-channel power MOSFETs. The low-side driver is directly powered by the supply voltage and the high-side driver by a bootstrap capacitor. During the low-side driver on-time, the swichting node (SW) pin is pulled down to ground and the bootstrap capacitor is charged by the supply voltage through the boot diode.
During startup in buck mode, the bootstrap capacitor is initially not charged. The LM5170 then holds the high-side driver outputs and sends pulses to precharge the capacitor. When the boot voltage is greater than the $6V$ threshold, the high-side drivers output PWM signals on the respective pins for normal switching operations. During startup in boost mode, the capacitor is charged by the normal turn-on of the low-side MOSFET.
To prevent shoot-through between the high-side and low-side power MOSFETs on the same half-bridge leg, the built-in adaptive dead time is used.
This dead time is realized by real-time monitoring of the output of one driver (either high side gate driver (HO) or low side gate driver (LO)) by the other driver (LO or HO) of the same half-bridge switching leg. Only when the output voltage of the one driver drops below $1.25\,V$, the other driver turns on.

13.2.2.2 Sensing Module

For current, voltage control and the load distribution control, the measurement of the DC-DC converter output current, of the voltage at the high and low voltage side as well as the measurement of the total current on the DC line are required.
The bidirectional current controller LM5170 already provides the measurement of the inductor current of the two channels via shunt resistors. In addition, two sensor modules based on the INA228 IC [527] are integrated at the LV- and HV-side of the power circuit (Fig. 13.7). In addition to current, voltage and power determination, these modules also enable the acquisition of charge, energy and temperature (Fig. 13.11). The additional measured values are required for the battery state estimation.

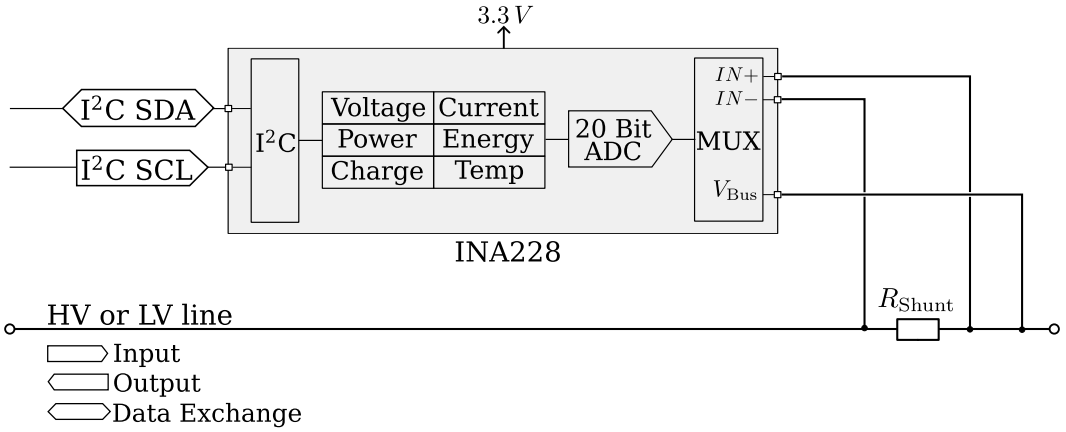


Figure 13.11: Additional sensing modules based on the IC INA228 [527] are inserted at the HV and LV side. In addition to current, voltage and power, energy, charge and temperature are also recorded. The analog values are converted with a 20 bit delta sigma ADC. Furthermore, the sensing module has an I^2C interface which is connected to the microcontroller.

For more accurate battery state estimation, additional sensors and more sophisticated state determination approaches are recommended, especially for temperature sensing as well as for SoH, SoC and internal resistance determination. The temperature measurement of the IC INA228 is suitable for recording the ambient temperature of the system. Additional temperature sensors are useful for recording the battery temperature, for example near the electrode and additionally inside the cell.
The sensor module is connected to the microcontroller via an I^2C interface. It is not mainly used for current and voltage control due to the latency created over the communication interface, but it is useful to detect defective current and voltage sensing and to perform additional measurements. It is also suitable for collecting operation data as a basis für determining the SoC and the SoH, for example using the Coulomb counting method. Furthermore, the sensing module can be connected to the display unit.
The feedback path of the internal current control corresponds to the two shunt resistors of the channels, which are directly connected to the LM5170. For voltage measurement, the HV and LV voltages are stepped down via corresponding voltage dividers (Fig. 13.12).
The output of the voltage dividers is connected to the analog inputs of the microcontroller. The conversion of the analog reference voltage takes place with a frequency of $115.2\,kHz$.

An external 12 Bit ADC is used for improved resolution, especially for the current measurement values. The actual current value is required for the digital load distribution control. In this case, the real-achievable resolution of the ADCs installed internally in the microcontroller is not sufficient. The reason for the insufficient resolution of the current value are problems with the ADC unit of the used microcontroller [528]. Therefore an external ADC is used for the acquisition of the output current value. The ADC120 is a 12 bit ADC with the conversion method of successive approximation [529]. An SPI interface connects the ADC to the microcontroller, with a maximum conversion rate of 1 MBps. The ADC120 is operated with the maximum frequency of $10\,kHz$. This is sufficient for the outermost control loop, the load distribution control loop.

13.2.2.3 Computation Module

A microcontroller based on the ARM Cortex-M4 [530] is used to evaluate and manage the operating parameters, coordinate the system and perform the necessary calculations. Figure 13.15 shows the main input and output signals of the microcontroller. At the beginning, the DC-DC converter and its two channels are activated by corresponding GPIO signals. Furthermore, the own board ID, which is defined by a dual in-line package (DIP) switch in hardware, is read via the I^2C interface. For current and voltage control, the measured actual values are processed first. Both the internal ADCs and an external one that can be controlled via SPI are used for this. Depending on the operating mode, the instantaneous values are either compared with the specifications of the temporary leader (communication-based control) or a new reference voltage is calculated (droop-based control). Subsequently, when using analog hardware-based control, the ISET switch is driven accordingly, and the corresponding reference voltage for the subsequent operational amplifier circuit is generated by the DAC. With digital control, a pulse-width modulated signal is generated where the duty cycle is proportional to the required output current. Furthermore, based on the specifications of the leader or the measurement of the DC line current, the direction and thus the mode (buck or boost) is determined.

13.2.2.4 Communication Interfaces

The control and readout of sensors, the coordination of system tasks and the maintenance of system-wide data consistency require appropriate communication interfaces (Fig. 13.15 and Fig. 13.16).
At the local communication level, the communication connections are on a single LCU board. The board ID which is implemented via a corresponding DIP switch

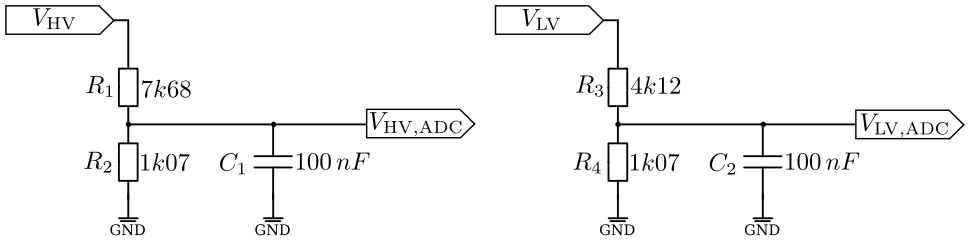


Figure 13.12: The voltages on the HV and LV side are adjusted via appropriate voltage dividers and connected to the analog inputs of the microcontroller. They are necessary for the digital control.

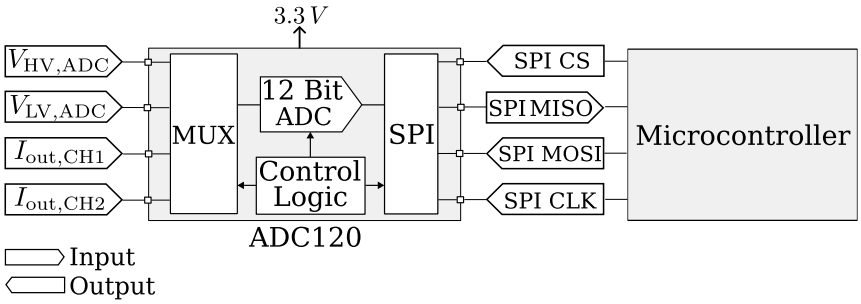


Figure 13.13: The external ADC120 is mainly used for improved resolution of the current measurement values. Internally, the conversion method sukszessive approximation is used. Via an SPI interface, conversions are triggered and digital values are sent to the microcontroller [529].

is read out via an I^2C interface. The two sensing modules are also connected to the microcontroller via an I^2C interface. Control and data exchange with the external ADC is realized via SPI. To display the instantaneous values and the status of the leader election, the microcontroller sends corresponding data via UART to a display unit.
Global communication refers to data exchange between multiple LCUs. The main communication technology for this is the broadcast-based bus communication CAN FD (Chapter 6). In order to further improve communication failure rates and thus system reliability [531], a second CAN FD line is considered in the DBMS, which is not implemented in hardware at the moment.
In addition to this, a point-to-point connection via UART between the boards is provided. The connection with the left and right neighboring board enables communication via a daisy chain structure and also ensures system-wide data consistency. It should be noted, that a higher number of messages and therefore more time are required due to this architecture. Parallel and simultaneous data exchange between several boards can be realized with the help of the additional UART communication. Furthermore the UART communication allows the localization of the boards within the network and localization of errors, e.g. an interruption of the CAN FD lines.
Figure 13.17 shows the unassembled board of the LCU integrating the presented functionalities (Fig. 13.6).

13.3 Load box: Stepwise Load Switching via CAN Communication Interface

During startup and shutdown of the system, it is beneficial to have controllable loads available. This allows the DC line voltage to be set to the desired setpoint quicker and more efficiently. Furthermore, it is helpful to activate or deactivate loads according to the total available energy. The load box allows loads to be switched on and off step by step.
The load box is controlled via CAN FD and thus enables loads to be switched on and off using corresponding CAN FD messages. It also enables measurement of the total current on the DC line. The load box integrates a microcontroller with CAN FD and I^2C interface, four relays and sensor modules to measure voltage, current and power (Fig. 13.18). Furthermore, the loadbox has a real time clock with external

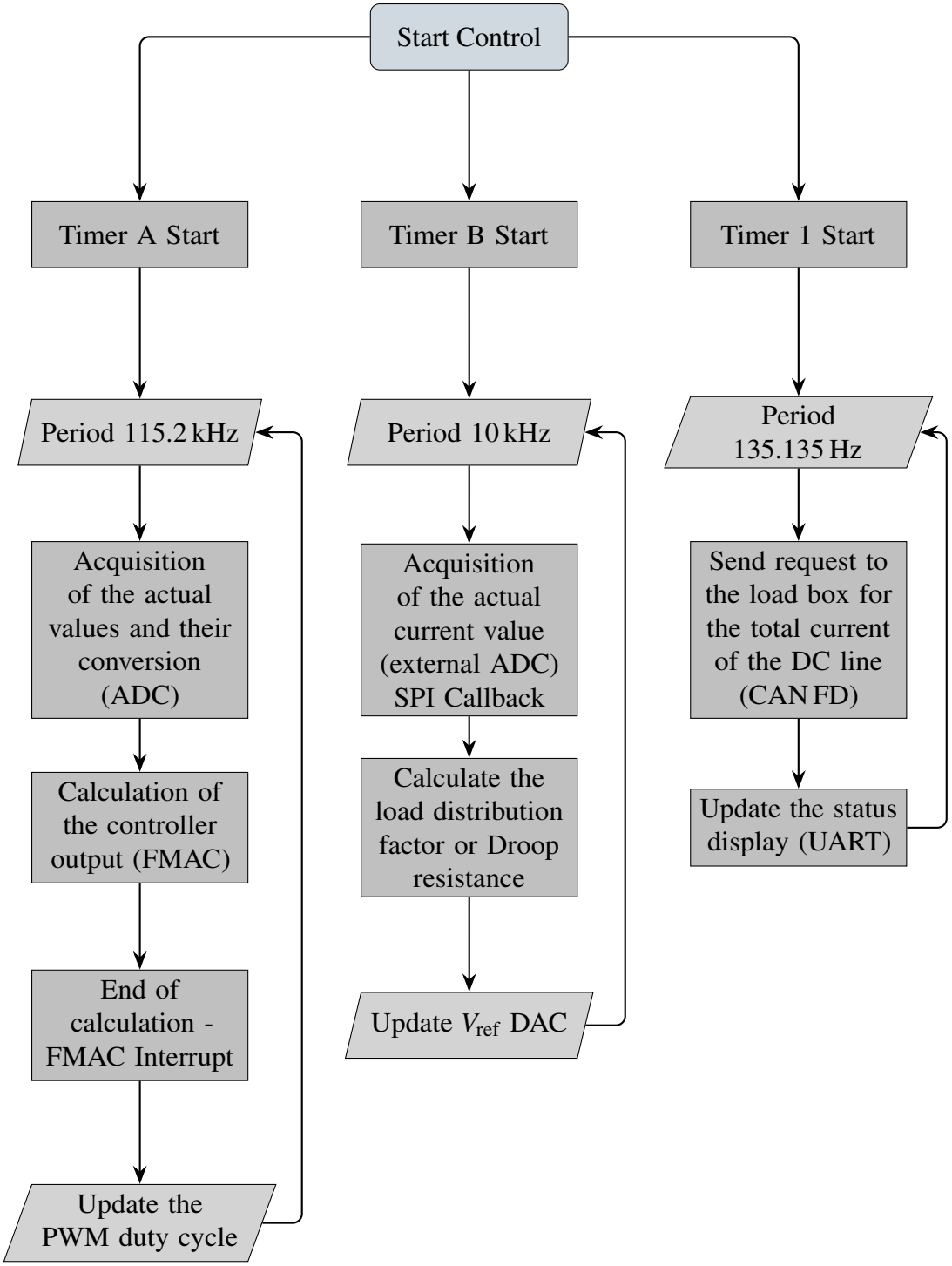


Figure 13.14: Overview of the timers relevant for the control and their frequency. Timers A and B are high resolution timers.

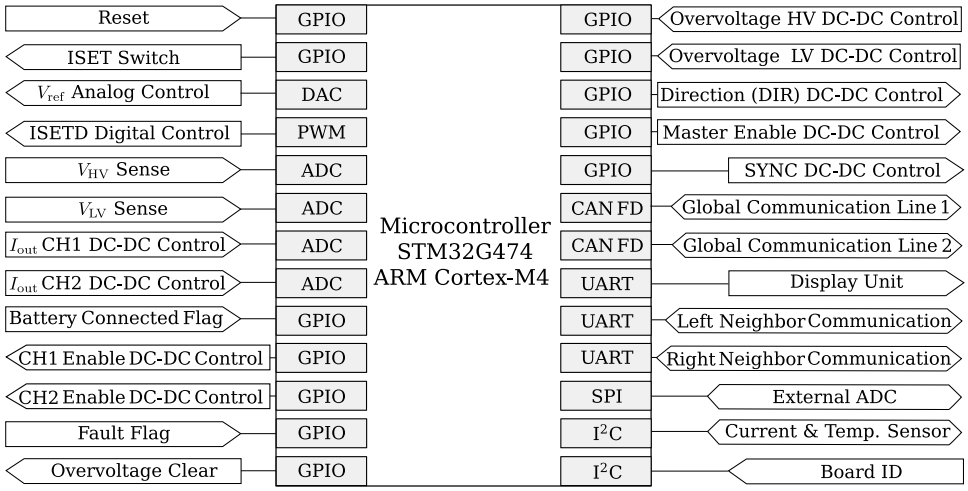


Figure 13.15: Overview of the main input and output signals of the microcontroller and part of the peripheral units used. [530]

energy supply via a battery. The sent messages, in particular the measured values, are time-stamped and enable future long-term data evaluations.
A real time operating system with the tasks `system control`, `RTC data`, `INA data` and `CAN FD` runs on the microcontroller to process the received CAN FD messages, to execute the required operations and to collect the data (Fig. 13.19). The main functions thereby include:

- the sending of an error message if too high current occurs,
- the response to load box status requests in the form of a CAN FD message, which contains the load box ID, the states of the individual relays and a timestamp,
- the switching of the individual relays according to the request specified in the corresponding CAN FD message, and
- the sending of the current, voltage and power measurement on request.

13.4 Display Unit for Current Operating Parameters and the State of the Leader Election

A separate display unit is used to visualize the current operating parameters and the status of the leader election (Fig. 13.20). The display shows the measured voltage at the LV and HV side, the (dis)charge current, the total current on the DC line,

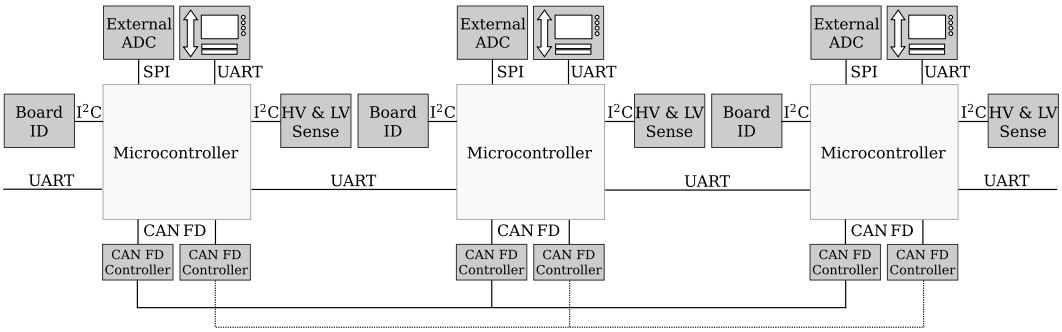


Figure 13.16: Local and global communication interfaces.

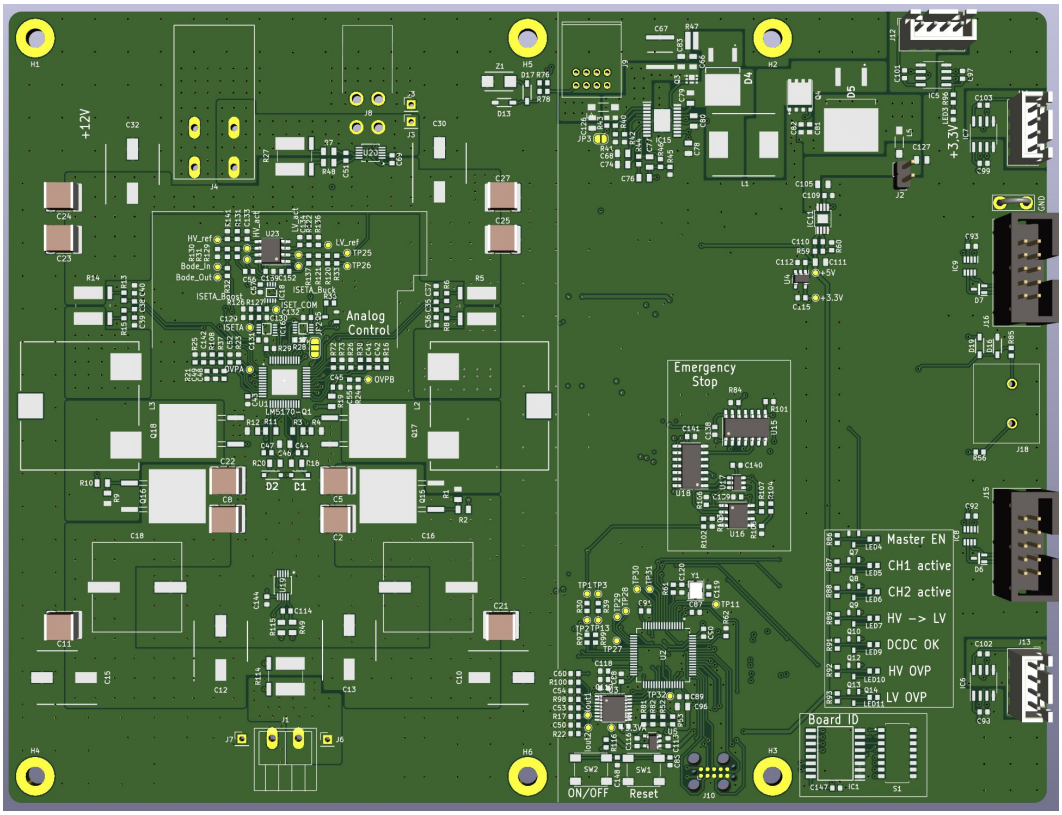


Figure 13.17: Unassembled PCB (20 cm x 15 cm) of the LCU. Figure 13.6 shows an abstracted overview of the LCU.

battery state information such as SoC and SoH and actual generator and load data. Furthermore, an arrow consisting of LEDs indicates the current power flow direction in the form of a running light in the corresponding direction. Below the display there are two LED bars to indicate the SoC and the SoH. Depending on the value of the SoC and SoH, all ten LEDs light up (at 100%) or only a part of them. The color of the LEDs also changes depending on the state. A battery state that is safe and optimal for operation is indicated with green light, a battery state that is still permissible for operation is indicated with orange light, and red LEDs indicate invalid value ranges. In addition, LEDs indicate the current state of the leader election. A node can be leader, assistant, co-assistant or actuator. The role of the node is indicated by a corresponding status LED.

13.5 Data Logger for Long-term Evaluation

For long term data analysis a data logger, which stores all messages on the global CAN FD communication line, is added to the DBMS. The control strategies try to realize an optimized battery operation. In order to be able to make statements in the future about whether the control strategies have a positive effect on battery degradation, it is necessary to track the operating parameters during operation over a longer period of use. Furthermore, the data can be used for load and generation forecasts and for battery usage profiles.
For the implementation of the CAN data logger a Rasperberry Pi is used together with a CAN FD shield. The data received via the CAN FD are stored according to

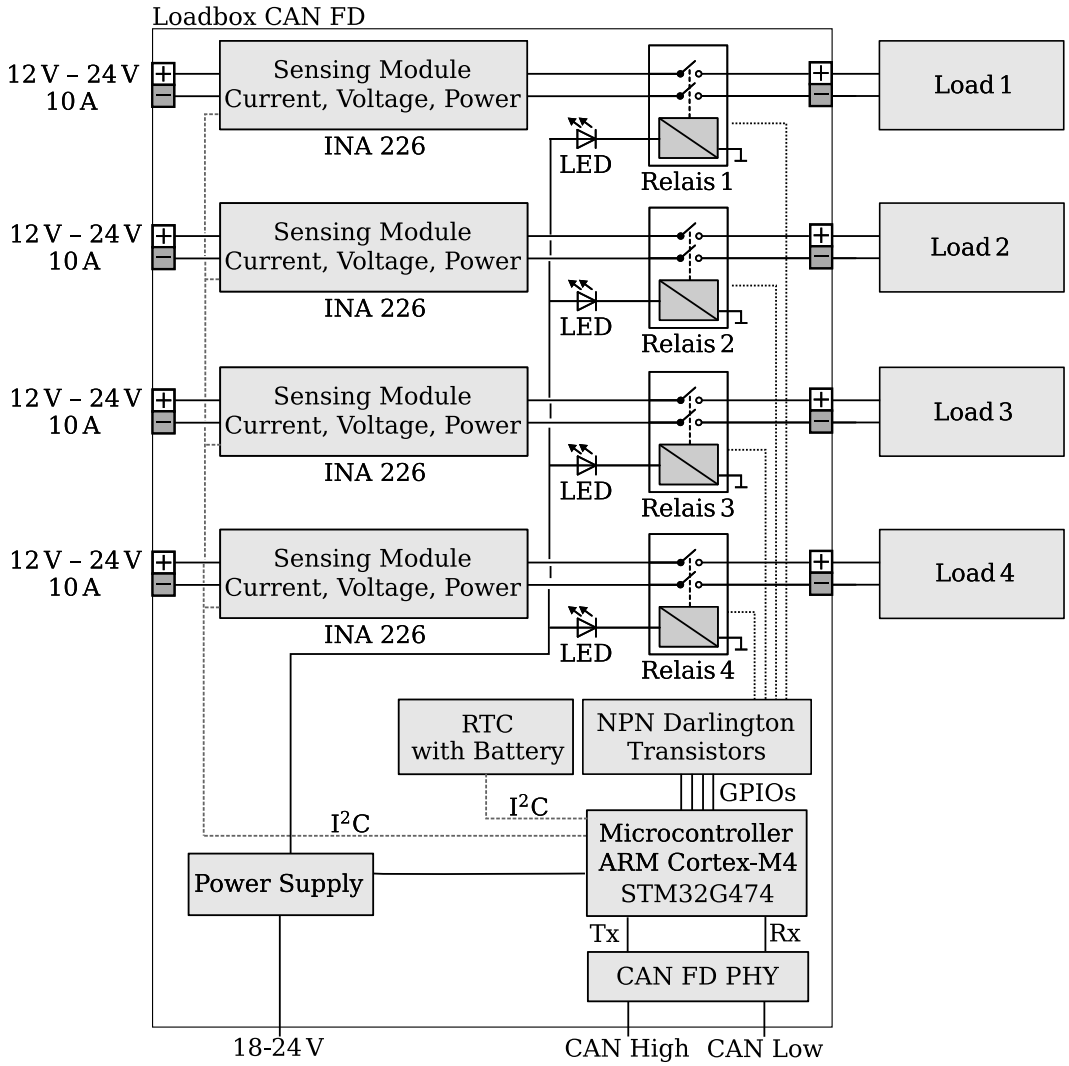


Figure 13.18: Block diagram of the load box CAN FD: The load box consists of a microcontroller [530], four sensing modules based on the IC INA 226 [532] together with a shunt resistor, four relays [533] connected to the GPIO pins of the microcontroller via darlington transistors [534], a real time clock [535], a CAN FD Interface [536], a power supply for the microcontroller [537] and connectors [538].

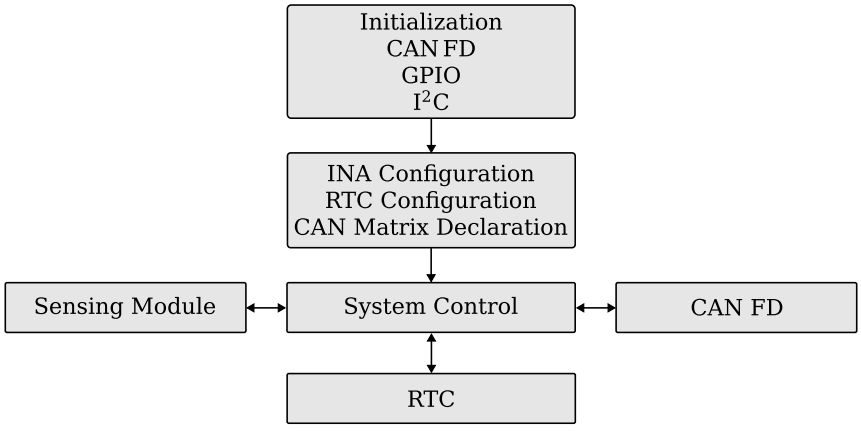


Figure 13.19: Abstracted overview of the software running on the microcontroller of the load box.

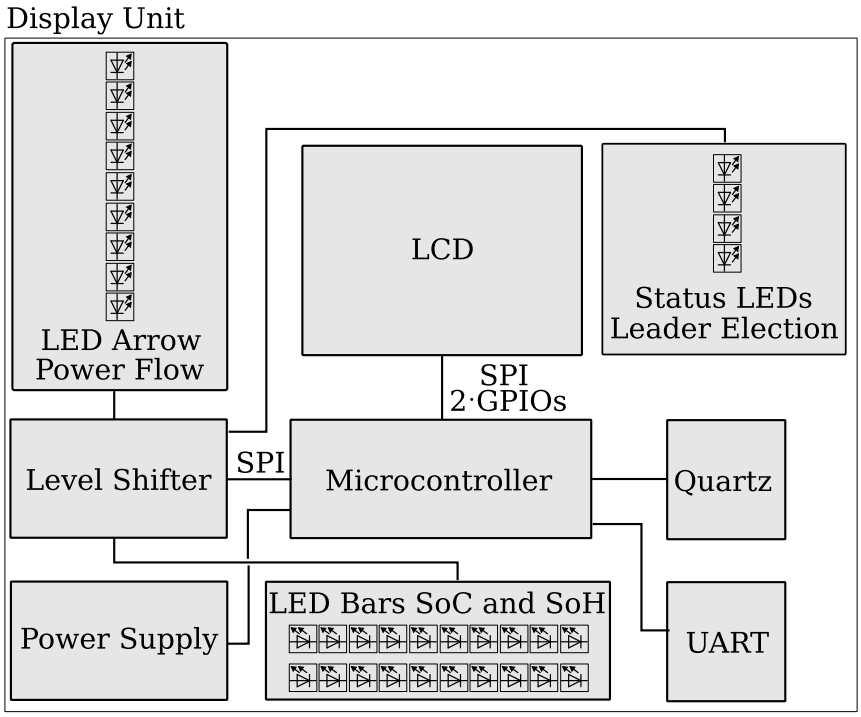


Figure 13.20: Block diagram of the display unit: The microcontroller controls the LEDs and the LC-display via an SPI interface. It receives the data via the UART interface from the microcontroller of the LCU. [539–544]

their node id in the time-based database InfluxDB. Grafana is used for the graphical representation of the data.
The web interface allows remote monitoring of the system.

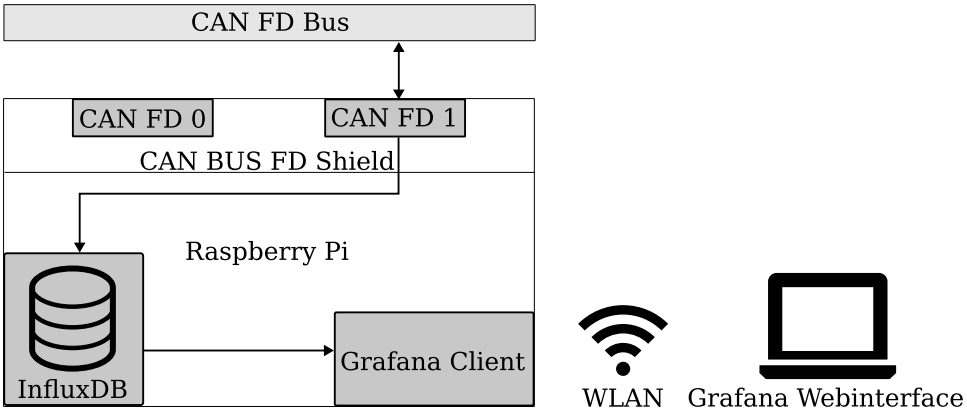


Figure 13.21: Block diagram of the CAN (FD) data logger. All the messages are logged and stored sorted by their user ID in a database. Additionally the actual state of the batteries can be monitored vie the web interface.

13.6 Summary

In this chapter the hardware components of the decentralized battery management system and their implementation were described. Various DC-DC converters were adapted to meet the requirements of the DBMS. A DC-DC converter operating in buck mode only has been implemented, and meets the requirements of an amateur

radio station, which is an example application. For the battery nodes a bidirectional, multiphase DC-DC converter was implemented. The LCU is implemented on a single PCB in the final version (Fig. 13.22). Display units show the actual operating parameters, the power flow direction and the outcome of the leader election. A load box controllable via CAN FD allows the stepwise switching of loads on or off. To monitor the operating data, all CAN messages are logged and stored in a database. The test setup (Fig. 13.23) allows a proof of concept of the proposed system.

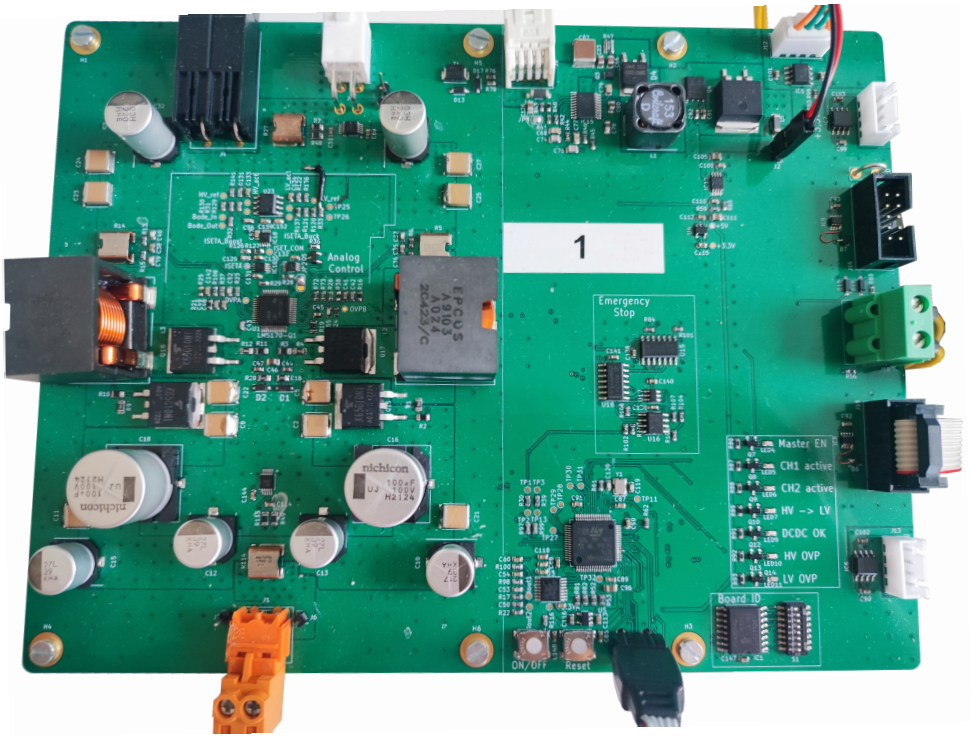


Figure 13.22: Hardware implementation of the local control unit, where the left part of the board corresponds to the power circuit and the right part to the control and communication elements.

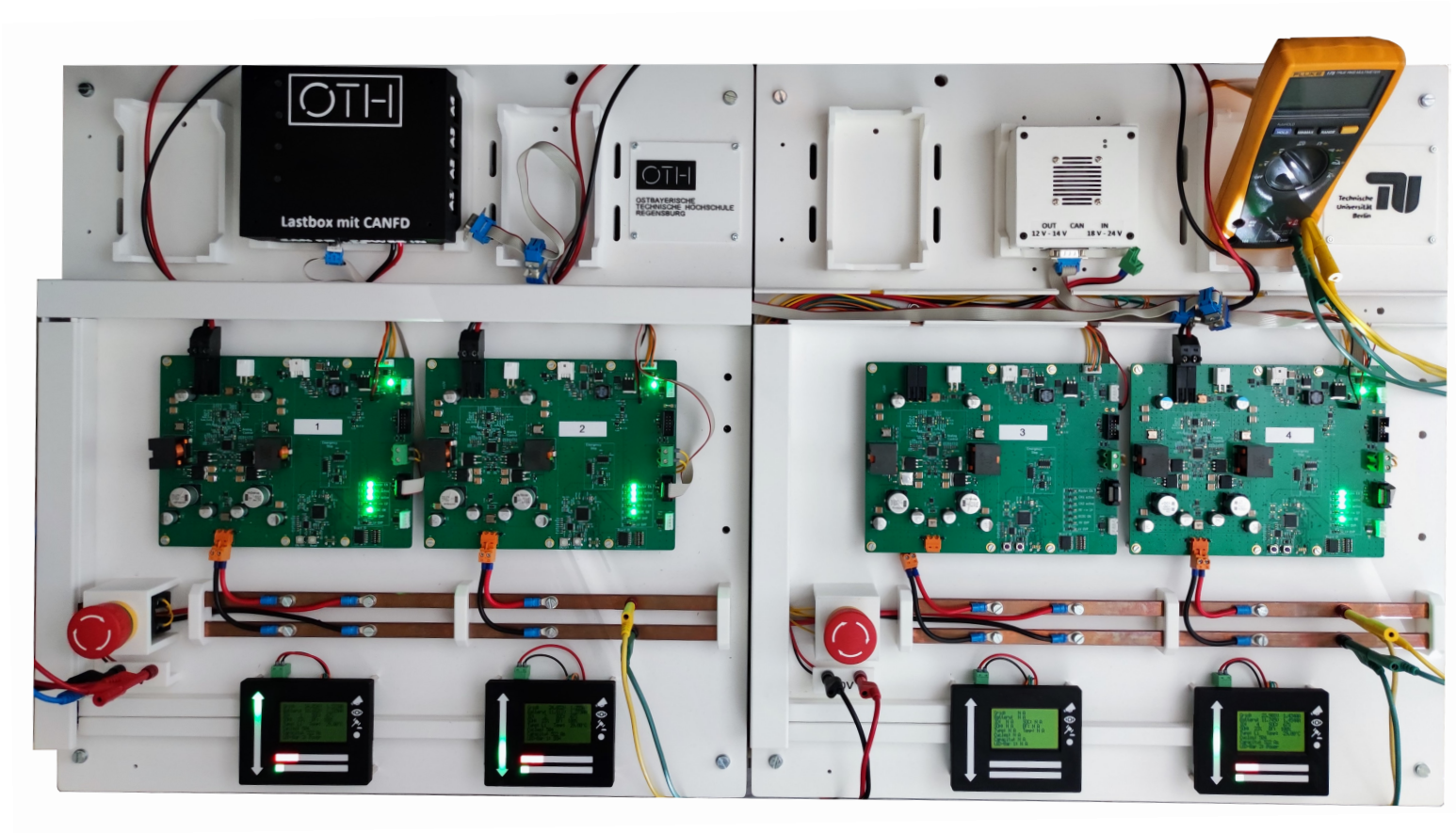


Figure 13.23: Hardware test setup consisting of four local control units (LCUs) with display units, the load box and the DC-DC converter for the load. The LCUs are connected in parallel via the copper bar. Furthermore they are connected via a CAN FD line. The multimeter is used to display the DC link voltage.

14

Experimental Data and Final Evaluation regarding the System Goals

In this chapter, the experimental validation of the decentralized battery management system architecture and the control concepts is presented. The experimental setup consists of up to four Local Control Units (LCUs) connected in parallel in addition to electronic loads and supplies to emulate batteries, generators and loads as well as ohmic loads. First, the droop-based control method is validated and analyzed in buck and boost mode using an electronic and an ohmic load. Subsequently, the communication-based digital control scheme is investigated also in buck and boost mode. Experiments with varying load distribution gain factors are conducted and a correlation between the accuracy of the load current distribution and the magnitude of the gain factor is observed. Finally, specific application cases are examined. System start-up using the droop-based control is investigated as well as switching between the droop- and the communication-based control. The impact of an initial election process on the control is analyzed. Furthermore, the abrupt change of the values of the load distribution factors is investigated. For the estimation of the system robustness and reliability, the influence of an incorrect voltage measurement and an unannounced deactivation of a DC-DC converter is investigated.

14.1 Experimental Setup

To validate the operation of the DBMS, between two and four LCUs are connected in parallel. The DC-DC converters are operated in buck and boost mode respectively. The test setups for the two operating modes differ slightly (Figs. 14.1, 14.2).
The batteries are emulated by electronic supplies. A sliding resistor (ohmic) or an electronic load, which can generate constant load currents, rectangular and ramp shaped load currents, are used as loads. When using the sliding resistor, load changes are generated by manually moving the wiper.
The display units (Figs. 14.1, 14.2) are used to monitor the instantaneous values. The microcontrollers of the LCUs sample the voltage measurements at the Low Voltage

(LV) and High Voltage (HV) side with a frequency of $115.2\,kHz$ and the current values with a frequency of $10\,kHz$. The voltage is measured via a voltage divider. The downscaled voltage proportional to the HV or LV voltage is subsequently converted to a digital value using the internal 12 bit ADC of the microcontroller. The output current is determined via the two $I_{\text{out}1,2}$ pins of the LM5170 controller. The output current of each of the two channels is measures by the voltage drop across the shunt resistor. A current proportional to the actual output current of the corresponding channel flows out of the respective I_{out} pin. Terminating resistors and filter capacitors connected to the I_{out} pins generate a voltage. The two voltages are converted into two corresponding digital values by the external ADC, and sent to the microcontroller via an SPI interface.
The micrcontroller processes and adds the digital current values and generates a CAN FD message with the actual total output current value of the DC-DC converter, together with the LV and the HV voltage measurement values. The messages are sent with a frequency of $10\,kHz$. These messages are received and processed by all other microcontrollers. Furthermore, all CAN FD messages are logged by a Python script running on the test laptop and sorted according to the user ID, which is identical to the LCU ID.
In the following measurements, $12\,V$ is used as the setpoint for the LV voltage and $24\,V$ as the setpoint for the HV voltage. Both voltages are variably adjustable in a range from $0\,V$ to $48\,V$. The objective of the designed control concepts is to realize a load sharing between the parallel connected DC-DC converters in addition to the control to the setpoint voltage at the HV- and LV-side.
The terms *LCU* and *DC-DC converter* are used synonymously. The DC-DC converter is part of the power circuit of the LCU which additionally integrates a microcontroller, an external ADC and sensors.
In the following measurement graphs, deviations from the setpoint are represented by error shadows, i.e. transparent filled areas.

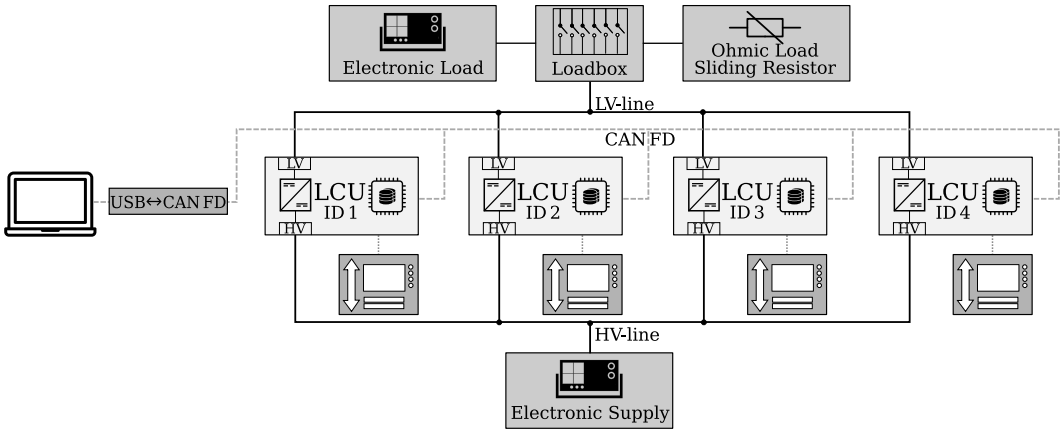


Figure 14.1: Test setup to validate the operation and the control of the DC-DC converters in buck mode, i.e. when the batteries are charged. The HV voltage of $24\,V$ is provided by an electronic supply. The DC-DC converters are connected to the HV line. At the LV line a load (ohmic or electronic load) is connected via the load box. The load box closes the relays according to the instructions received via CAN-FD messages and connects one of the loads to the LV line. In addition, current and voltage are measured via an INA sensor (measurement based on a shunt resistor). The set point of the voltage to be controlled at the LV-line is $12\,V$.

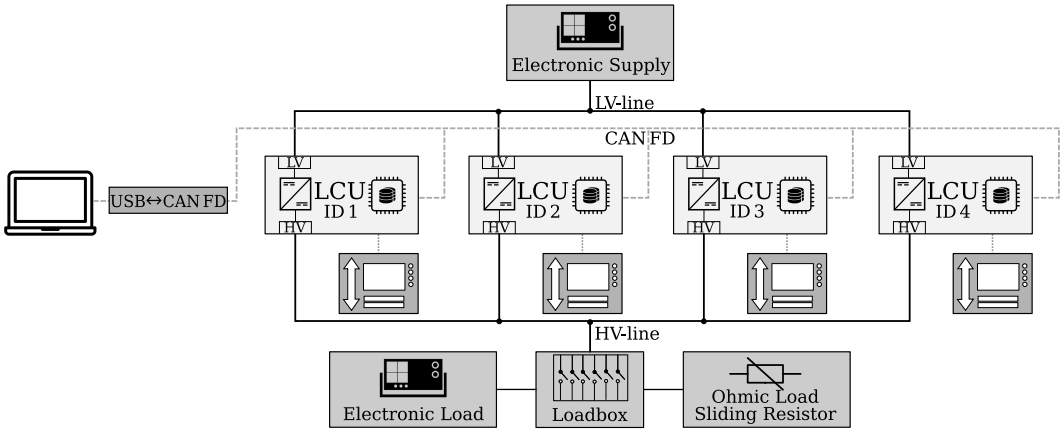


Figure 14.2: Test setup to validate the operation of the control and the DC-DC converters in boost mode, i.e., when the batteries are discharged. The batteries are replaced by an electronic supply connected to the LV sides of the DC-DC converters. It provides a constant voltage of $12\,V$ in the following tests. On the HV side, a slide resistor or an electronic load is connected via the load box. The load box closes relays according to commands received via CAN FD messages and connects one of the loads to the HV line. Furthermore, it detects current and voltage on the HV line via an INA sensor (measurement based on shunt resistor). The set point of the voltage to be controlled at the HV-line is $24\,V$.

14.2 Experimental Data to Validate Droop-based Control

The droop-based control is characterized by the communicationless operation based on local measurements. In the DBMS, this control method is used at system startup, as long as no temporary leader is selected. Furthermore, it serves as a fallback strategy in case of communication failure or operating states that place a significant load on CAN FD communication or computing power, such as a big leader election process or software updates. The droop-based control with virtual droop resistor is chosen and implemented exclusively with the analog control variant. An implementation with the digital control is possible in principle, however, it was omitted in the context of this thesis, since the droop-based control is used only for the aforementioned purposes. The virtual droop resistor is implemented as a variable on the microcontroller and allows to change the load sharing between the DC-DC converters during operation. Furthermore, the battery condition can be taken into account, for example in the form of a battery fitness dependent droop resistor. A second variable, the reference voltage, allows the setpoint voltage to be changed. For boost and buck respectively, there is one variable for the droop resistor and one for the reference voltage.

14.2.1 Droop-based Control in Boost Mode

One of the primary use cases is the start-up of the system, where the DC-DC converters operate in boost mode to set the HV-line to the reference value. Figure 14.3 on p. 276 shows the measurement of four DC-DC converters connected in parallel operating in boost mode and using the droop-based control. The test setup is according to figure 14.2 using the ohmic load without variations ($I_\mathrm{L} \approx 4\,A$). Equal droop resistors ($R_\mathrm{d} = 0.1\,\Omega$) and equal reference voltages ($V_\mathrm{ref} = 2.02\,V$) are used for all LCUs. It

can be clearly seen that the DC-DC converter with ID 4 responds to small voltage deviations with a rather high output current ($t = 2200\,ms$, $t = 5000\,ms$, $t = 7000\,ms$, $t = 9000\,ms$, $t = 10000\,ms$, beginning from $t = 13000\,ms$). The way too high output current of the DC-DC converter with ID 4 leads to overshoots of the HV voltage to be controlled up to $V_{\mathrm{HV}} = 26.6\,V$. This behavior is due to a too high gain factor, which results from the droop resistor and the internal resistance of the DC-DC converter. Although the DC-DC converters were built with the same components, they show different output characteristics due to component tolerances.
In the first measurements, the load had the shortest line distance to the DC-DC converter with the ID 4. The first assumption was that the line resistance, which was the lowest for the DC-DC converter with the ID4, caused this behavior. Re-localization of the load showed that the line resistances have only a minor effect on the load distribution and the behavior of the DC-DC converter with the ID 4 remained similar.
Individual adjustments to the reference voltage allow the output characteristics to be taken into account. Figure 14.4 on p. 277 shows the measurement under similar circumstances with adjusted reference voltages. The DC-DC converter with the ID 4 no longer delivers excessive output currents and the voltage at the HV-side remains stable at the setpoint value. A closer look at the currents shows that they are still not identical. The largest deviation shows the output current of the DC-DC converter with the ID 3 with approximately $-0.2\,A$ offset.
A more precise consideration of the different output characteristics of the DC-DC converters, as well as additional consideration of the temperature and aging influences on them and the inclusion of the line resistances are possible approaches to improve the load sharing accuracy. A possible implementation in future work would be to set all the droop resistors to an identical value and use the current measurement of the load box as well as the single output current measurements of the DC-DC converters. One of the microcontrollers, for example the temporary leader or the microcontroller of the load box, subsequently generates adjusted reference voltage values until the output currents of the DC-DC converters are approximately the same. In this way, aging and temperature effects can also be taken into account by periodically repeating the adjustment of the reference voltages.
Figure 14.5 on p. 278 shows a measurement with four DC-DC converters connected in parallel in boost mode with different droop resistors and adjusted reference voltages. The load changes were generated by manually shifting the wiper of the sliding resistor. The DC-DC converter with ID2 has the lowest droop resistance in this case, which corresponds to the highest gain. The DC-DC converter with ID 4 has the highest droop resistance, which corresponds to the lowest gain compared to the rest.
Figure 14.6 on p. 279 shows another measurement with identical setting. In the beginning the load is still changed followed by a constant load current. In this case, the droop-based control with different droop resistor values also shows the desired effect in the load current distribution.

Conclusion

The droop-based control in boost mode was successfully validated. The control to the setpoint voltage value was achieved and remained stable even during high load changes. The total load current was divided between the components. Using identical droop resistor values, showed that the DC-DC converters have different output characteristics, in particular different internal resistances. This leads to different

output currents with identical droop resistors. Initial adjustments of the reference voltage, a software variable for setting the voltage setpoint, showed that the output characteristics can be taken into account in this way. A detailed analysis of the output characteristics is recommended for future work. A possible method for adjusting the reference voltage is described.

14.2.2 Droop-based Control in Buck Mode

In order to use the droop-based control as a fully functional fallback strategy, correct operation in buck mode is also required. The test setup is as shown in figure 14.1, using the electronic load with rectangular load steps between $6A$ and $10A$. The reference voltages are also adjusted according to the individual output characteristics in buck mode.
Figure 14.7 on p. 280 shows the measurement of four DC-DC converters connected in parallel which operate in buck mode with droop-based control. The voltage fluctuations at the HV side are due to interferences between the electronic supply and the electronic load. The LV voltage to be controlled remains stable at approximately $12V$ over the entire measurement period. The total load current is successfully distributed between the parallel connected DC-DC converters. The DC-DC converters have identical droop resistances. Detailed examination of the load currents (Fig. 14.8 on p. 281 and Fig. 14.9 on p. 282) show deviations from the actual setpoint marked by error shadows (transparent filled areas p. 276 ff.). Furthermore, all measurement plots are divided into voltage and current measurements, whereby the voltage measurement plots also show the course of the currents (marked with grey lines) in order to better recognize the effect of current changes on the voltage to be regulated. The maximum deviation from the nominal value is approximately $0.2A$.

Conclusion

The droop-based control in buck mode was successfully validated. The voltage control to the setpoint value was achieved and remained stable even during high load changes. The load current was distributed in accordance to the droop resistors. Also in this case, a more precise adjustment of the reference voltage could still improve the accuracy of the load current sharing.
For the use as a fallback strategy and as a control strategy for the system start-up, the deviations that occurred in boost and buck mode are tolerable.

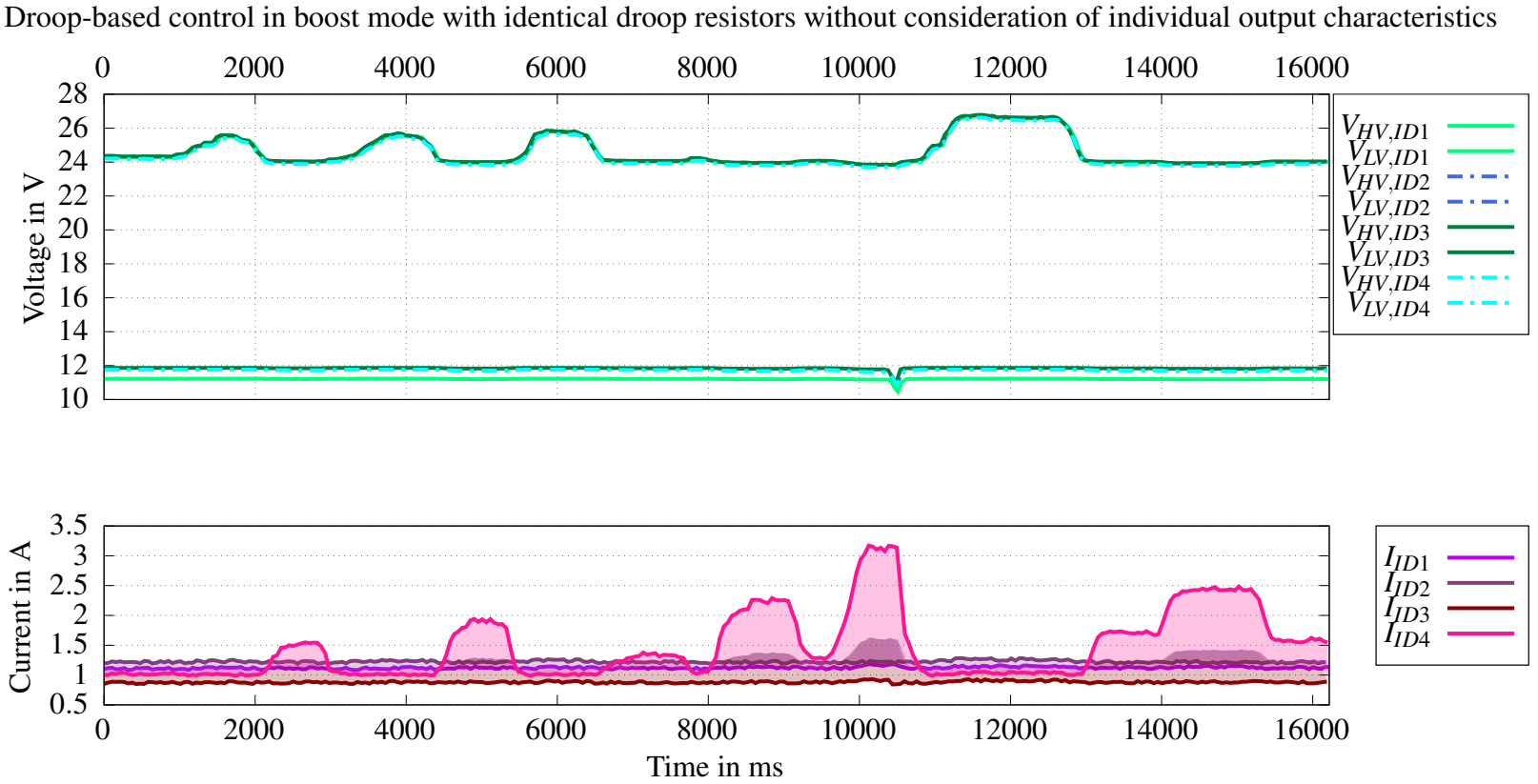


Figure 14.3: Four DC-DC converters connected in parallel operate in boost mode using droop-based control. All DC-DC converters have identical droop resistance ($R_\mathrm{d} = 0.1\,\Omega$) and individual output characteristics are not considered ($V_\mathrm{ref} = 2.05\,V$). The DC-DC converter ID1 has an incorrect LV measurement. The DC-DC converter ID4 has a lower internal resistance compared to the remaining ones, which leads to an increased total gain resulting in high output currents and fluctuations at the high voltage.

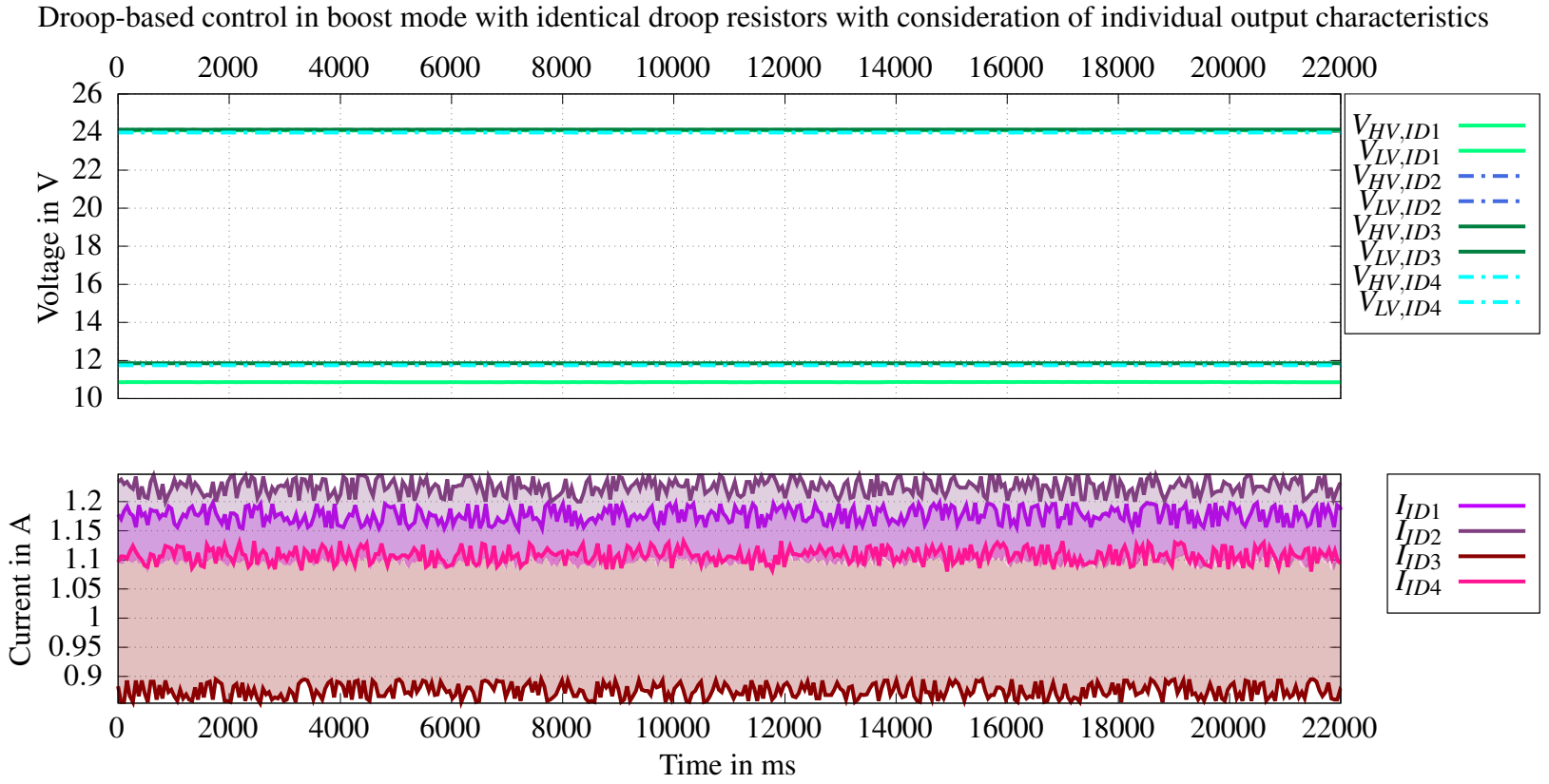


Figure 14.4: Four DC-DC converters are connected in parallel and operate in boost mode. For load distribution, the droop-based analog control is used with equal droop resistors with considering individual output characteristics ($R_{\mathrm{d,ID1-4}} = 0.1\,\Omega$, $V_{\mathrm{ref,ID1}} = 2V$, $V_{\mathrm{ref,ID2}} = 1.87V$, $V_{\mathrm{ref,ID3}} = 2.02V$, $V_{\mathrm{ref,ID4}} = 2V$). The LV measurement of the DC-DC converter with the ID1 is incorrect. The DC-DC converters do not exhibit equal output currents due to varying output characteristics and measurement tolerances.

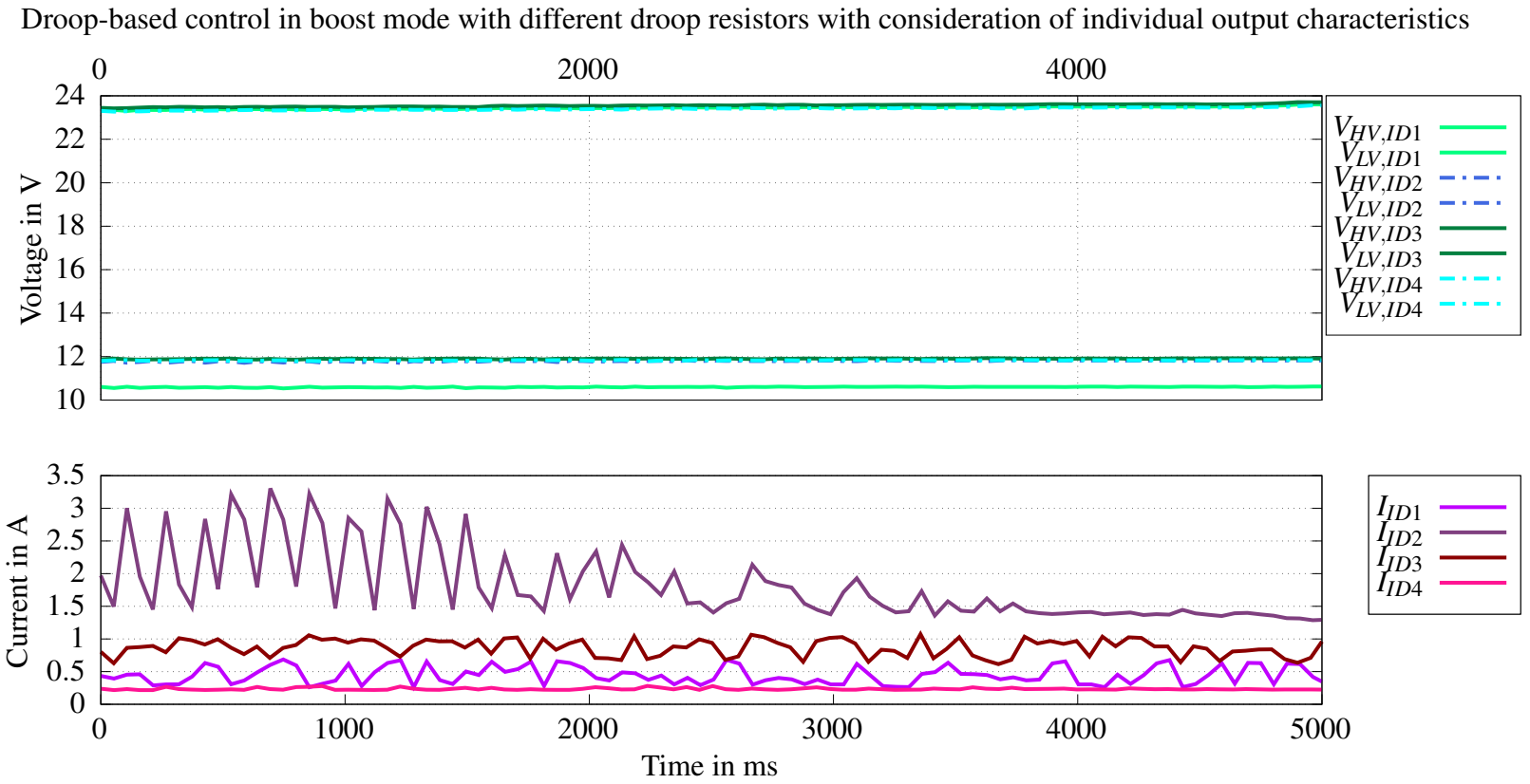


Figure 14.5: Four parallel connected DC-DC converters, which operate with analog, droop-based control in boost mode, are connected at the HV-side to an ohmic load and at the LV-side to an electronic supply. The reference voltages are adjusted in order to change the output behavior of the DC-DC converters and the droop resistors are different ($R_{\mathrm{d,ID1}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID1}} = 2\,V$, $R_{\mathrm{d,ID2}} = 0.3\,\Omega$, $V_{\mathrm{ref,ID2}} = 1.87\,V$, $R_{\mathrm{d,ID3}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID3}} = 2.02\,V$, $R_{\mathrm{d,ID4}} = 1.2\,\Omega$, $V_{\mathrm{ref,ID4}} = 2\,V$).

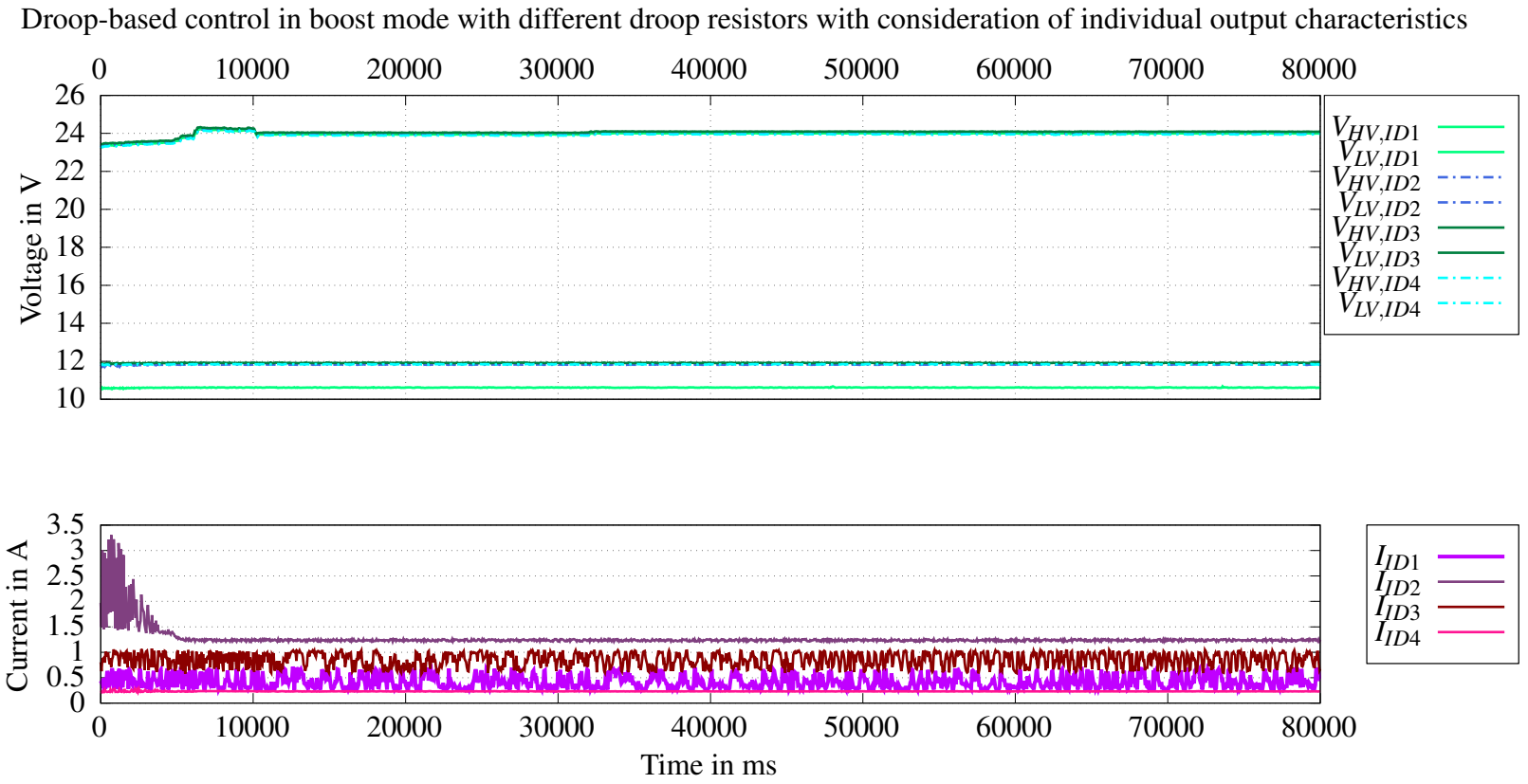


Figure 14.6: Four DC-DC converters connected in parallel operate in boost mode using the droop based control. An ohmic load is connected at the HV-side. Both the droop resistors and the reference voltages are individual adapted ($R_{\mathrm{d,ID1}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID1}} = 2\,V$, $R_{\mathrm{d,ID2}} = 0.3\,\Omega$, $V_{\mathrm{ref,ID2}} = 1.87\,V$, $R_{\mathrm{d,ID3}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID3}} = 2.02\,V$, $R_{\mathrm{d,ID4}} = 1.2\,\Omega$, $V_{\mathrm{ref,ID4}} = 2\,V$).

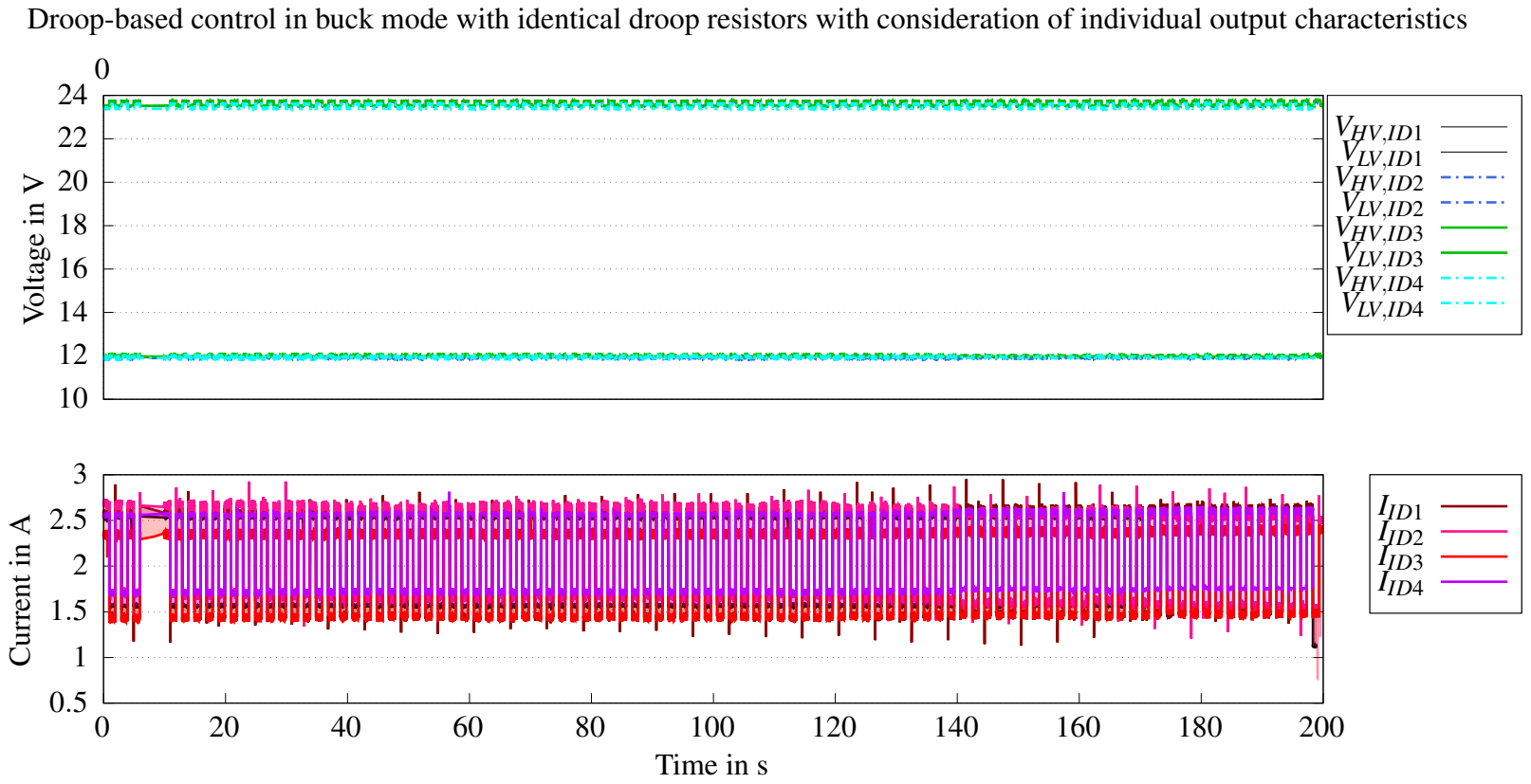


Figure 14.7: Measurement over a duration of 200 s: Four parallel connected DC-DC converters, which operate with analog, droop-based control in buck mode, are connected at the HV-side to an electronic supply and at the LV-side to an electronic load which generates rectangular load jumps between 6 A and 10 A. The reference voltages and the droop resistors are identical. Fluctuations at the HV-side are due to interference of the electronic supply and load.

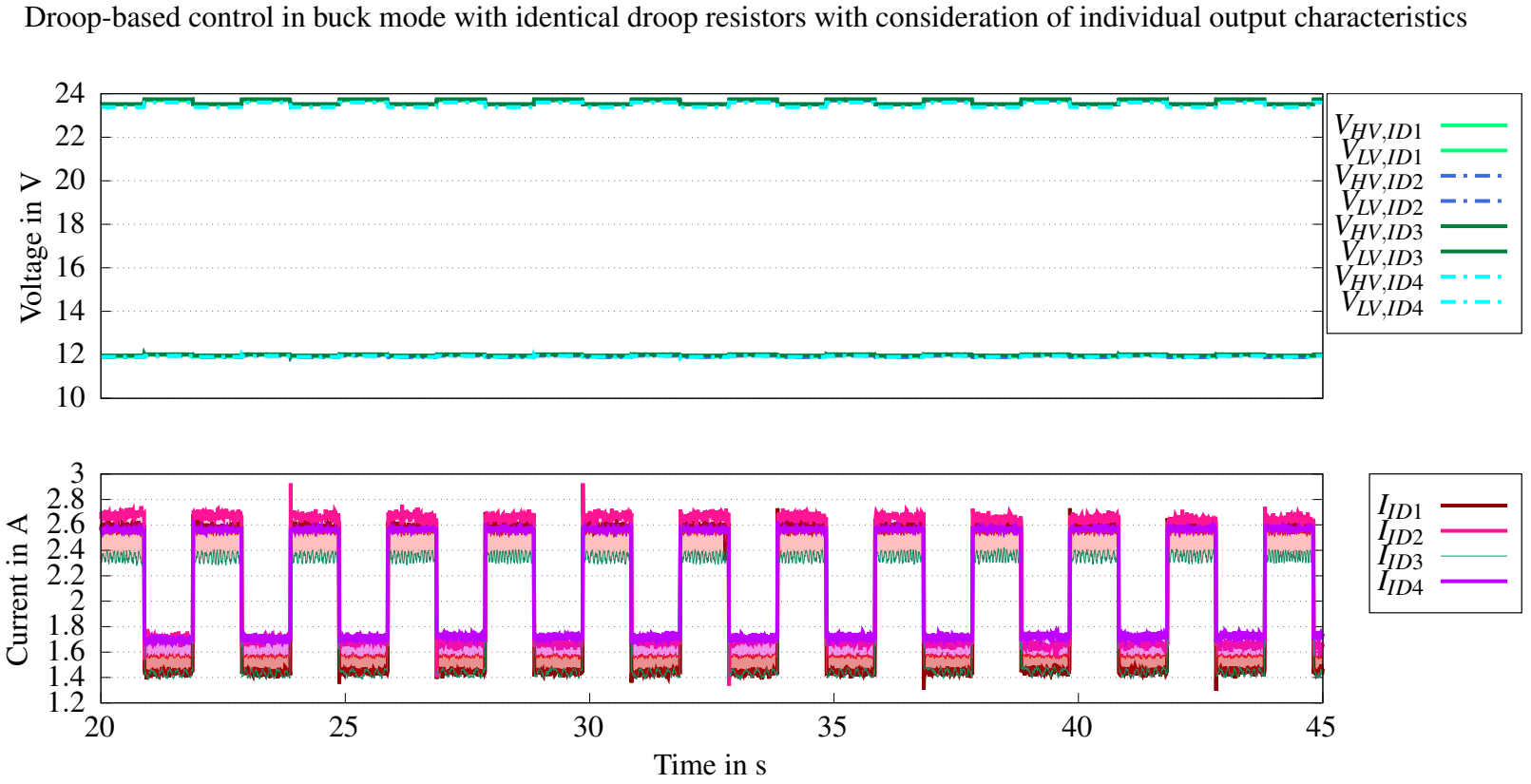


Figure 14.8: Excerpt of the measurement in Fig.14.7: Four parallel connected DC-DC converters, which operate with analog, droop-based control in buck mode, are connected at the HV-side to an electronic supply and at the LV-side to an electronic load which generates rectangular load jumps between $6A$ and $10A$. The reference voltages and the droop resistors are identical. Fluctuations at the HV-side are due to interference of the electronic supply and load.

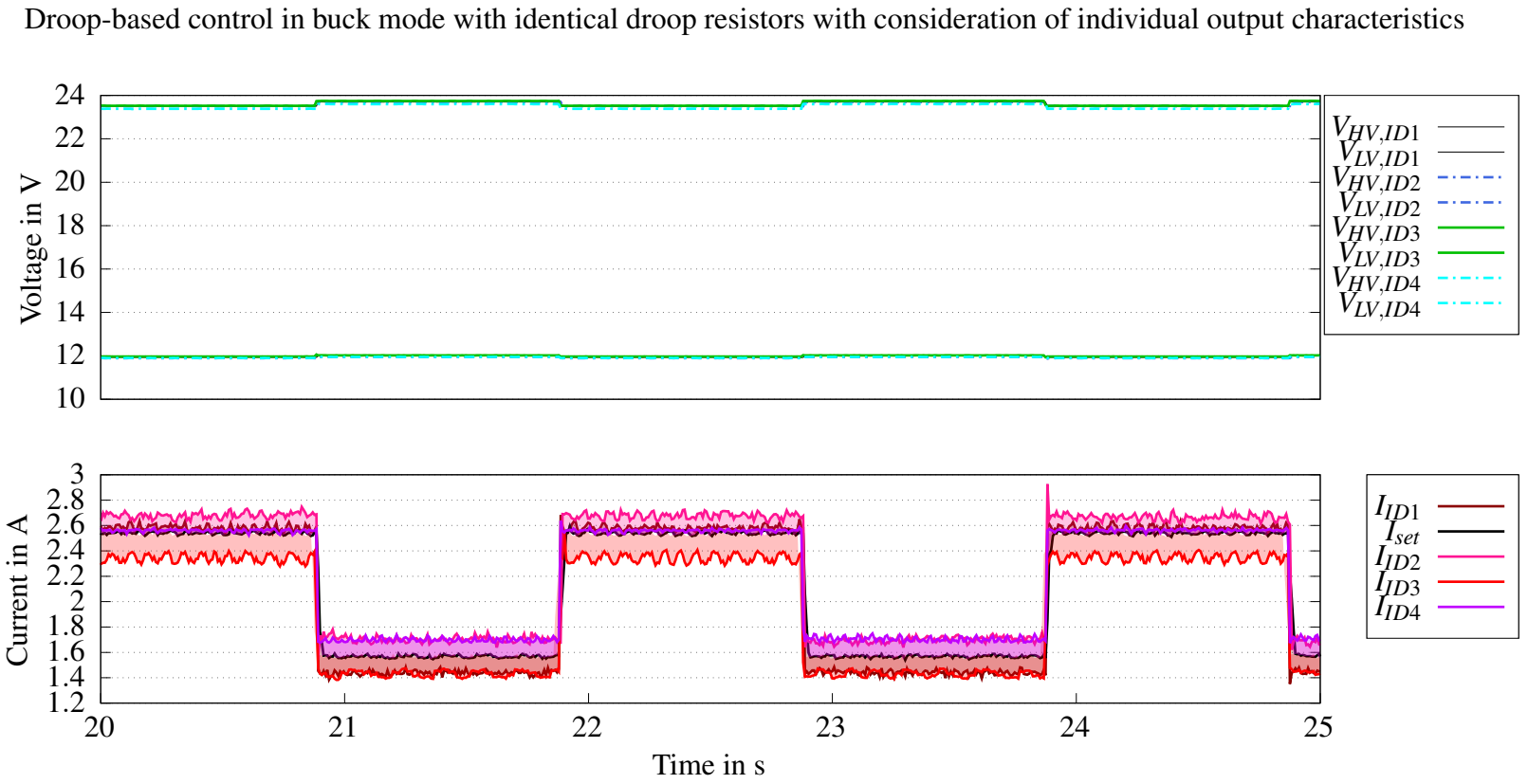


Figure 14.9: Excerpt of the measurement in Fig.14.7: Four parallel connected DC-DC converters, which operate with analog, droop-based control in buck mode, are connected at the HV-side to an electronic supply and at the LV-side to an electronic load which generates rectangular load jumps between $6A$ and $10A$. The reference voltages and the droop resistors are identical. Fluctuations at the HV-side are due to interference of the electronic supply and load.

14.3 Experimental Data to Validate Communication-based Control

The communication-based load distribution control is primarily used as control method in the DBMS, as it allows load current distribution with high accuracy. The prerequisite for its use is a fault-free, functioning broadcast communication between the nodes and a selected temporary leader. The temporary leader specifies the distribution factors and sends the measured value of the actual total load current to all the remaining nodes, which is the basis for an exact load current distribution. Subsequently, the communication-based load distribution control is verified with the digital control implementation. The use of the analog control is also implemented for the communication-based load distribution control and can be used accordingly. However, the digital implementation is the preferred one in this case because it allows the implementation of adaptive control. Since the control behavior is load dependent, different control parameters can be stored for different load ranges. In the context of this work, the use of a single control parameter set is validated. Switching between two parameter sets is also successfully tested. The simulation of the entire control system allows the calculation of the corresponding control parameters for different load ranges and can be used in future work to determine the different control parameter sets.
The digital implementation is realized once by direct calculation of the control parameters and the adapted duty cycles by the microcontroller and by using the Filter Math ACcelerator (FMAC) unit of the microcontroller. In the following, the digital communication-based control with direct calculation by the microcontroller in boost and buck mode is validated first and the effect of different gain factors of the load distribution control is examined. Subsequently, the functionality of the FMAC is confirmed. Finally, the abrupt change of the load distribution factors is investigated.

14.3.1 Communication-based Digital Control in Boost Mode

The communication-based digital control with direct calculation of the updated manipulated variables by the microcontroller is analyzed subsequently in boost mode. In the communication-based load distribution control, the distribution factor is amplified by a gain factor. Higher gain factors result in more accurate load sharing, but can also lead to overshoots. Figure 14.10 on p. 287 shows the measurement of two parallel connected DC-DC converters in boost mode using the communciation-based digital control with a comparatively high load sharing gain factor of $g_{\mathrm{dis}} = 0.3$. The load distribution factors are $\alpha_{\mathrm{ID}\,3} = 20\%$ and $\alpha_{\mathrm{ID}\,4} = 80\%$. The test setup is according to figure 14.2 using a slide resistor with manually shifted wiper. Only very small deviations occur in the load sharing (recognizable by the few small error shadows). However, overshoots of up to V occur on the voltage to be controlled on the HV-side line. However, overshoots of $\pm 2.3\,V$ up to $+3\,V$ occur on the voltage to be controlled at the HV-side line. At time $t = 11.3\,s$, a voltage overshoot occurs at the level of approximately $27\,V$ and the DC-DC converter ID 4 is deactivated as it enters the overvoltage protection state. The DC-DC converter with ID 3 takes over the entire load current until the DC-DC converter with ID 4 leaves the overvoltage protection state and is deactivated again. The overvoltage protection state occurs when the controller IC LM5170 detects an overvoltage event. The higher gain factor leads to an increased accuracy and dynamic. Nevertheless, the higher output currents

cause overshoots at the voltage side, which can trigger the deactivation of the DC-DC converter in case of an overvoltage event.
Figure 14.11 on p. 288 shows a measurement with reduced load distribution gain factor of $g_{\text{dis}} = 0.25$. The load distribution factors and the test setup remain otherwise unchanged. The magnitude of the voltage over- and undershoots on the HV-line are significantly reduced to a maximum of up to $-0.3V$ and $+0.7V$ deviation from the setpoint. The reduced amplification factor results in lower output currents and thus lower voltage overshoots. No overvoltage event occurs and the deviation from the setpoint is only slightly increased.
Figure 14.12 on p. 289 shows the measurement of two DC-DC converters connected in parallel with the distribution factors $\alpha_{\text{ID}3} = 30\%$ and $\alpha_{\text{ID}4} = 70\%$ and a reduced load distribution gain factor of $g_{\text{dis}} = 0.25$. The measurement setup is also carried out as shown in figure 14.2 using the electronic load, which generates a rectangular load current of $3A$ and $9A$ ($T = 2s$). The HV voltage to be controlled, shows overshoots and undershoots of $\pm 1.2V$ when the load current changes. Deviations occur in the load distribution control, with an average of 7.2 percent. The deviations in the load current sharing and the voltage to be controlled are within the acceptable range. No significant overshoots occur during the abrupt load current change from $3A$ to $9A$ and vice versa.
For the measurement shown in figure 14.13 on p.290, two DC-DC converters were connected in parallel with load distribution factors of $\alpha_{\text{ID}3} = 30\%$ and $\alpha_{\text{ID}4} = 70\%$ and a reduced load distribution gain factor of $g_{\text{dis}} = 0.1$. For the load, the sliding resistor is used, whose resistance value is changed manually. The further reduction of the load distribution gain factor significantly improves the voltage control accuracy. Only small voltage deviations in the amount of on average $\pm 0.1V$ and a maximum of $\pm 0.4V$ occur.

Conclusion

The digital communication-based control with direct calculation by the microcontroller was successfully validated in boost mode under high and abrupt load changes. The influence of the load distribution gain factor was explicitly analyzed. A higher load distribution gain factor leads to improved load distribution accuracy and higher control dynamics, but also to higher output currents in case of control deviations and consequently to overshoots at the voltage to be controlled. The magnitude of the gain factor represents a trade-off between higher load distribution accuracy with improved control dynamics and lower accuracy with more accurate voltage control. As a result of the measurements and their analysis, a default value for the load distribution gain factor of $g_{\text{dis}} = 0.1$ was specified and is used hereafter. The gain factor is a software variable and can also be changed during active operation. For low load currents, for example, the gain factor can be increased, since the load distribution accuracy decreases along with the load current, and a higher gain factor counteracts this.

14.3.2 Communication-based Digital Control in Buck Mode

To validate the digital communication-based control with direct computation by the microcontroller, the test setup shown in figure 14.1 is used with a sliding resistor as the load and a low load distribution gain factor of $g_{\text{dis}} = 0.1$.
Figure 14.14 on p. 291 shows a measurement of two DC-DC converters connected in parallel, which operate with digital control in buck mode. The load distribution factors

of $\alpha_{\mathrm{ID}\,1} = 30\%$ and $\alpha_{\mathrm{ID}\,3} = 70\%$ and a load distribution gain factor of $g_{\mathrm{dis}} = 0.1$ were chosen. The value of the sliding resistor is changed. The low voltage to be controlled remains stable at $12V$ throughout the entire measurement period and no significant oscillations nor overshoots occur. The load current is successfully distributed between the two DC-DC converters.
Initially ($0s < t \leq 8s$), at lower load currents, noticeable deviations from the current setpoint occur. The load distribution factors deviate by 5 percent and are actually approximately $\alpha_{\mathrm{ID}\,1} = 35\%$ and $\alpha_{\mathrm{ID}\,3} = 65\%$. In absolute values, a maximum deviation of $+0.19A$ occurs for ID1 and $-0.19A$ for ID 3 over the entire measurement period, whereby the load current value is between $1.4A$ and $4.4A$. With increasing load currents, the load distribution accuracy also increases and the load distribution is actually 30% and 70% for example at $t = 17.3s$ with a total load current of $3.1A$.

Conclusion

The communication-based digital load sharing control with direct calculation by the microcontroller in buck mode with a load distribution gain factor of $g_{\mathrm{dis}} = 0.1$ was successfully validated. Even with high load jumps, the voltage to be controlled remains stable and the deviations that occur in the load current distribution are within the acceptable range.

14.3.3 Communication-based Digital Control using the Filter Math Accelerator Unit

When using the the Filter Math Accelerator Unit (FMAC), the control parameters are calculated in parallel and autonomously, which leads to a significant reduction of the computation time required to update the control parameters. This reduces the required computation time of the control loop and allows more computation time for other calculations such as the battery fitness value or for updating the error counters. The number representation of the FMAC is limited to a maximum of 15 bits and the actual values are alternately rounded up and down.
Figure 293 on p. 293 shows four parallel connected DC-DC converters operating with communication based digital control using the FMAC in buck mode. The test setup according to figure 14.1 is used with an electronic load and a constant load current of $12A$. The load distribution factors are $\alpha_{\mathrm{ID1}} = 35\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 20\%$ and $\alpha_{\mathrm{ID4}} = 20\%$. The load distribution between the DC-DC converters is achieved successfully and the voltage to be controlled remains stable over the entire measurement period.
Figure 294 on p. 294 shows a section of the measurement from figure 293 for a more detailed analysis of the deviation in the load current distribution. Error shadows (transparent filled areas) indicate the amount of deviation. Table 14.1 lists the mean and maximum values of the deviations. They are all within the acceptable range.

Table 14.1: Mean and maximum deviation of the measurement shown in figure 14.16 on p. 293.

	$\alpha_{\mathrm{ID}\,1}$	$\alpha_{\mathrm{ID}\,2}$	$\alpha_{\mathrm{ID}\,3}$	$\alpha_{\mathrm{ID}\,4}$	$I_{\mathrm{ID}\,1}$	$I_{\mathrm{ID}\,2}$	$I_{\mathrm{ID}\,3}$	$I_{\mathrm{ID}\,4}$
Average	-0.45%	-1.89%	-0.5%	2.7%	$-0.06A$	$-0.23A$	$-0.06A$	$0.35A$
Maximum	-1.16%	-2.49%	-1.12%	4.61%	$-0.14A$	$-0.31A$	$-0.14A$	$0.56A$

In figure 14.18 on p. 295 the measurement of two DC-DC converters operating in buck mode with communication based digital control using the FMAC is shown. They are connected at the LV-side with an electronic load which first generates a constant load current of $11\,A$, then suddenly drops to $3A$ and ramps up to 11 A again. The load distribution factors are identical with a value of $\alpha = 50\%$. Deviations in the load current distribution occur over the entire load current range indicated by error shades, with a maximum of 3% or $0.5A$. The load change from $11\,A$ to $3A$ at $t = 6.5\,s$ results in a voltage rise to a maximum of $13.6\,V$.
The test setup for the measurements in figure 14.19 on p. 296 is similar with the use of a rectangular load current with load jumps between $6A$ and $13A$. The load distribution factors remain $\alpha = 50\%$ for each DC-DC converter and communication-based, digital load distribution control with FMAC in buck mode is used. Deviations in the load current distribution occur over the entire load current range, with a maximum of 3% or $0.5A$. When the load current value changes, voltage deviations of $\pm 0.3\,V$ occur.

Conclusion

The control objectives of control to a stable output voltage and load distribution between the DC-DC converters connected in parallel according to the specified load distribution factors are also achieved when using the FMAC unit for calculating the control parameters. The limited number representation of the FMAC and the alternating up and down rounding of the actual values can be seen in the output currents of the DC-DC converters. The voltage control remains stable. The deviations that occur in the load current distribution are within the acceptable range. For an improved load current distribution, it is recommended to use improved methods for the conversion of the instantaneous values to the limited number representation in a future work.

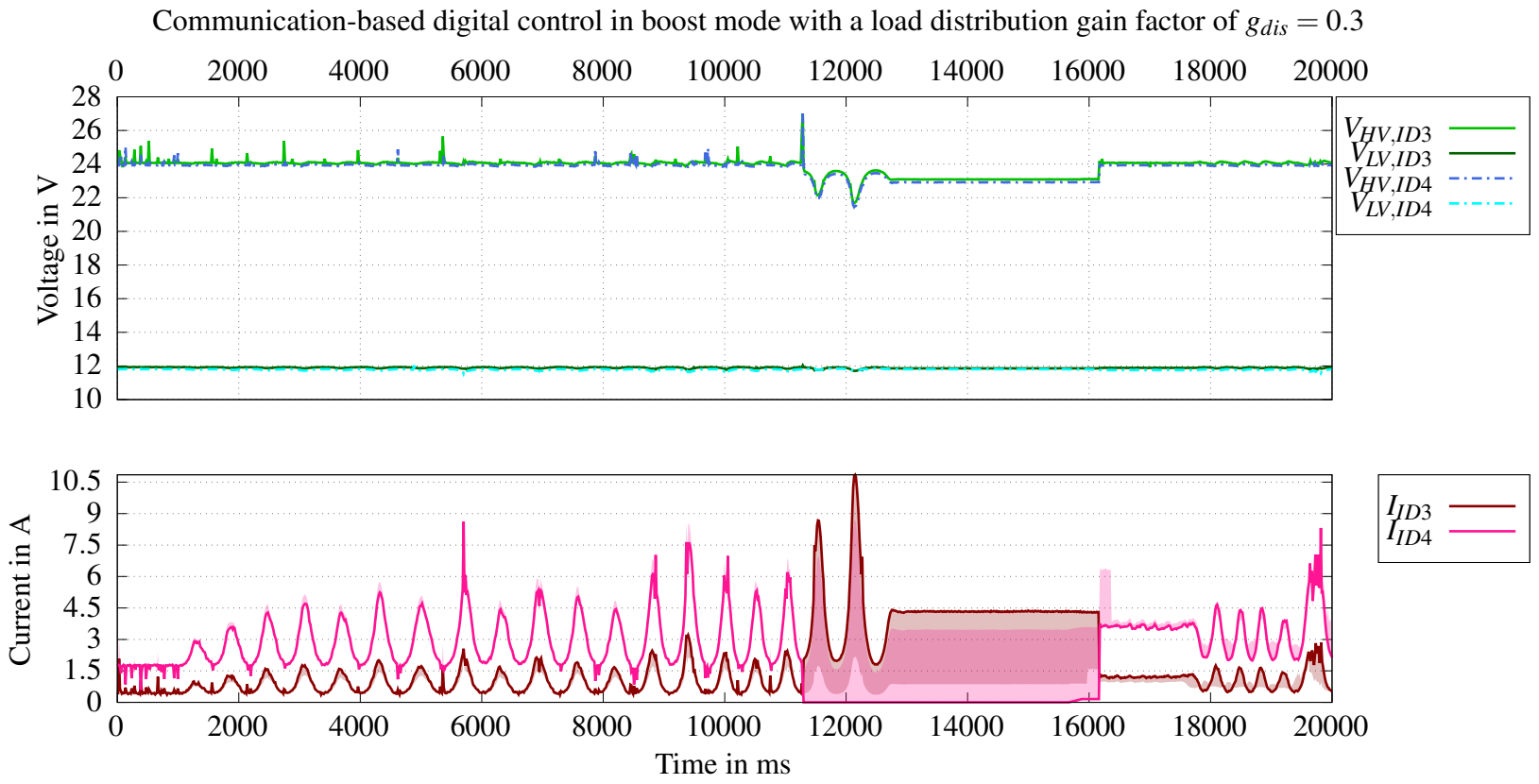


Figure 14.10: Two DC-DC converters (ID 3, ID 4) are connected in parallel and operate in boost mode. They are connected to a ohmic load at the HV-side. The digital load distribution control without FMAC with fixed sharing factors of $\alpha_{\mathrm{ID}3} = 20\%$ and $\alpha_{\mathrm{ID}4} = 80\%$ is used. The load sharing gain factor is high at 0.3. The sharing accuracy is increased. However, the high gain factor also leads to high output currents and eventual to the occurrence of the overvoltage protection state. At the time $t = 11\,s$ the overvoltage protection leads to the deactivation of the DC-DC converter ID 3. The DC-DC converter ID 4 takes over a majority of the load current and the high side voltage remains at $23\,V$.

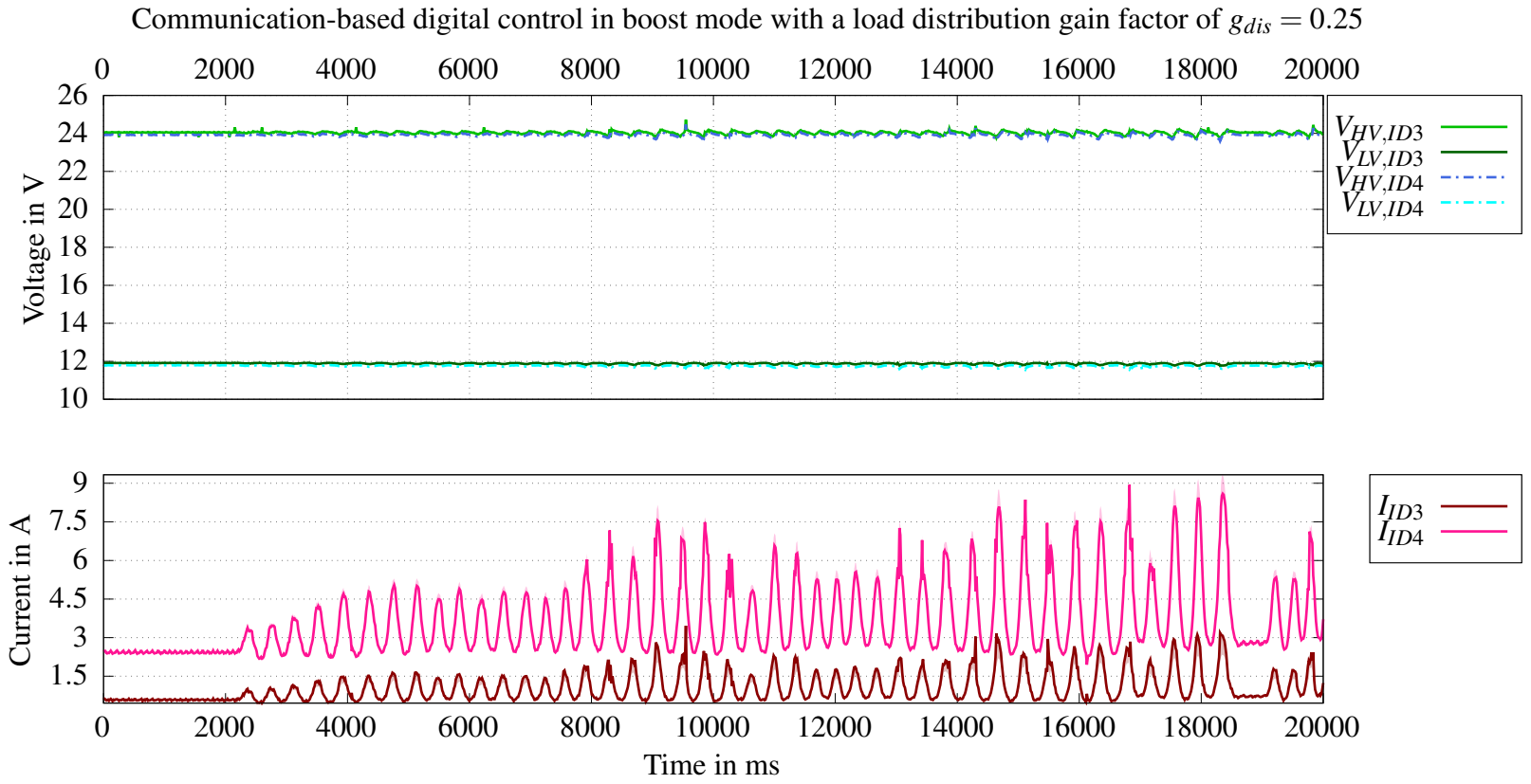


Figure 14.11: Digital load sharing control without FMAC with a parallel connection of two DC-DC converters (ID 3, ID 4) and a fixed load sharing of 20% (ID 3) and 80% (ID 4). The load sharing gain factor of 0.25 results in higher current distribution accuracy. Due to the lower gain factor, the output currents are also lower and consequently the probability of the occurrence of the overvoltage protection state is also lower. The higher gain factor still results in voltage fluctuations.

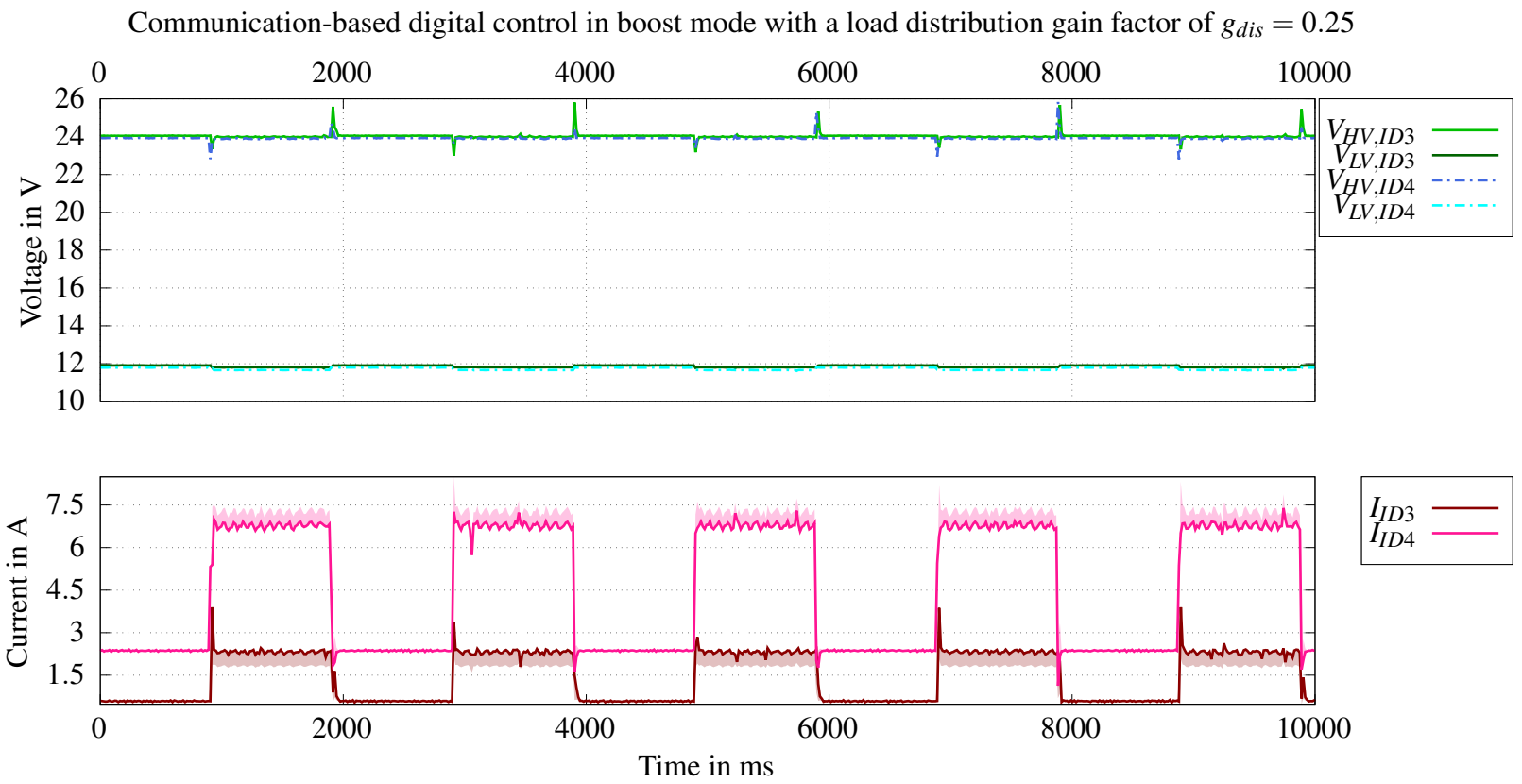


Figure 14.12: The two DC-DC converters (ID 3, ID 4) connected in parallel operate in boost mode. At the HV-side an electronic load is connected generating rectangular load steps from $3A$ to $9A$. The digital load distribtution control with fixed sharing factors of 30% (ID 4) and 70% (ID 3) and a gain factor of 0.25 is used. With the high voltage to be regulated, overshoots and undershoots of up to $\delta V = 1.2V$ occur at the time of the load current change. Reducing the gain factor results in a reduction of the magnitude of these.

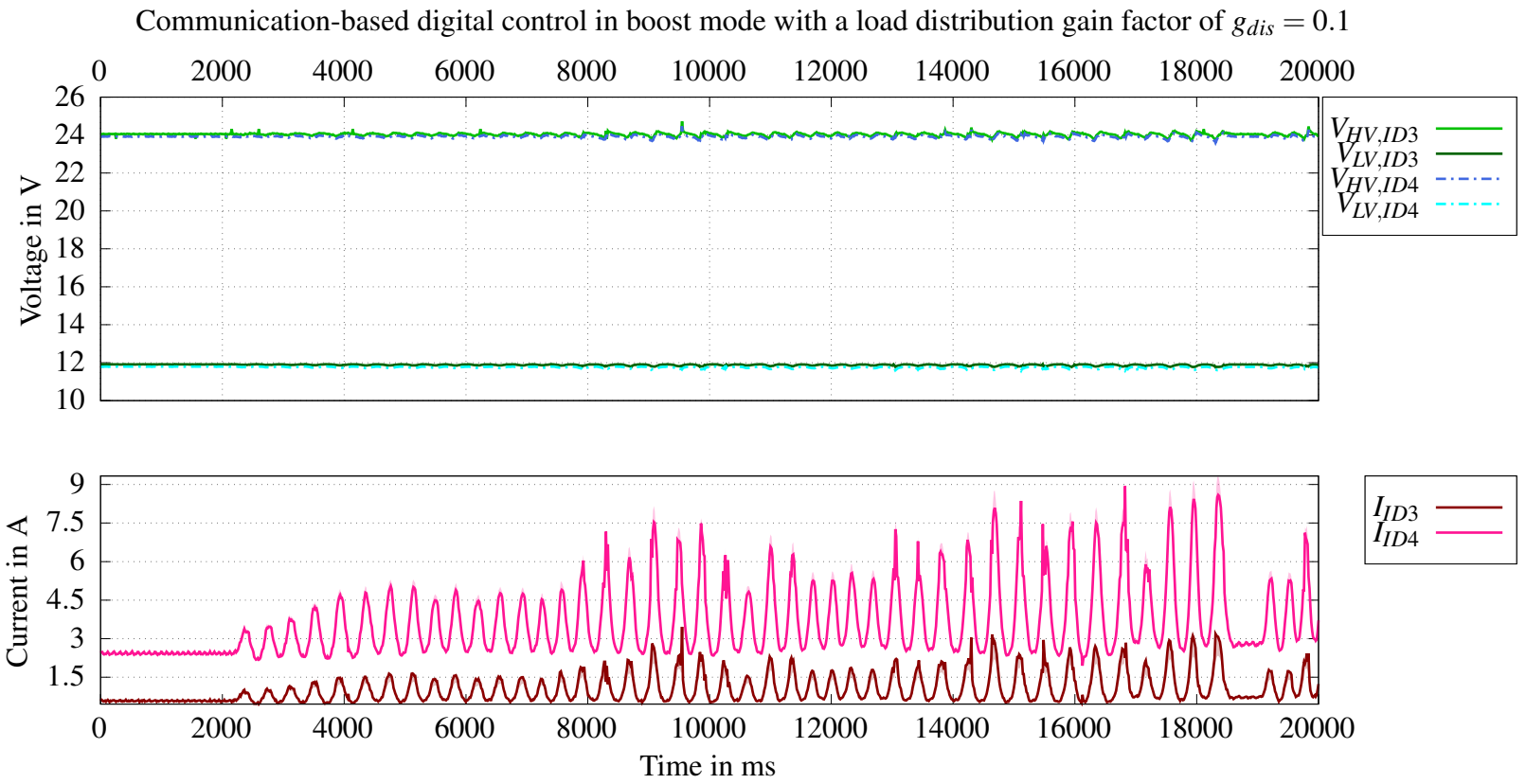


Figure 14.13: Two DC-DC converters (ID 3, ID 4) are connected in parallel and connected to a ohmic load at the HV-side. They operate in boost mode. Communication based digital control without FMAC is used and a fixed load sharing of 30% (ID 3) and 70% (ID 4). The gain factor of the load distribution is low with 0.1. Deviations in load distribution occur and amount to up to 5%, especially at low currents. This results in a load sharing of 25% (ID 3) and 75% (ID 4). An ohmic load is used.

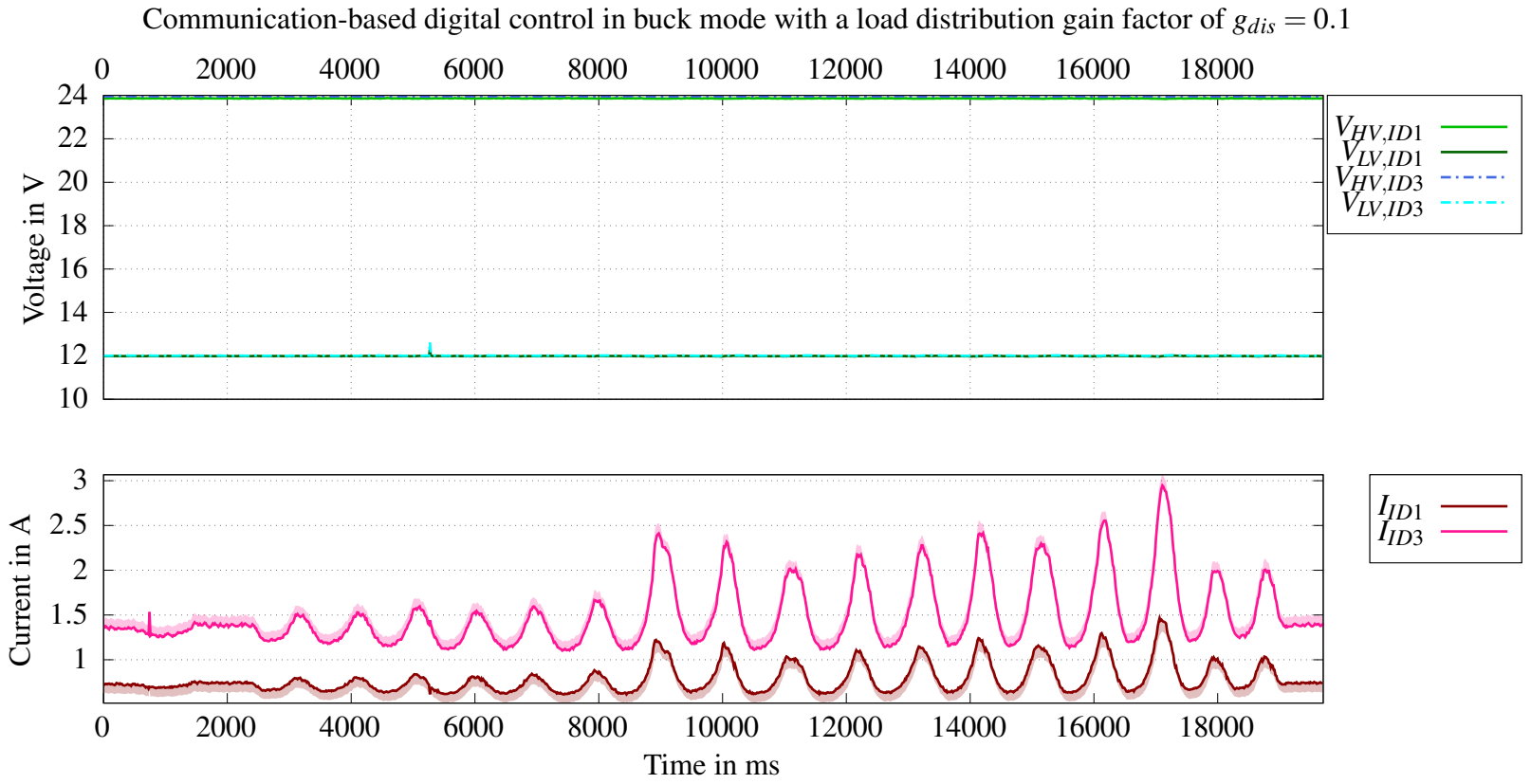


Figure 14.14: Load sharing between two parallel connected DC-DC converters (ID 1, ID 3) operating in buck mode. The digital load distribution control is used without using the FMAC. A fixed load sharing of 30% (ID 1) and 70% (ID 3) is chosen. The gain factor of the load distribution (g_{dis}) is low and equals 0.1. The actual load distribution is approximately 35% (ID 1) to 65% (ID 3). An ohmic load is used.

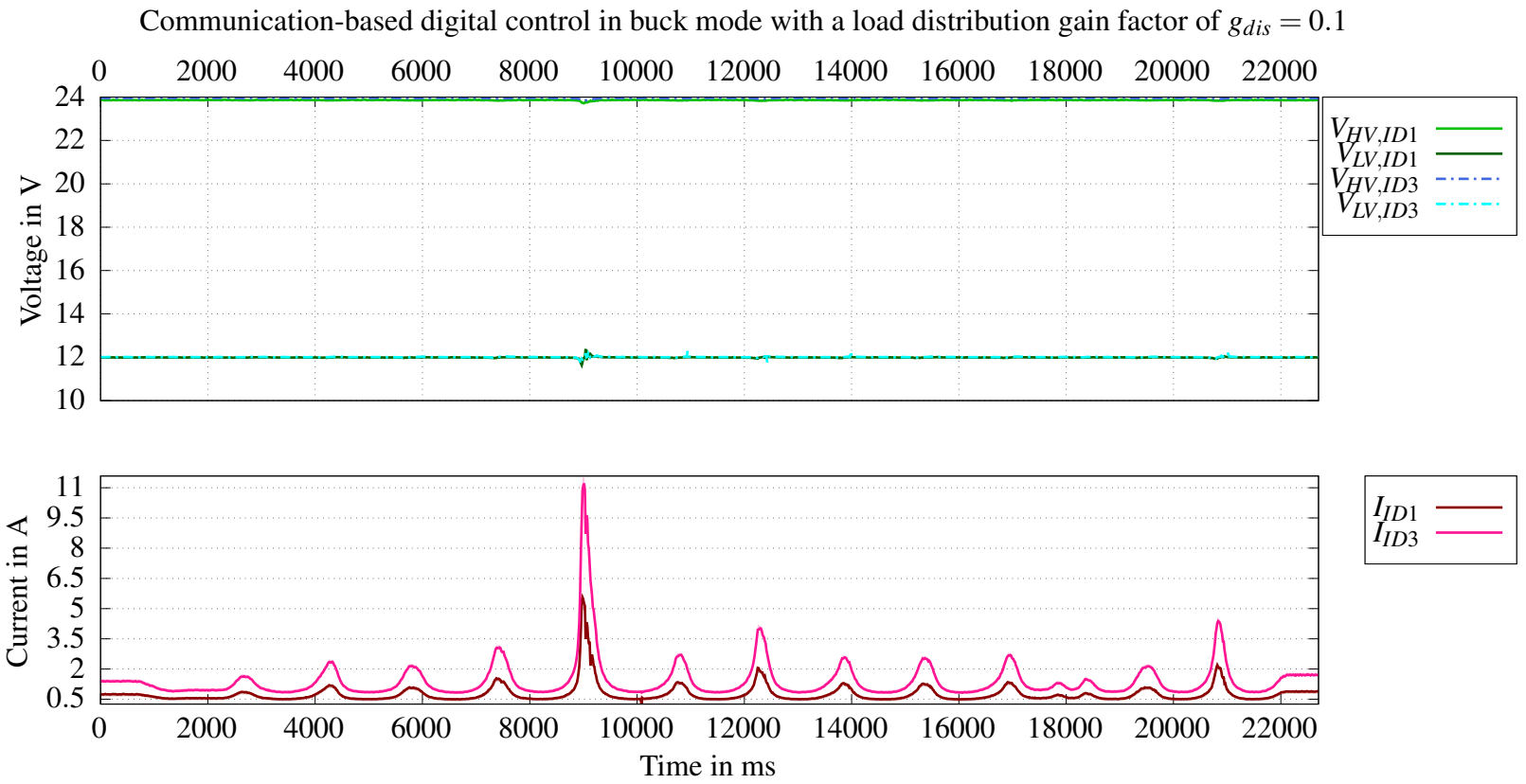


Figure 14.15: Load sharing between two DC-DC converters connected in parallel (ID 1, ID 3) operating in buck mode. The digital load distribution control is applied without using the FMAC. A fixed load distribution of 30% (ID 1) and 70% (ID 3) is selected. The gain factor of the load sharing (g_{dis}) is low and is 0.1. The accuracy of the load sharing increases with higher load currents. Even high load current jumps, such as 16.5 A at $t \approx 9\,s$ in this case, do not affect the voltage to be controlled (V_{LV}). An ohmic load is used.

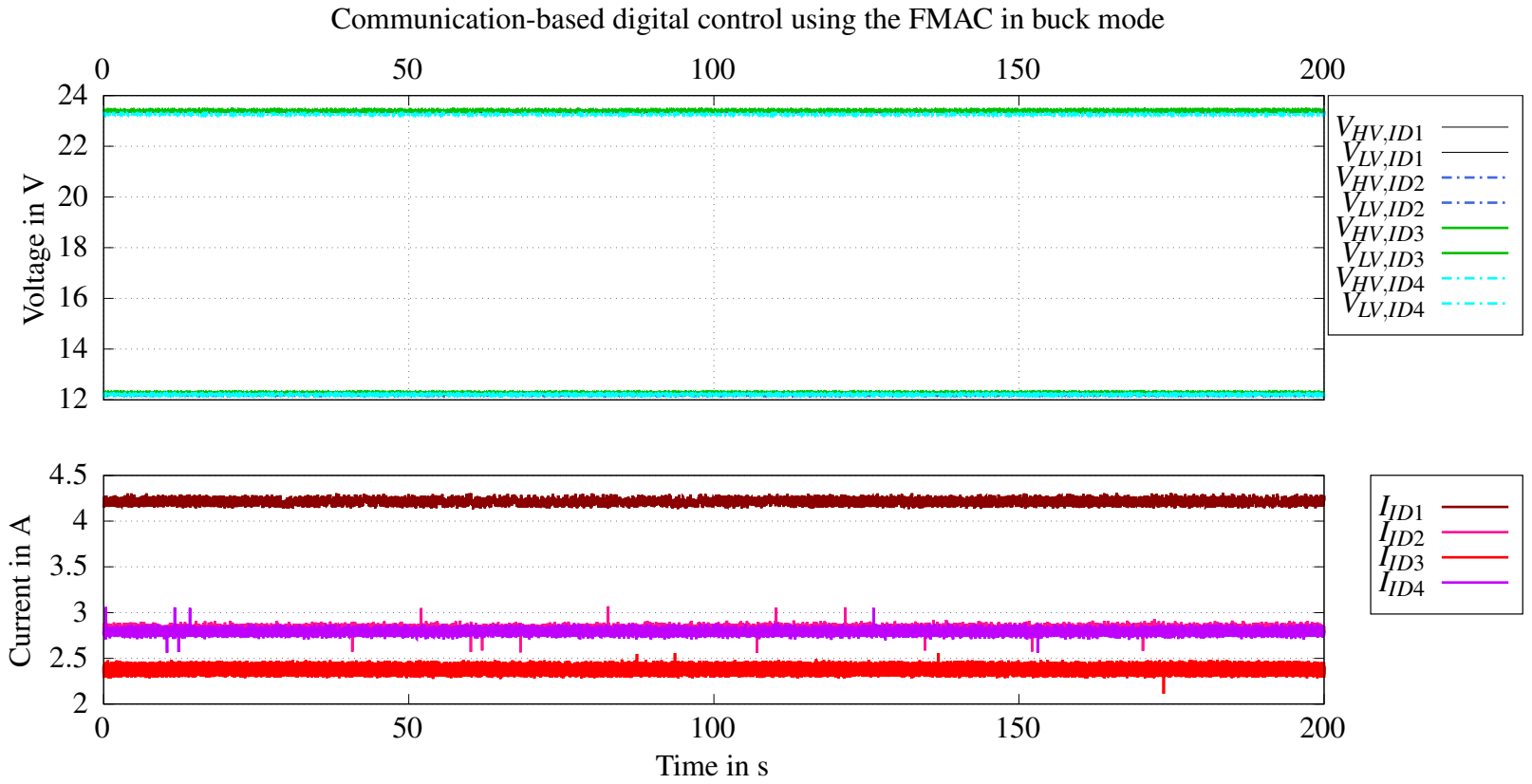


Figure 14.16: Four DC-DC converters in parallel are connected at the HV-side to an electronic load with a constant current of $12A$. For the control, the communication-based, digital one with FMAC and the following distribution factors is used $\alpha_{\text{ID1}} = 35\%$, $\alpha_{\text{ID2}} = 25\%$, $\alpha_{\text{ID3}} = 20\%$, $\alpha_{\text{ID4}} = 20\%$.

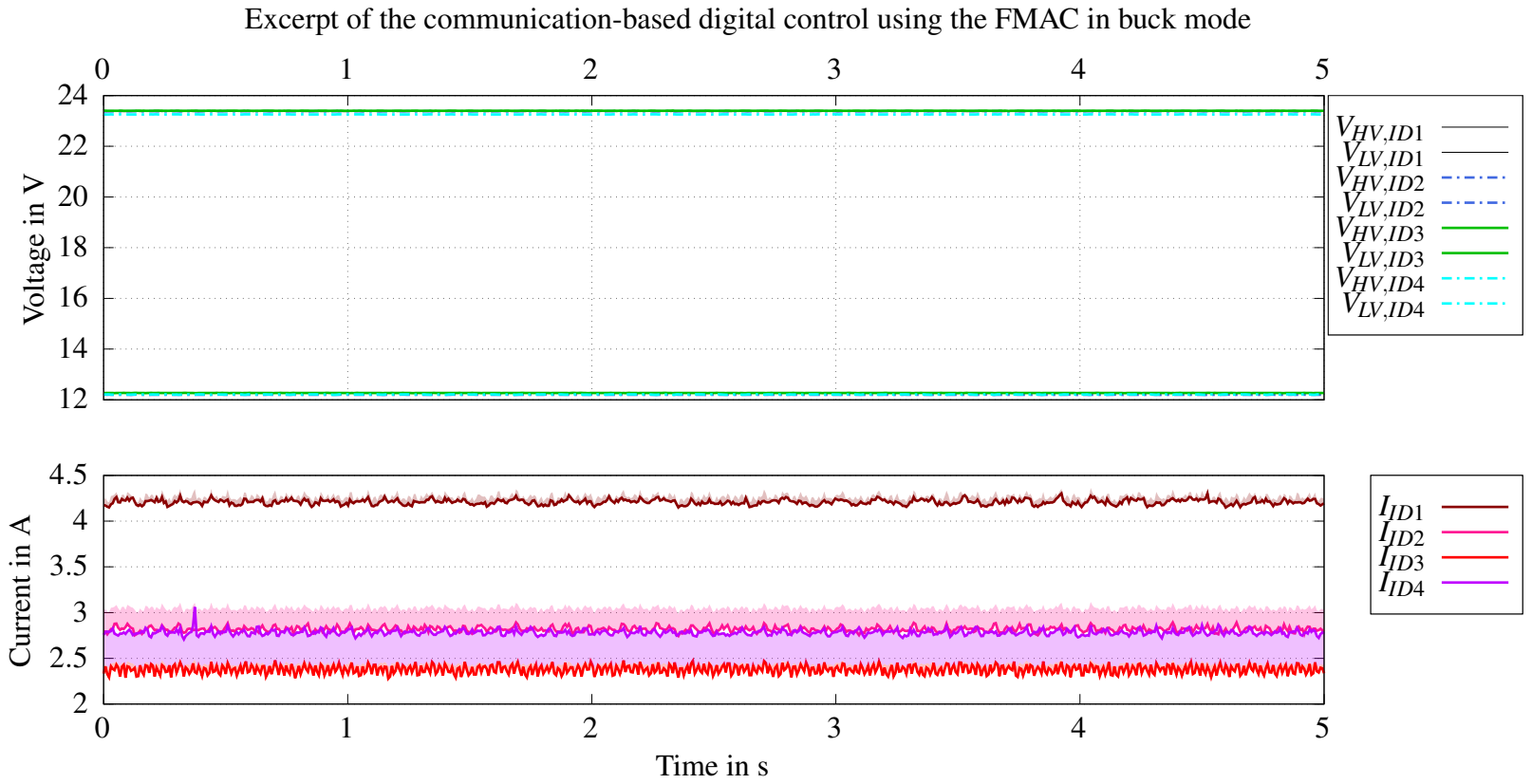


Figure 14.17: Excerpt of Fig. 14.16: Four DC-DC converters in parallel are connected at the HV-side to an electronic load with a constant current of $12A$. For the control, the communication-based, digital one with FMAC and the following distribution factors is used $\alpha_{\text{ID1}} = 35\%$, $\alpha_{\text{ID2}} = 25\%$, $\alpha_{\text{ID3}} = 20\%$, $\alpha_{\text{ID4}} = 20\%$.

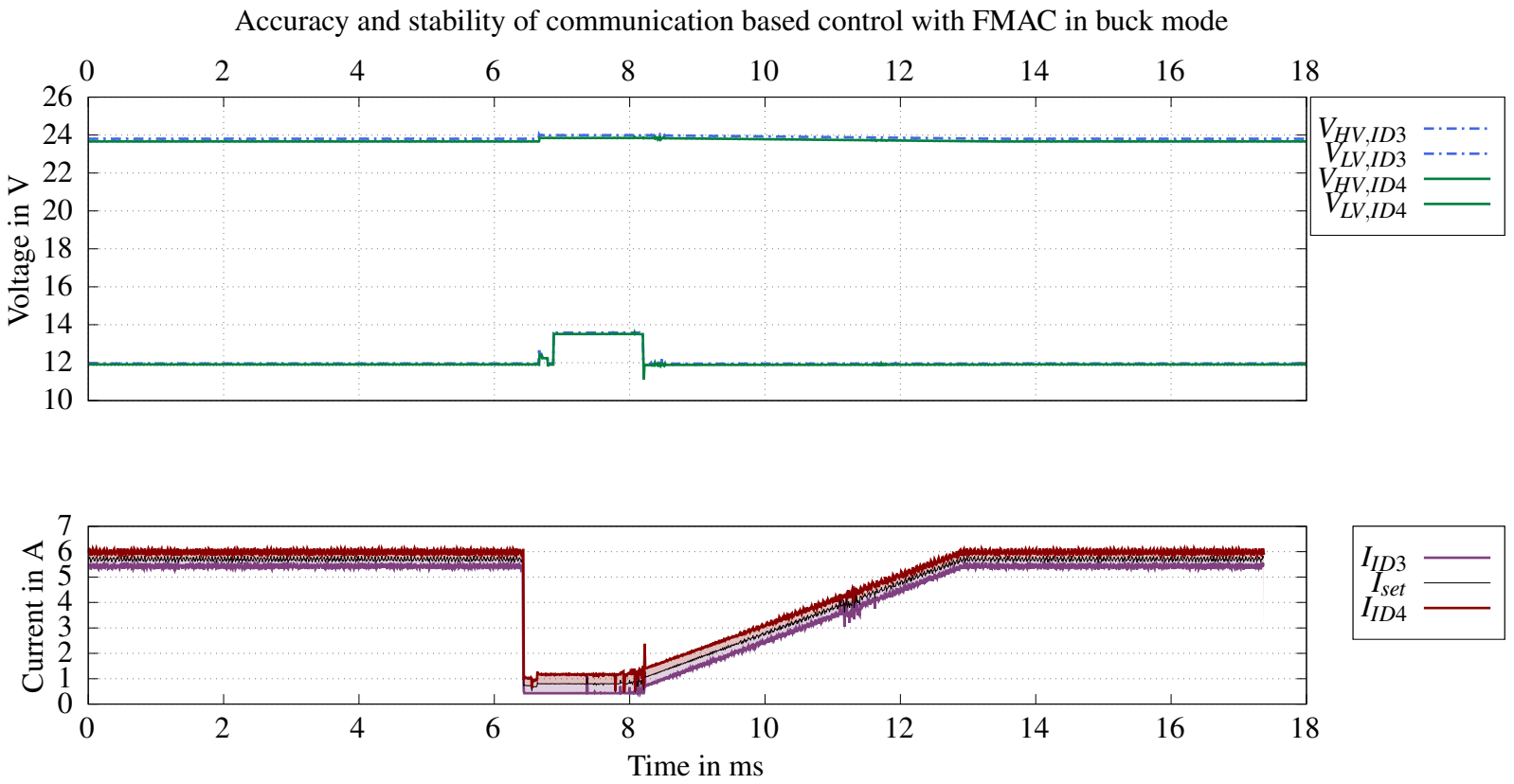


Figure 14.18: Two DC-DC converters operating in buck mode are connected at the LV-side with an electronic load which first generates a constant load current of $11A$, then suddenly drops to $3A$ and ramps up to $11A$ again. Communication-based, digital control with FMAC is used and an identical distribution factor of $\alpha = 50\%$. Deviations in the load current distribution occur over the entire load current range, with a maximum of 3% or $0.5A$. The load change from $11A$ to $3A$ at $t = 6.5s$ results in a voltage rise to a maximum of $13.6V$.

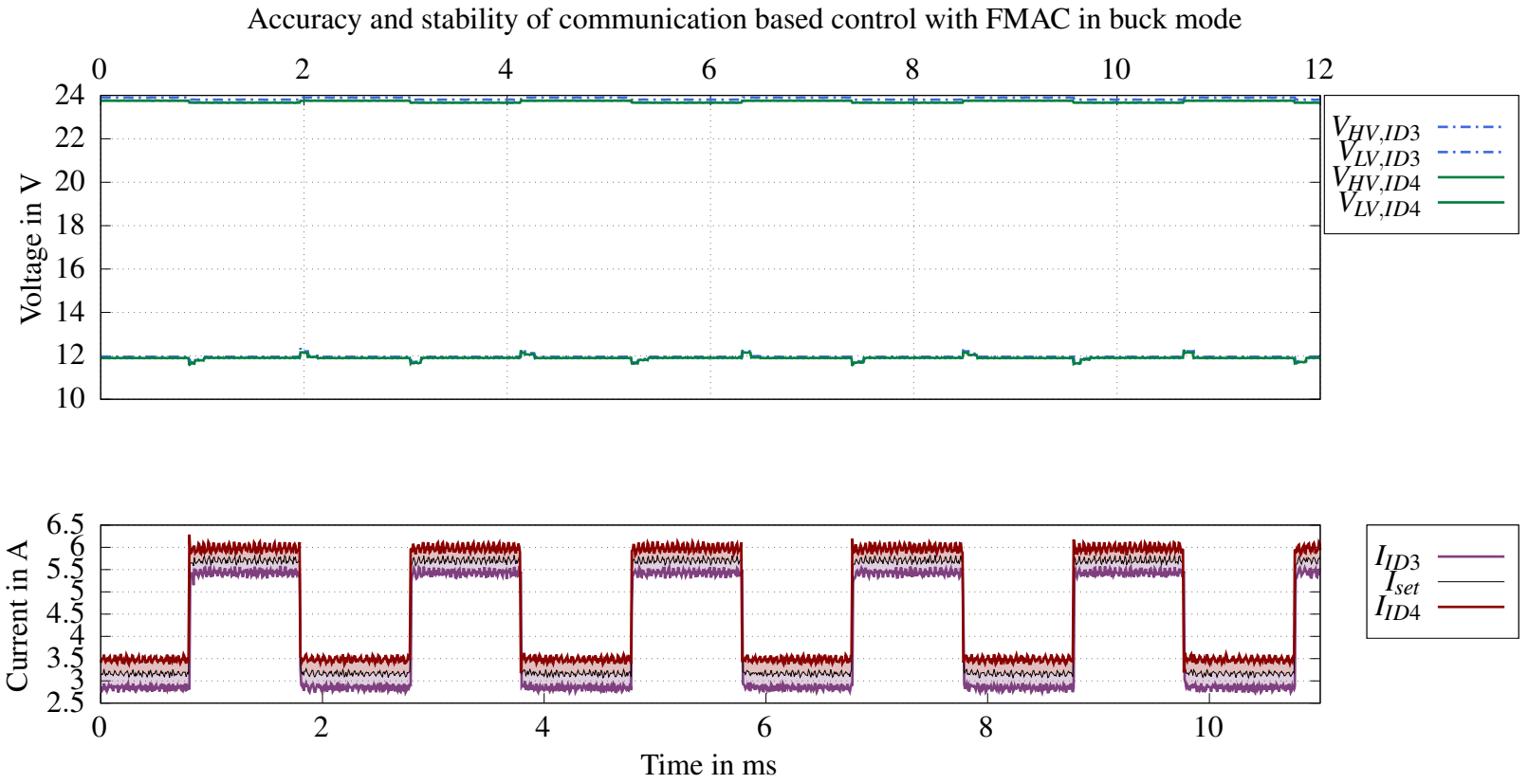


Figure 14.19: Two DC-DC converters operating in buck mode are connected at the LV-side with an electronic load which generates rectangular load steps between $63A$ and $13A$. Communication-based, digital control with FMAC and identical distribution factors of $\alpha = 50\%$ is used. Deviations in the load current distribution occur over the entire load current range, with a maximum of 3% or $0.5A$. When the load current value changes, voltage deviations of $\pm 0.3V$ occur.

14.3.4 Change of the Load Distribution Factors

For a load distribution control with distribution factors in accordance to the battery state, it is an essential requirement that the distribution factors can be changed during active operation via communication without significantly affecting the control stability of the system. In the following, the change of the load distribution factors in the communication-based digital control using the FMAC unit is analyzed starting with the boost mode and followed by the buck mode.
Figure 14.20 on p. 298 shows the measurement of four DC-DC converters connected in parallel operating in boost mode, which are connected on the HV-side with an electronic load generating a constant load current of $11\,A$. Initially, the distribution factors are $\alpha_{\mathrm{ID1}} = 70\%$, $\alpha_{\mathrm{ID2}} = 10\%$, $\alpha_{\mathrm{ID3}} = 10\%$, $\alpha_{\mathrm{ID4}} = 10\%$. At time $t = 42.9\,s$ they are changed to $\alpha = 25\%$ each and at time $t = 60.7\,s$ to $\alpha_{\mathrm{ID1}} = 20\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 5\%$, $\alpha_{\mathrm{ID4}} = 50\%$. The current changes without significant delay in the event of a distribution factor change and the current deviations are small. The voltage to be regulated is slightly too high at the beginning with a value of $24.2\,V$. All deviations are within the acceptable range.
Four DC-DC converters connected in parallel operate in boost mode and are connected at the HV-side to an electronic load which generates a rectangular load current of $6\,A$ and $13\,A$ (Fig. 14.21 on p. 299). Initially, all distribution factors are identical and equal to $\alpha = 25\%$. At time $t = 9.2\,s$, the value of the distribution factors changes to $\alpha_{\mathrm{ID1}} = 15\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 5\%$, $\alpha_{\mathrm{ID4}} = 50\%$. The quantization errors that occur when using the FMAC and their effects on the output currents are evident. The voltage to be controlled (V_{HV}) remains stable. Fluctuations on the LV-side are due to interferences between the electronic load and supply. In this case, it clearly shows that an improved procedure to reduce the quantization errors when using the FMAC unit should be considered in future work. The output current fluctuations are significant and too high to further ensure an acceptable operation of the batteries with regard of aging accelerated operating states. Nevertheless, the change of the distribution factors can be validated even with a rectangular load current. The distribution according to the updated factors occurs without noticeable delay and without overshoot. The change still has no effect on the voltage to be controlled.
The measurement of four parallel DC-DC converters in buck mode, which are connected at the LV-side to an electronic load with a constant load current of $14\,A$, is presented in figure 14.22 on p. 300. At the beginning, the distribution factors are $\alpha_{\mathrm{ID1}} = 20\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 35\%$, $\alpha_{\mathrm{ID4}} = 20\%$. At $t = 11\,s$, they are changed to $\alpha_{\mathrm{ID1}} = 10\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 5\%$, $\alpha_{\mathrm{ID4}} = 60\%$. The change has no effect on the voltage to be controlled and the deviations in the load current sharing are marginal, but increasing with lower output current values. In this case, too, the distribution according to the updated factors is performed without noticeable delay and without overshoot.

Conclusion

The change of the load distribution factors during active operation with communication-based digital load distribution control using the FMAC unit was successfully validated in boost and buck mode. The update of the distribution factors leads to the change of the load current distribution without noticeable delays. No overshoot occurs and the voltage to be controlled remains stable. The quantization

errors caused by the FMAC unit are clearly visible and have to be addressed in future work by appropriate methods.

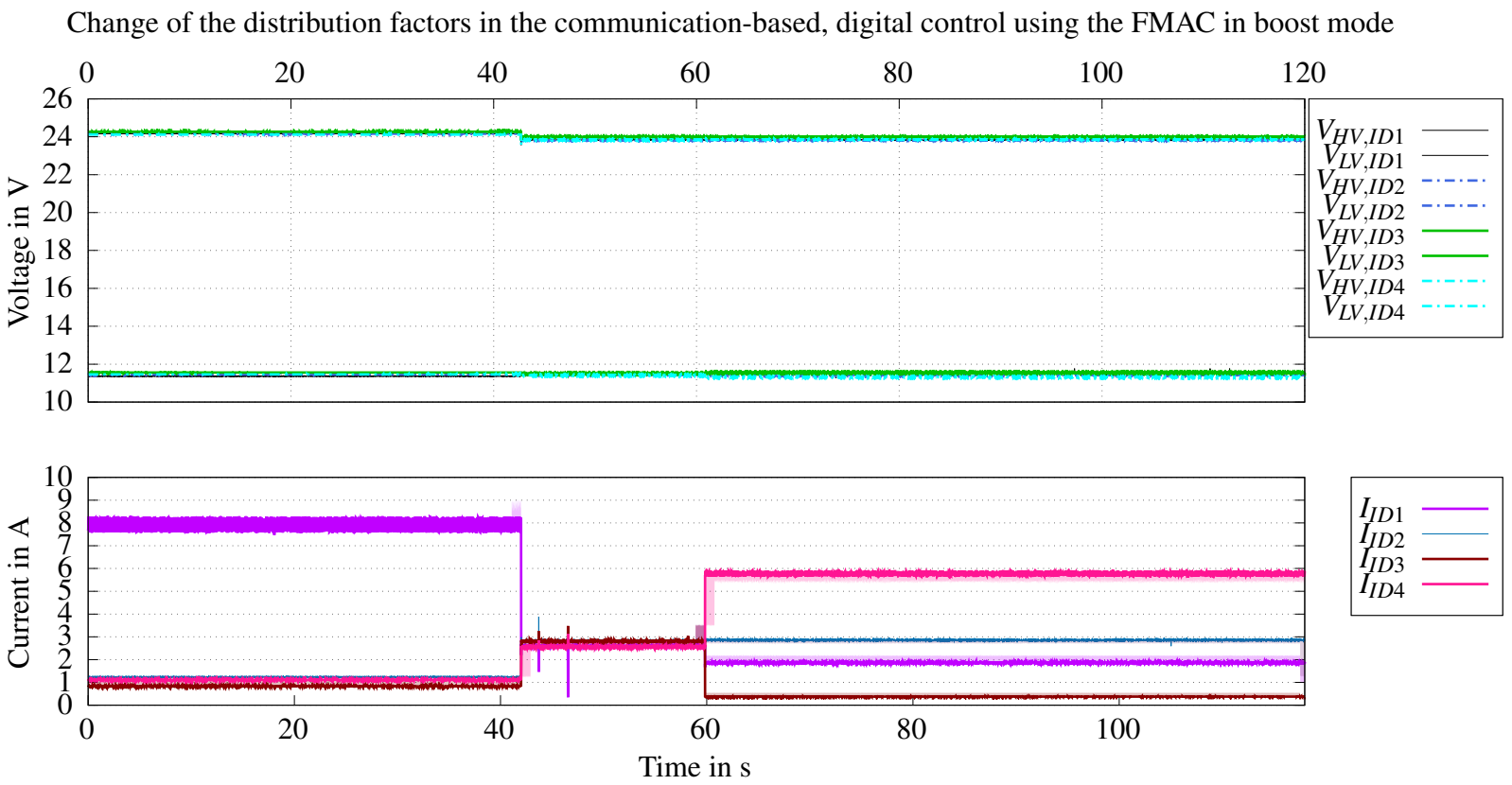


Figure 14.20: Four DC-DC converters connected in parallel operate in boost mode and are connected on the HV-side with an electronic load which generates a load current of $11A$. Communication-based digital control is used and the values of the distribution factors are changed. Initially, the distribution factors are $\alpha_{\text{ID1}} = 70\%$, $\alpha_{\text{ID2}} = 10\%$, $\alpha_{\text{ID3}} = 10\%$, $\alpha_{\text{ID4}} = 10\%$. At time $t = 42.9\,s$ they are changed to $\alpha = 25\%$ each and at time $t = 60.7\,s$ to $\alpha_{\text{ID1}} = 20\%$, $\alpha_{\text{ID2}} = 25\%$, $\alpha_{\text{ID3}} = 5\%$, $\alpha_{\text{ID4}} = 50\%$. The current changes without significant delay and the deviations are small.

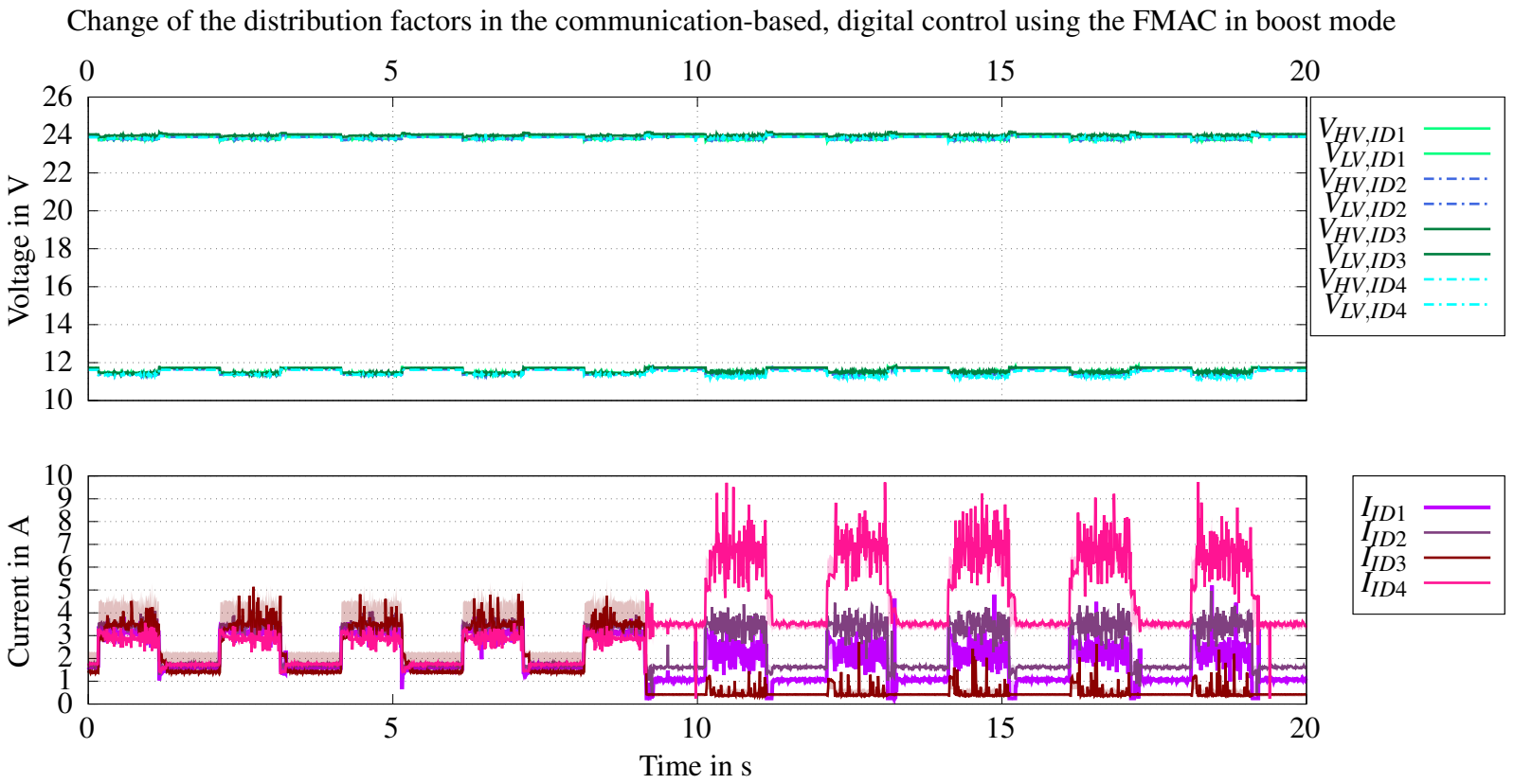


Figure 14.21: Four DC-DC converters connected in parallel operate in boost mode and are connected at the HV-side to an electronic load which generates a rectangular load current of $6A$ and $13A$. For the control, the communication-based digital one with FMAC is used. Initially, all distribution factors are identical and equal to $\alpha = 25\%$. At time $t = 9.2s$, the value of the distribution factors changes to $\alpha_{\mathrm{ID1}} = 15\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 7\%$, $\alpha_{\mathrm{ID4}} = 53\%$. The quantization errors that occur when using the FMAC and their effects on the output currents are evident. The voltage to be controlled (V_{HV}) remains stable. Fluctuations on the LV-side are due to interferences between the electronic load and supply.

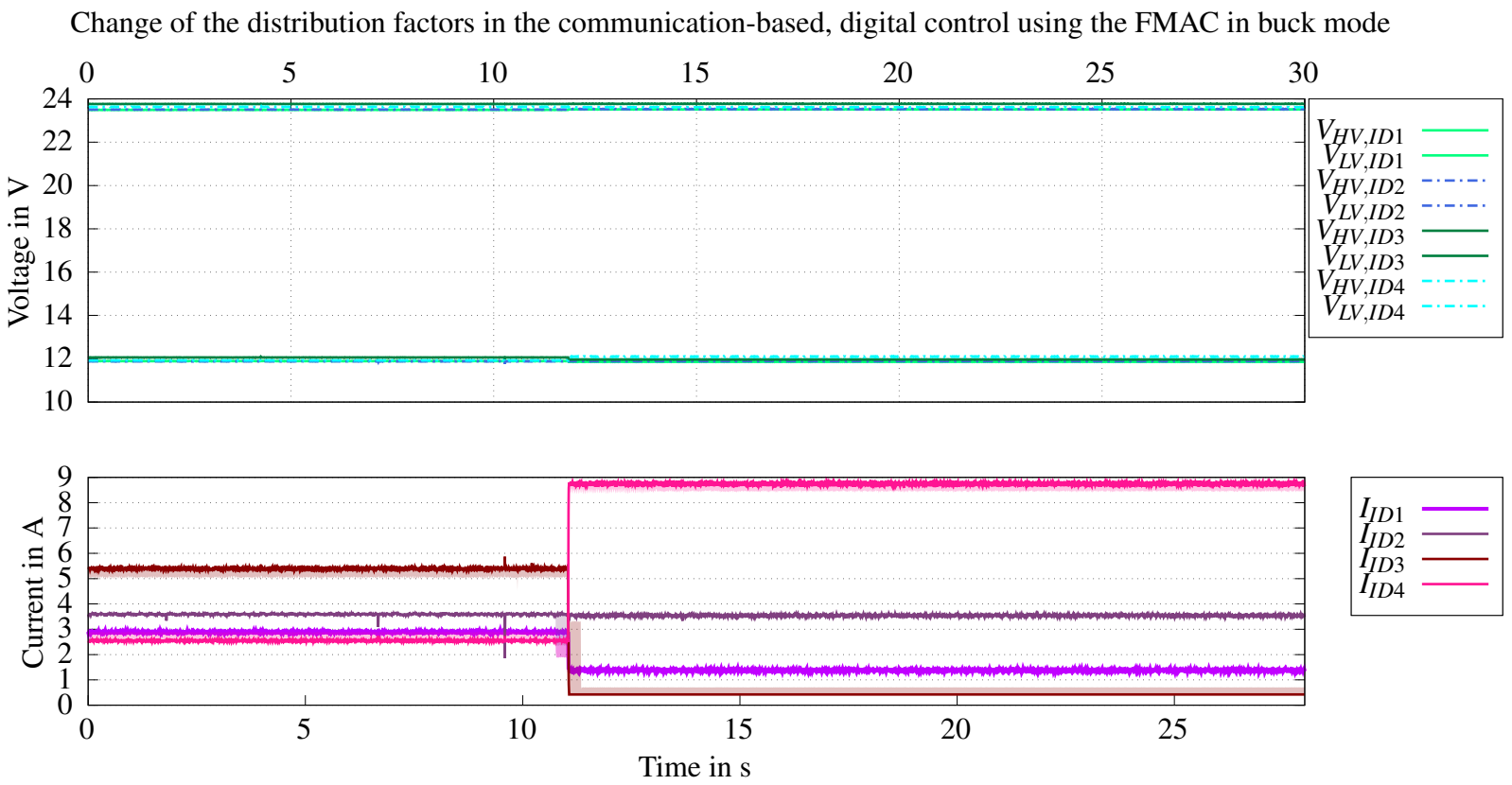


Figure 14.22: Four parallel DC-DC converters in buck mode are connected at the LV-side to an electronic load with a constant load current of $14A$. The communication-based digital control with FMAC is used for the control. At the beginning, the distribution factors are $\alpha_{\mathrm{ID1}} = 20\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 35\%$, $\alpha_{\mathrm{ID4}} = 20\%$. At $t = 11\,s$, they are changed to $\alpha_{\mathrm{ID1}} = 10\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 5\%$, $\alpha_{\mathrm{ID4}} = 60\%$. The change has no effect on the voltage to be controlled and the deviations in the load current distribution are marginal, but increasing with lower output current values.

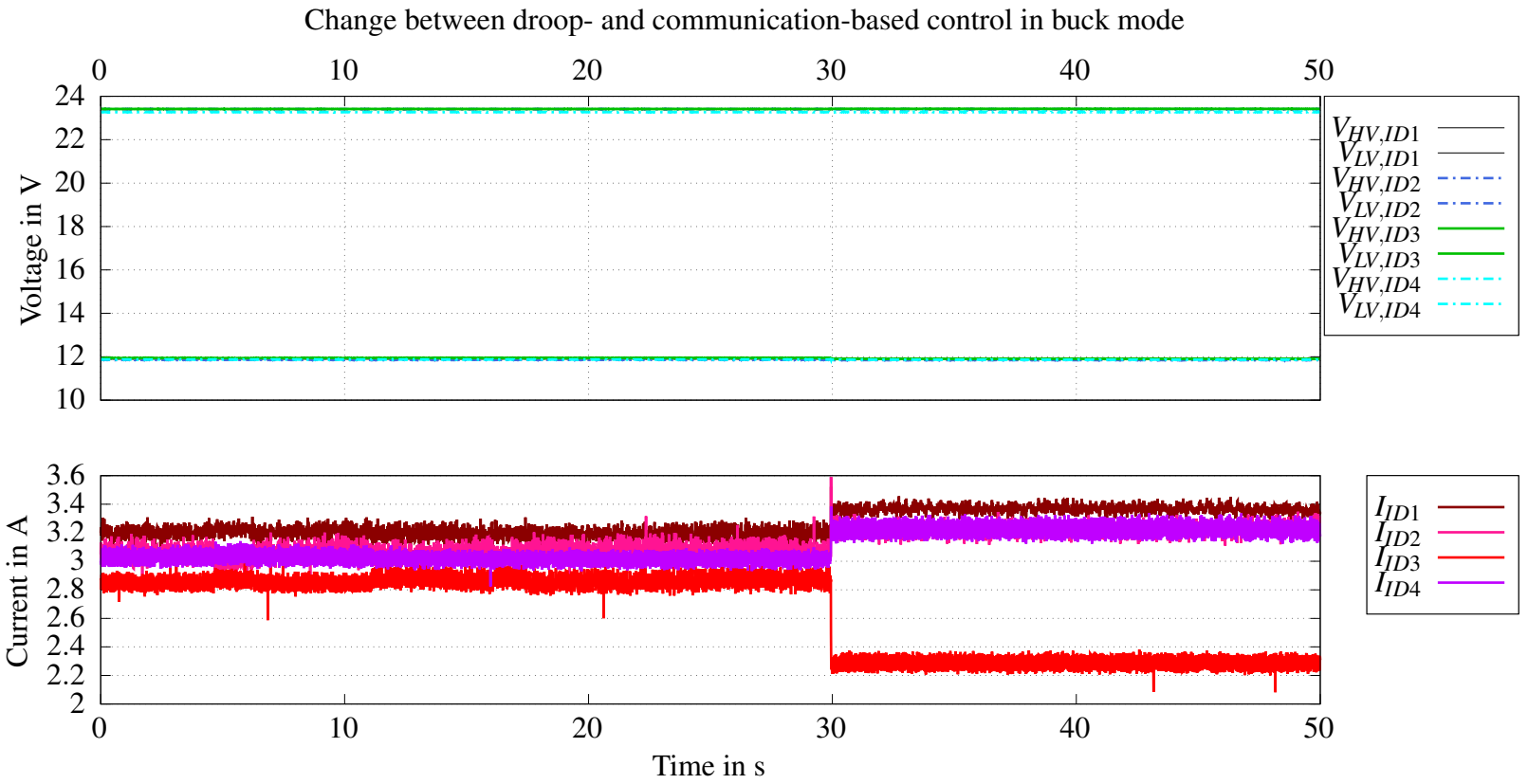


Figure 14.23: Four DC-DC converters connected in parallel are connected at the HV-side to an electronic load with a constant load current of $12A$. Initially up to $t = 30\,s$ the DC-DC converters operate in the droop-based control with adjusted reference voltages and identical droop resistors. After that they change to the communication-based, digital control using the FMAC with a load sharing of $\alpha_{\mathrm{ID1}} = 30\%$, $\alpha_{\mathrm{ID2}} = 25\%$, $\alpha_{\mathrm{ID3}} = 20\%$, $\alpha_{\mathrm{ID4}} = 25\%$. The change between the two control methods does not affect the voltage to be controlled (V_{HV}).

14.4 Selection of Specific Use Cases

After successful validation of the droop-based, the communication-based with and without FMAC during normal operation in buck and boost mode, a selection of specific application cases is considered in the following. First, the startup of the system, which is always performed with the droop-based control, is investigated. The change from the droop-based to the communication-based control is analyzed and it is examined whether the big leader election process has an influence on the control. Subsequently, the influence of an erroneous voltage measurement, an incorrect total current measurement and the deactivation of a DC-DC converter on the control is investigated.

14.4.1 System Start-up and Change between Droop-based and Communication-based Control

At system startup, the droop-based control is always used and the big leader election process is started after a random waiting time has elapsed. The control objective is to bring the DC link voltage as quickly as possible to the setpoint, which is $24\,V$ in the following cases. At the same time it is necessary to distribute the load current between the DC-DC converters. The DC-DC converters thereby operate in boost mode.
Figure 14.24 on p. 304 shows the start-up of the system with four DC-DC converters operating in boost mode with droop-based control. The test setup according to figure 14.2 was used, where only the droop-based control was selected by respective software changes to allow a detailed investigation of the droop-based control. The droop resistors used are identical ($R_\mathrm{d} = 0.1\,\Omega$) and individual output characteristics ($V_\mathrm{ref,ID1} = 2\,V$, $V_\mathrm{ref,ID2} = 1.87\,V$, $V_\mathrm{ref,ID3} = 2.02\,V$, $V_\mathrm{ref,ID3} = 2\,V$) are considered. The DC-DC converter ID1 has an incorrect LV voltage measurement, whereby the LV voltage does not play a role in the control when operating in boost mode. The output current of the DC-DC converter ID 1 exhibits an overshoot of about $0.5\,A$. A possible reason for this is that the DC-DC converters are not started simultaneously. In this case, the DC-DC converter ID 1 starts first and measures the largest deviation in comparison to the remaining ones started slightly later. The setpoint of the DC link voltage is reached almost immediately but definitely without significant delay and without overshoot and the load is divided between the DC-DC converters. The load distribution shows significant deviations but the objective that not one single DC-DC converter supplies the entire load current and is thus heavily loaded is achieved.
In figure 14.25 on p. 305 the measurement of th start-up of the system consisting of four parallel connected DC-DC converters and an electronic load at the HV-side which generates a ramped load current (0 to $10\,A$ in $5\,s$) is presented. The test setup according to figure 14.2 was used, an the normal software was executed. This means, that the DC-DC converter first operate in boost mode using the droop-based control, while they are sending messages containing the relevant information for the leader election process. After a random waiting time has elapsed, which has been increased on purpose for the measurements, the big leader election process is started and a leader, an assistant and a co-assistant is elected. After that, the DC-DC converter change to the communication-based, digital control with FMAC. In this case identical droop resistors ($R_\mathrm{d} = 0.1\,\Omega$) and individual output characteristics ($V_\mathrm{ref,ID1} = 2\,V$, $V_\mathrm{ref,ID2} = 1.87\,V$, $V_\mathrm{ref,ID3} = 2.02\,V$, $V_\mathrm{ref,ID3} = 2\,V$) are used in the droop-based control.

At approximately $t = 17.8\,s$ the leader election process is finished and the DC-DC converter change to the communication-based, digital control with FMAC. The distribution factors are initially all identical and equal to $\alpha = 25\%$. At $t = 40\,s$ they are changed to $\alpha_{\mathrm{ID1}} = 30\%$, $\alpha_{\mathrm{ID2}} = 20\%$, $\alpha_{\mathrm{ID3}} = 25\%$, $\alpha_{\mathrm{ID4}} = 25\%$. Even with the activation of all software processes and a running election process, the HV-voltage setpoint is controlled stably and load distribution between the DC-DC converters is realized. The change between the droop-based and the communication-based control takes place without any effect on the control stability.
Since the switch between droop and communication-based control is difficult to detect when identical droop resistors and initially identical distribution factors are selected, another measurement is made to analyze the switching process using different droop resistors. Figure 14.26 on p. 306 shows the measurement recorded during a switch of the control methods for four parallel connected DC-DC converters operating in boost mode. At the HV-side an electronic load which generates rectangular load steps between $6A$ and $13A$ is connected. Initially, the DC-DC converters operate in droop mode with adjusted reference voltages and different droop resistors ($R_{\mathrm{d,ID1}} = 0.1\,\Omega$,$V_{\mathrm{ref,ID1}} = 2V$, $R_{\mathrm{d,ID2}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID2}} = 1.87V$, $R_{\mathrm{d,ID3}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID3}} = 2.02V$, $R_{\mathrm{d,ID4}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID4}} = 2V$). Afterwards they switch to digital control with FMAC with identical division factors of $\alpha = 25\%$. Fluctuations on the LV-side occur due to interference between the electronic supply and load. The HV-voltage to be controlled remains stable with a single exception of an overshoot with the value $25.5\,V$ at the time of the switch between droop- and communication-based control.

Conclusion

The start-up of the system with using the droop-based control only and with the additional activation of all software processes were both successfully validated.
The step response of the system start-up with the droop control shows no considerable overshoot. The DC link voltage setpoint is reached almost instantaneously while distributing the total current between the DC-DC converters. The big leader election process performed at system start-up shows no effect and the switch between droop-based and communication-based control is performed without any significant impact on the control stability and accuracy.

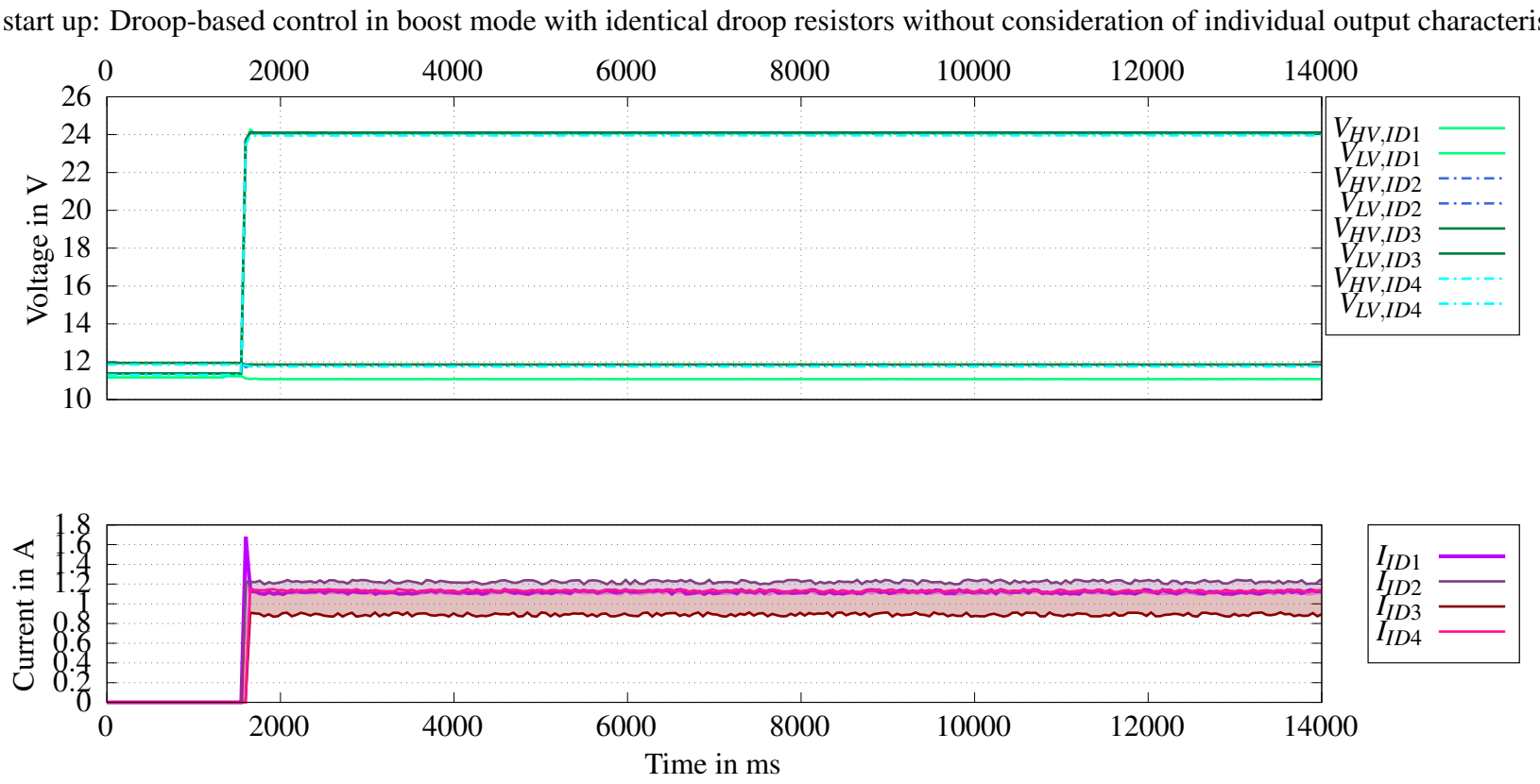


Figure 14.24: Start-up of the system with four DC-DC converters operating in boost mode with droop-based control. The droop resistors used are identical ($R_\mathrm{d} = 0.1\,\Omega$) and individual output characteristics ($V_\mathrm{ref,ID1} = 2\,V$, $V_\mathrm{ref,ID2} = 1.87\,V$, $V_\mathrm{ref,ID3} = 2.02\,V$, $V_\mathrm{ref,ID3} = 2\,V$) are considered. The DC-DC converter ID1 has an incorrect LV voltage measurement. The output current of the DC-DC converter ID 1 exhibits an overshoot of about $0.5\,A$. A possible reason for this is that the DC-DC converters are not started simultaneously. In this case, the DC-DC converter ID 1 starts first and measures the largest deviation in comparison to the remaining ones started slightly later.

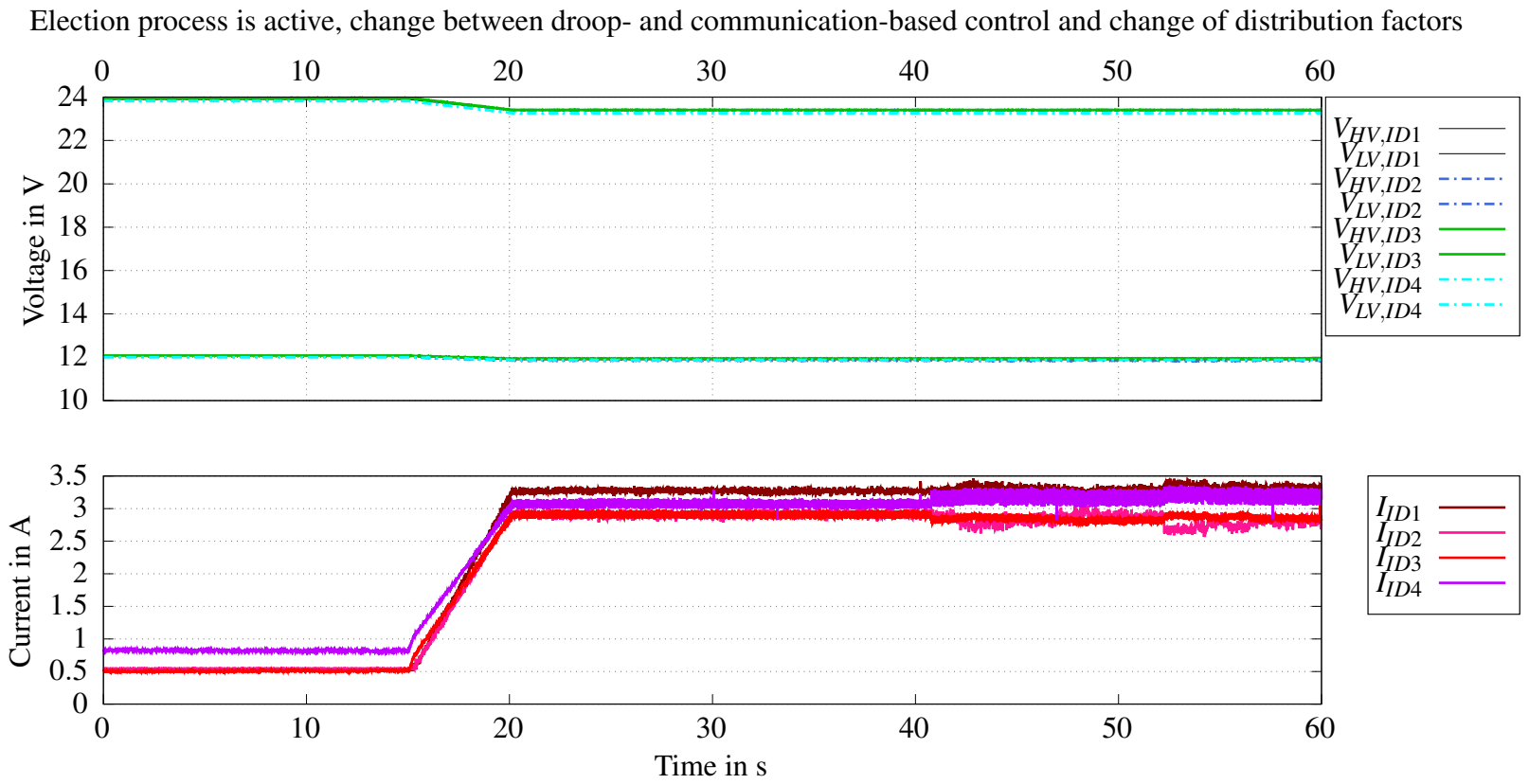


Figure 14.25: Start-up of the system consisting of four parallel connected DC-DC converters and an electronic load at the HV-side which generates a ramped load current (0 to 10A in 5s). The election process was completed approximately at $t = 17\,s$ and the control scheme switched from droop to communication-based control. The distribution factors are initially all identical and equal to $\alpha = 25\%$. At $t = 40\,s$ they are changed to $\alpha_{\mathrm{ID1}} = 30\%$, $\alpha_{\mathrm{ID2}} = 20\%$, $\alpha_{\mathrm{ID3}} = 25\%$, $\alpha_{\mathrm{ID4}} = 25\%$. For the digital control, the FMAC of the microcontroller is used.

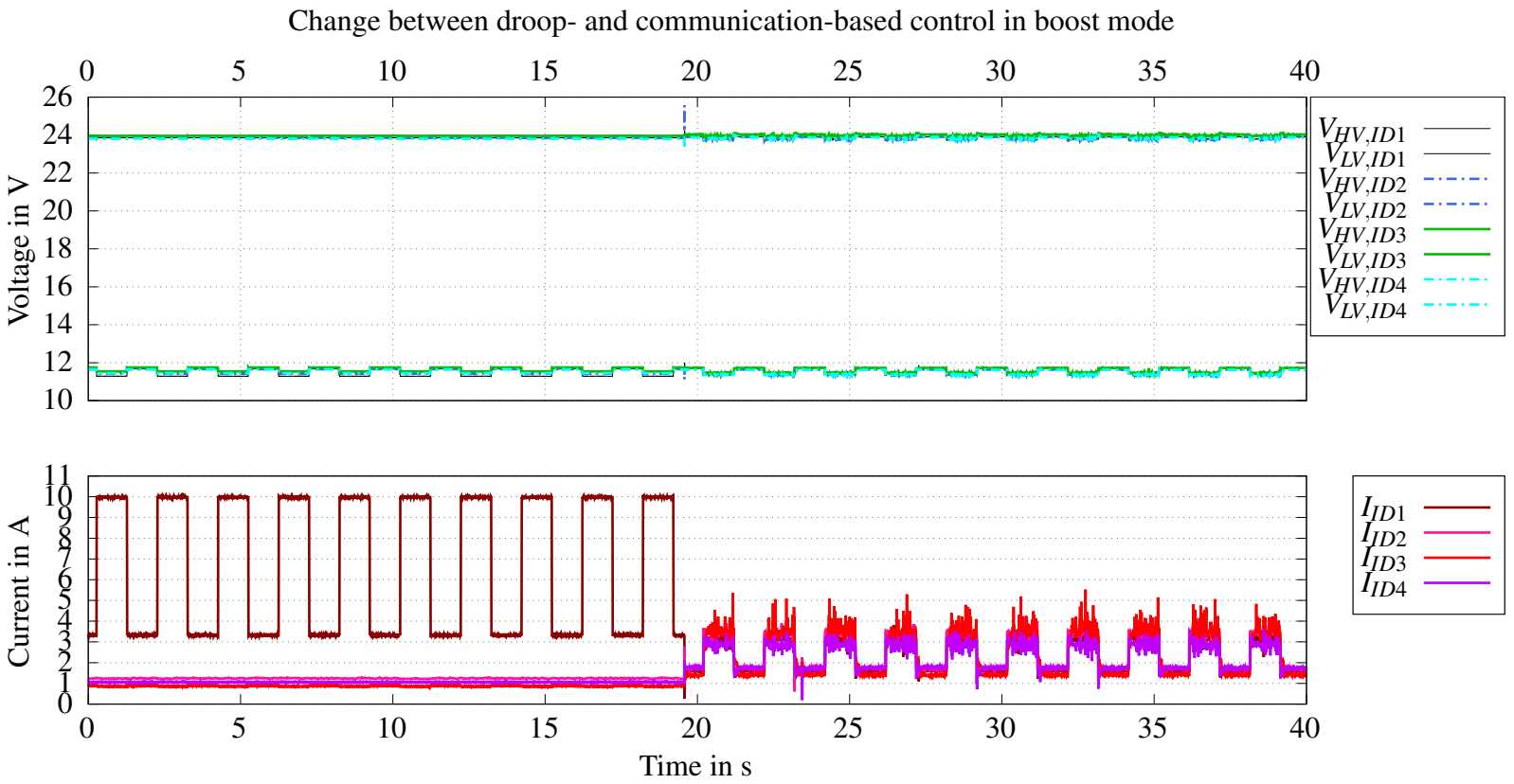


Figure 14.26: Four parallel DC-DC converters operating in boost mode are connected at the HV-side with an electronic load which generates rectangular load steps between $6A$ and $13A$. Initially, the DC-DC converters operate in droop mode with adjusted reference voltages and different droop resistors ($R_{\mathrm{d,ID1}} = 0.1\,\Omega$, $V_{\mathrm{ref,ID1}} = 2V$, $R_{\mathrm{d,ID2}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID2}} = 1.87V$, $R_{\mathrm{d,ID3}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID3}} = 2.02V$, $R_{\mathrm{d,ID4}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID4}} = 2V$). Afterwards they switch to digital control with FMAC with identical division factors of $\alpha = 25\%$. Fluctuations on the LV-side occur due to interference between the electronic supply and load.

14.4.2 Selection of Test Cases for Analyzing Robustness

One of the design goals of the DBMS is robustness, i.e. the control stability and accuracy in case of disturbances like missing or erroneous measurements or failure of single components. In the following, two cases are considered to validate initial robustness investigations. First, the influence of an erroneous voltage measurement of an LCU as well as the abrupt deactivation of an LCU is examined. The influence of an erroneous total current measurement in the communication-based control is investigated thereafter.
In figure 14.27 on p. 309 the measurement of four parallel connected DC-DC operating in buck mode with a wrong LV-measurement of the LCU with the ID 1 and an abrupt deactivation of the LCU with the ID 2 is shown. The droop-based control with adapted droop resistors and reference voltages is used with the following setting: $R_{\mathrm{d,ID1}} = 0.7\,\Omega$,$V_{\mathrm{ref,ID1}} = 2\,V$, $R_{\mathrm{d,ID2}} = 0.3\,\Omega$,$V_{\mathrm{ref,ID2}} = 1.87\,V$, $R_{\mathrm{d,ID3}} = 1.2\,\Omega$,$V_{\mathrm{ref,ID3}} = 2.02\,V$, $R_{\mathrm{d,ID4}} = 0.7\,\Omega$,$V_{\mathrm{ref,ID4}} = 2\,V$. The LV-measurement of the DC-DC converter ID 1 is incorrect with an average offset of $-1.4\,V$. The DC-DC converters work in buck mode and the faulty LV voltage influences the output of the DC-DC converter with the ID 1. It can be seen that the individual output characteristics of the DC-DC converters have not yet been optimally considered. The DC-DC converters with the ID 1 and ID 4 have identical droop resistances, whereby the LCU ID 1 consistently detects a higher deviation due to the erroneous LV measurement. A higher deviation results in higher output currents. In this case, nevertheless, the DC-DC converter with the ID 4 still takes over a higher portion of the load current. The voltage control of the LV-voltage remains stable despite the erroneous measurement, even if deviations occur in the load current distribution. The DC-DC converter ID 2 is deactivated at $t = 19.54\,s$ and the remaining ones take over the load current. No significant voltage (V_{LV}) changes occur in response to the deactivation of the DC-DC converter.
The effects of a faulty total current measurement are demonstrated in the measurements in figure 14.28 on p. 310. The three DC-DC converters operating in buck mode are connected in parallel and use the communication-based digital control with direct calculation by the microcontroller with an erroneous fixed value for the total current of $2A$. The division factors are identical with the value 33%. An electronic load connected at the LV-side is generating rectangular load jumps between $5\,A$ and $8\,A$. The voltage control to the set point shows no significant deviation proofing that the voltage control is independent of the load current distribution control. As expected, the load current distribution shows significant deviations. The load current is, however, still distributed between the components. The DC-DC converters with the ID 2 and ID 4 supply a much larger current than defined by their distribution factors, while the DC-DC converter with the ID 3 delivers a much lower one. Possible reasons for this are the measuring times of the individual LCUs or the different output characteristics. A future analysis to explain this load distribution is advisable for a future work.

Conclusion

Both the droop- and the communication-based control were successfully validated in terms of robustness for the selected failure cases.
The droop-based control is the preferred control strategy in case of communication failure, a deactivated leader and faulty measurements. Erroneous individual

measurements, such as the LV-voltage in this case, or unannounced deactivation of a component had no discernible effect on the control stability and accuracy of the voltage control. Load sharing was performed, again showing that detailed adjustment according to the individual output characteristics should be considered in future work. The communication-based control is used in normal operation. In the measurements of individual nodes, fault detection by other nodes can be effectively implemented. However, the total current is currently measured by only two sensors. Therefore, the effect of a faulty total current measurement was analyzed. It was found that regulation to the voltage setpoint occurs without degradation. The total load current was still divided between the DC-DC converters, but with deviations. With the identical distribution factors selected, the DC-DC converters took over partly less and partly more load current. The analysis of the reasons for this is part of future work.

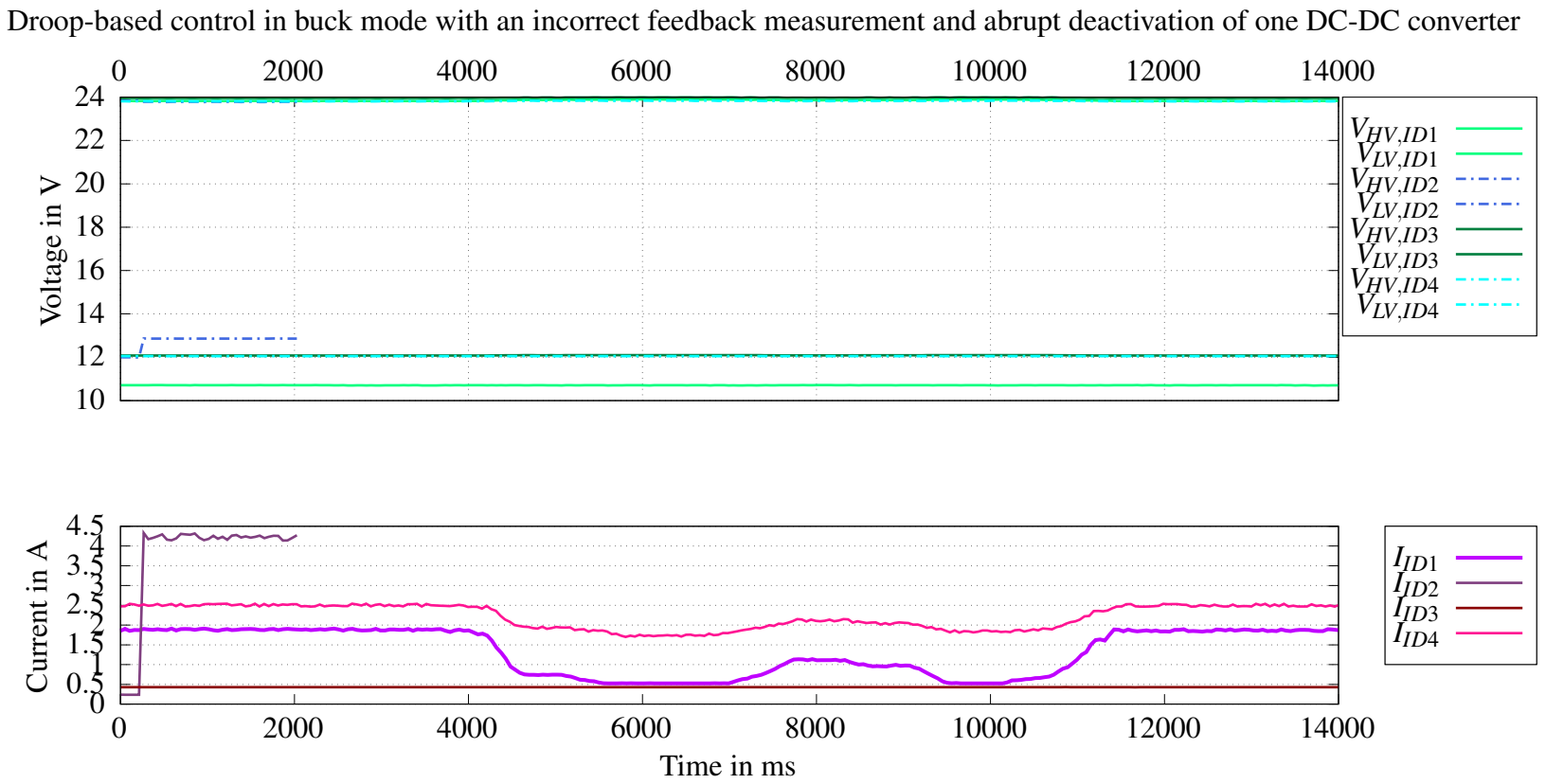


Figure 14.27: Parallel connection of four DC-DC converters operating in buck mode. The droop-based control with adapted droop resistors and reference voltages is used ($R_{\mathrm{d,ID1}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID1}} = 2V$, $R_{\mathrm{d,ID2}} = 0.3\,\Omega$, $V_{\mathrm{ref,ID2}} = 1.87V$, $R_{\mathrm{d,ID3}} = 1.2\,\Omega$, $V_{\mathrm{ref,ID3}} = 2.02V$, $R_{\mathrm{d,ID4}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID4}} = 2V$). The DC-DC converter ID 2 is deactivated and the remaining ones take over the load current. No significant voltage (V_{LV}) changes occur. The LV-measurement of the DC-DC converter 1 is incorrect.

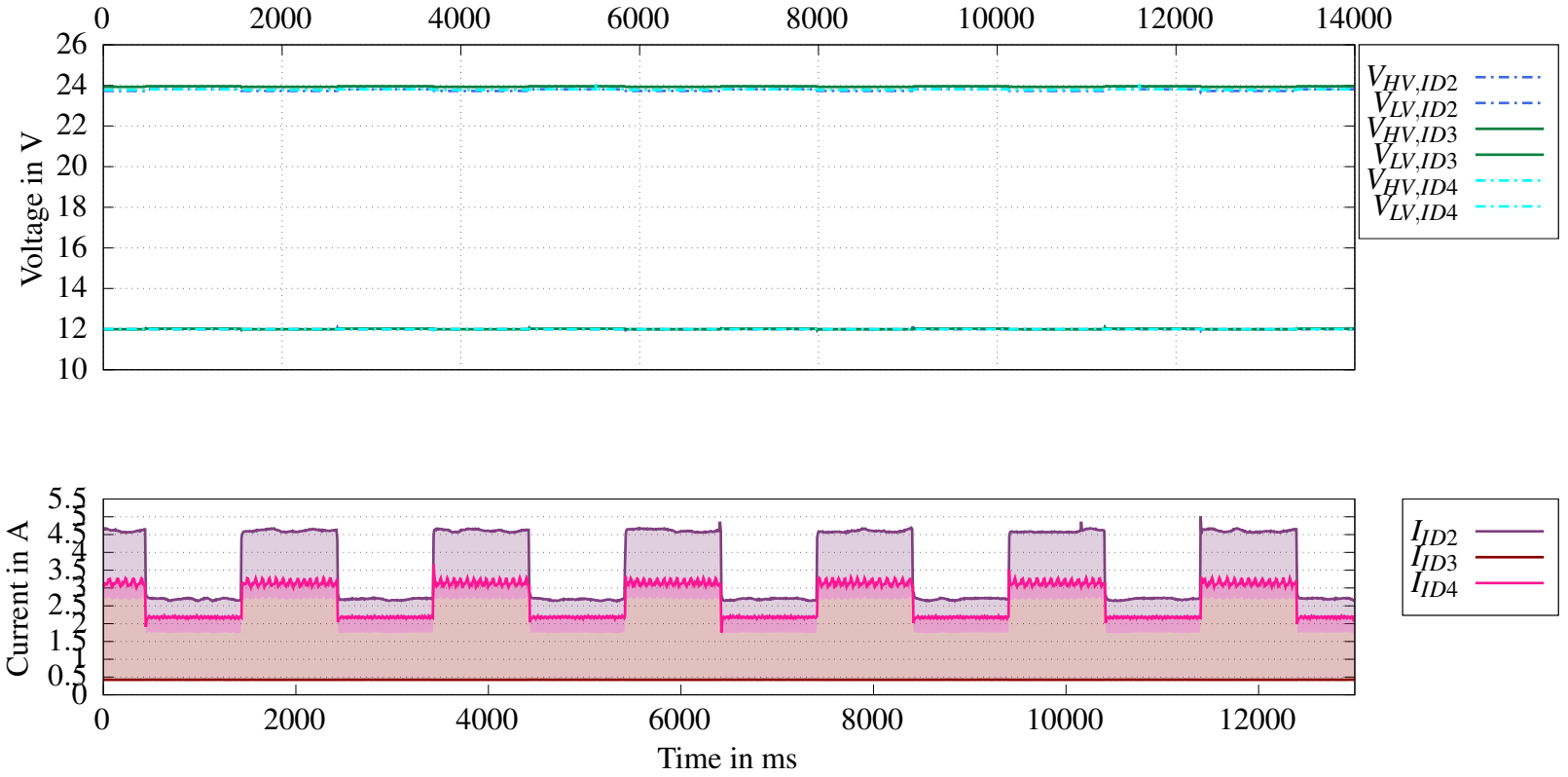


Figure 14.28: Incorrect total current: The three DC-DC converters operating in buck mode are connected in parallel and use the communication-based digital control with direct calculation by the microcontroller with an erroneous fixed value for the total current of $2A$. The division factors are identical with the value 33%. An electronic load connected at the LV-side is generating rectangular load jumps between $5A$ and $8A$. The voltage control to the set point shows no significant deviation while deviations occur in the load current distribution. This proofs that the voltage control is independent of the load current distribution control.

14.5 Summary

In this chapter experimental data for the validation of the control concepts was shown. The droop-based control was tested in both, buck and boost mode. It exhibited stable voltage control at distributed load currents, even in the case of abrupt load changes. The DC-DC converters exhibited different output characteristics, especially different internal resistances. First adjustments of the reference voltage showed that the differences of the output characteristics can be taken into account in this way. A more detailed analysis and determination of the output characteristics and the corresponding adjustment of the reference voltage is recommended for future work. Adjusting the accuracy of the load sharing is not possible in the same way with the droop based method as with the communication-based load distribution control. Rather, a gain and current limiting factor is determined via the droop resistor. As a fallback strategy, the communicationless droop-based control is nevertheless a valuable part of the DBMS and it is fully functional.
The communication-based control was also analyzed in buck and boost modes. First, measurements were made in which the control parameters were calculated directly by the microcontroller. Initially, the influence of the load distribution gain factor was analyzed: Higher gain factors lead to improved accuracy of the load current distribution and to higher control dynamics. They also resulted in overshoots at the voltage to be controlled. These voltage peaks pose the risk of triggering an overvoltage protection event, which deactivates the DC-DC converter. A gain factor was determined that can be used for a wide load range with an acceptable load distribution accuracy. Subsequently, measurements in buck and boost mode at variable load steps validated the voltage and load current distribution control. The load current distribution was performed with high accuracy, which is excellent for the application in a heterogeneous battery system.
In the following, measurements were performed in buck and boost mode using the FMAC unit of the microcontroller. Both the voltage and the load current distribution control were successfully validated, with the current control showing numerous fluctuations due to quantization errors. In future work, an improved method to reduce these quantization errors needs to be implemented.
Changes of the distribution factors showed almost instantaneous adjustment of the output currents of the DC-DC converters at stable voltage control.
The start-up of the system in droop mode with a running big leader election process and the switch to communication-based control was successfully tested.
First investigations regarding the robustness of the system have been performed. The effects of an incorrect feedback voltage measurement and the abrupt deactivation of an LCU when using the droop-based control continued to show stable voltage regulation as well as load current distribution among the DC-DC converters. The use of an incorrect total current measurement in the digital communication-based control showed no effect on the stability and accuracy of the voltage control. The load current also continued to be distributed between the DC-DC converters, although deviations occurred.

15 Conclusion and Outlook

Decentralized battery management systems are characterized by a variable number of locally operating, peer nodes. In contrast to centralized and hierarchical structures, they show a significant reduction of potential single points of failures and thus considerably improve system availability and reliability. In this thesis, a decentralized battery management system for heterogeneous battery systems was designed to realize the combination of of batteries with differences in cell chemistry, nominal capacity, safe operating area, and State of Health (SoH). The system design objectives of reliability, availability, robustness, flexibility, scalability, and reconfigurability thereby affect the software, control design, and hardware of the DBMS. The benefits of the decentralized, heterogeneous battery systems, such as support for a variety of different applications, realization of a second life applications for a variety of used batteries, and increased system reliability, are countered by challenges in the control and coordination of the system and in the hardware implementation. The focus of this work was to find solutions how to manage and control a heterogeneous battery system in a decentralized way and how to design the DBMS. The main research objective was to fully implement the DBMS in hardware with the required control methods and prove its functionality. In the following chapter, the main contributions divided into concept, architecture design, coordination and control are briefly summarized in conclusion. Furthermore, open questions and extensions for future work are described.

15.1 Conclusion

The thesis has successfully demonstrated the technical feasibility and functionality of the proposed decentralized battery management system (DBMS). The realization of the system objectives was influenced by various individual factors and required the consideration all of these in the system design.

System Control Architectures

Initially, a novel architecture was proposed after analyzing existing battery management system architectures and defining the objectives of reliability, availability,

robustness, flexibility, scalability, and reconfigurability. The proposed DBMS is characterized by functionally equal nodes that can operate autonomously and are capable of self-organization. Requirements for the communication, the control, and corresponding implementations in hardware and software were defined. This led to the main research questions: Is a stable decentralized battery system possible? And how can such a system be designed in terms of robustness and availability? To answer these questions, the system was implemented and important design decisions had to be considered in order to achieve the system objectives.

Comparative Analysis of Communication Technologies

Broadcast communication between the nodes is the basis for system-wide data consistency and for the coordination of system tasks. Communication requirements included low latency for messages consisting only of a few user data bytes, low processor workload, low power consumption, low error rate and the avoidance of RX-FIFO overloads. After a comparative analysis, the communication technology CAN FD was identified as the most suitable for the DBMS due to its one-third lower energy consumption compared to Ethernet at sufficiently high transmission rates and and adequate maximum number of user data bytes.

Leader Election for System Task Coordination

While the droop-based control is based entirely on local measurements and the nodes operate absolutely autonomously, the communication-based load distribution requires a central coordination unit. The coordination of the system tasks, the definition of the load distribution factors and the synchronization between the nodes is done by the temporary leader. One of the peer nodes is therefore elected as the temporary leader. The developed leader election algorithm uses a dynamic criterion-based election process that selects not only a leader, but also an assistant and a co-assitant to accomplish increased reliability and availability. The proposed algorithm has an approximately constant message and time complexity for the maximum number of communication participants allowed by common communication technologies by efficiently exploiting the CAN FD data format and the arbitration procedure. Furthermore, the leader election algorithm is deterministic and error handling mechanisms guarantee an abort of the election process in case of an error.

Control Strategies

Realizing the combination of different batteries in a system requires battery state-dependent load distribution and individual load current limitation. This led to the question of how heterogeneity can be managed in a decentralized system. Together with the chosen system architecture, special requirements arise regarding the DC-DC converters and their control concepts. Bidirectional DC-DC converters based on a half-bridge are used to realize the power flow in charging and discharging direction. For improved energy efficiency, a two-phase DC-DC converter was selected. Furthermore, a wide input voltage range is provided to support different batteries with varying terminal voltages, and an adjustable output voltage is given to allow diverse applications. For sufficiently high battery capacity and currents, multiple batteries together with the respective DC-DC converters are connected in parallel. A battery state dependent load distribution has been implemented. For this purpose an

evaluation value, the battery fitness, has been introduced, which takes into account the overall battery state.
The control objective is to provide a stable voltage control in the presence of variable generators and loads as well as of different, variable terminal voltages and an average current control to ensure safe battery operation.
Two control methods have been introduced: a fully decentralized droop-based control, where the nodes operate without communication using only local measurements, and a decentralized communication-based control. To reduce degradation mechanisms and ensure safe operation in a heterogeneous battery system, it is necessary to distribute the total load current among the safely usable batteries according to their actual state. In the implemented virtual droop control, the droop resistance is adjusted according to the battery state. The changes are made in software during active operation without interrupting the control or the operation. The hardware-based control is used for the implementation, which has a positive effect on the dynamics and the computational effort. This control method is characterized by robustness. Measurements using the developed hardware setup show that the droop-based control keeps the voltage setpoint stable even in the case of erroneous individual measurements or abrupt deactivation of a node. The total load current is also still divided according to the current droop resistances. Furthermore, system start-up using droop-based control has been successfully validated. Key characteristics of this control method are high dynamics due to the communicationless operation and low computational effort. The nodes do not need to know anything about the remaining system components and a measurement of the total load current is not required. A disadvantage is that droop-based control is always a trade-off between accurate voltage control or accurate load sharing. An accurate, percentage-wise load current distributions is not feasible, and the droop resistors are used instead for current limiting and gain adjustment. The use of the hardware-based controller implementation has the additional consequence that the control was designed for only one operating point. The control parameters are fixed and the total output current per LCU is limited to $13.4A$. The droop-based control was successfully validated for its intended use in the DBMS as a fallback control strategy. It is used in the event of communication failures, an erroneous or missing total current measurement, if there is no active temporary leader, and in the event of communication- or computationally-intensive operations such as softare updates.

Novel Communication-based Load Current Distribution Control

The novel communication-based control proposed in this thesis requires broadcast communication between the components, a functional temporary leader to coordinate the system tasks, and a total current measurement. It is realized as a cascaded control loop. The innermost control loop is the average current mode control which is used to control the average (dis)charging current. This one is surrounded by an outer voltage control loop to realize voltage and current control. For the load distribution, the average current mode control with external voltage control loop is overlaid by another control loop. This control method was implemented both hardware- and software-based. The hardware-based implementation is characterized by a slightly lower computational effort since it only requires the specification of a reference voltage. As described previously, the hardware-based implementation corresponds to a controller with a predefined type and fixed control parameters. In the software-based implementation, the controller is entirely implemented digitally. This offers more

flexibility and basically allows the implementation of any controller type and the realization of adaptive controllers, i.e. different controller types and parameters and the change between them. In the presented DBMS especially the change between different control parameters designed for various load ranges is especially promising. The communication-based control is characterized by an accurate load current distribution. Compared to the droop-based control, the computational complexity is higher and the dynamics is lower due to the communication in the control loop. The communication-based control has been successfully tested with both the hardware-based and software-based controller implementations. The increased requirements in terms of communication, central coordination unit (temporary leader) and total current measurement are countered by a precise load current distribution. Abrupt load changes and variations of the distribution factors were also tested and showed sufficient dynamics despite of the communication line as part of the control loop and the digital controller implementation. Communication-based digital control is the preferred control method because it provides accurate load distribution based on battery condition.
The consideration of the system objectives robustness and availability requires that the operation of the system is not endangered even if individual nodes and components such as sensors or the communication line fail. This was addressed and implemented by introducing two control schemes, the use of multiple functionally equivalent local control units (LCUs), and the redundant design of current and voltage measurements on the LCUs. These aspects reduce potential single points of failure and increase the system reliability.
The basis for the controller design was the complete mathematical modeling of the DC-DC converter in buck and boost mode, taking into account the continuous and discontinuous conduction mode respectively. The transfer functions relevant for the average current mode control with outer voltage control loop were derived generally from the electrical equivalent circuit diagrams. The pole and zero points were defined and analyzed and served as the basis for the control design. The mathematical models were successfully validated by comparison with hardware measurements. The generally derived models and transfer functions are transferable to other DC-DC converter implementations and are broadly usable.

Battery Fitness for Battery-state Evaluation in Heterogeneous Battery Systems

The load distribution between the DC-DC converters is conducted depending on the overall state of the batteries. In a heterogeneous system, this requires a system-wide unique metric to evaluate the states of different batteries. The varying safe and optimized operating areas of various batteries must be taken into account, as well as the different remaining capacities. To implement this approach, the evaluation value "battery fitness" was introduced, which evaluates the overall state of the batteries. This battery fitness value is determined individually for different operating states such as charging, discharging and storage. It takes into account parameters such as the nominal capacity, the remaining capacity, the state of charge, the temperature and the normalized capacity.

Test Framework and Simulation

For testing the DC-DC converters, a test framework was developed that considers the communication line as part of the control loop. It allows the consideration of the effect of the delays produced by the communication on the control. The test framework provides the control of electronic loads and supplies as well as the specification of set points via CAN (FD) for the DC-DC converters. It allows the testing of the DC-DC converters under consideration of the communication delay as well as the emulation of specific loads and generators.
The DC-DC converters were simulated at different abstraction levels with varying accuracy and different computational effort. On the one hand, this enabled the exact simulation of the switching processes of individual DC-DC converters and, on the other hand, it enabled system simulations with several DC-DC converters connected in parallel.
The runtime of the microcontroller software affects the control, especially the one with the digital implementation. Therefore, it was of significant importance to keep the program runtime as low as possible. This was achieved by activating different interrupts and by using the FMAC.

Key Contributions

In conclusion, the key contributions of this thesis can be summarized as follows:

- Design of a decentralized battery management system architecture for heterogeneous battery systems (HBS)
- Definition of requirements for the communication in the DBMS and selection of a suitable communication technology
- Development of a leader election algorithm for effective coordination of system tasks while reducing potential single point of failures compared to master-slave architectures
- Design of a control concept for improved reliability and robustness as well as for optimized battery operation in HBS
- Mathematical modeling of a DC-DC converter for buck and boost mode in CCM and DCM as well as derivation of the transfer functions relevant for the average current mode control with outer voltage control
- Implementation of the virtual droop control
- Design of a novel load distribution control and its hardware- and software-based implementation
- Definition of a system-wide unique metric (Battery Fitness) for the evaluation of the battery state considering the safe operating area in the operating states battery storage, charging and discharging
- Modeling of the DC-DC converter on three different abstraction levels with differences in accuracy and computational effort
- Test Framework for driving electronic loads and supplies and for testing DC-DC converters with CAN (FD) lines in the control loop
- Complete hardware test setup and experimental data for the validation of the functionality of the DBMS

15.2 Outlook

The proposed decentralized battery management system for heterogeneous battery systems and its control strategies can be further improved and investigated. Some remaining questions and promising directions for further research are summarized below.

Higher Level Energy Management Strategies

The DBMS provides the possibility to individually distribute the total load current between the DC-DC converters connected in parallel and to change the distribution factors during operation. The implementation of higher level energy management strategies offers the potential to optimize the cost, the energy efficiency, the battery lifetime and the degradation of the DC-DC converters. Efficiency improvements could be achieved, for example, by taking into account the DC-DC converter switching losses in the distribution factors and by disabling individual nodes, including the activation of deep sleep modes of the respective microcontroller used on the LCU of them. Furthermore, taking into account the electrical equivalent circuits of the batteries, in particular the internal resistances, could improve the system efficiency. In addition, the specific properties of different batteries could be taken into account to a greater extent in the optimization processes.

Consideration and Integration of Further Energy Storage Systems

So far, battery storage systems have been the main been focus for the energy storage system. In future work, an investigation could be of interest whether supercapacitors and fuel cells can be integrated into the proposed system architecture. Further investigations could examine the aging effects of the different energy storage systems and develop operating strategies for optimizations in terms of reliability of supply, energy efficiency and system lifetime.

Effect of Battery-State Dependent (Dis)Charging

While passive or active balancing strategies are used in conventional battery systems, in the DBMS the (dis)charging current is divided according to the battery state and, depending on the design of the distribution factor, recharging processes, such as those required for active balancing, can be avoided. Investigations and measurements would be interesting to determine whether the prevention of these recharging losses has an effect on the overall efficiency and whether the avoidance of recharging processes has an impact on battery degradation.

Improved Droop Control

The droop-based control still can be improved in various ways. First, the different output characteristics of the DC-DC converters have to be investigated. Here it is interesting to see whether the output characteristics remain constant over the operating time or whether they need to be adjusted at regular intervals. A detailed investigation of where these differences come from could reduce the differences in future designs. Furthermore, there are already numerous papers dealing with the improvement of the control accuracy of droop-based methods. A detailed investigation of these and a survey of their feasibility in the DBMS could also improve the load distribution

accuracy. In addition, a consideration of the line resistances is advisable for improving the load distribution accuracy.

Investigation of the Adaptive Controllers for the Software-Based Control

The software-based, digital control has so far been tested in detail with one control parameter set. Several control parameter sets have already been stored and switching between them during operation has been tested. More detailed investigations regarding the improvement of the control accuracy and dynamics compared to fixed control parameter sets have not yet been performed.

Reduction of Quantization Errors when using the FMAC

The FMAC unit was successfully implemented, but showed significant quantization errors due to the limited number display format. In future work, methods to reduce the quantization errors should be investigated and implemented.

Further Measurements

Initial measurements to validate the functionality have already been conducted. The use of higher-frequency loads is interesting for further investigations. Furthermore, the use of ohmic loads with a higher load current is recommended. Ohmic loads showed to be advantageous compared to the electronic loads as the latter ones interacted with the electronic supplies.

Long-term Tests and Investigation of Battery Degradation

Long-term measurements are required to study the effect of the battery state-dependent load distribution on the battery degradation. Data collected via the CAN FD logger will provide the usage history. Initial and later electrochemical imepdance spectroscopy measurements of the batteries together with the usage history could give first indications whether the chosen distribution factors help reducing the battery degradation.

Determination of the Limits for the Battery Fitness Value on the Basis of Experimental Data

In this thesis, the evaluation metric battery fitness was introduced for a battery state dependent load current distribution in a heterogeneous battery system. The limits for defining the safe operating area were obtained from data sheets and the operating area for the optimized operating area was defined by further reducing the SOA. It would be interesting, albeit complex, to define the boundaries of the SOA and OOA using experimental data. The challenge is that even small changes in the shape of the battery cells affect the limits. Furthermore, knowledge of the OOA requires time-consuming cycling of the batteries and complex electrochemical internal resistance measurements. However, since improved knowledge of this could potentially keep the internal resistance of the batteries at a lower value over a longer period of operation, which in turn affects the efficiency, lifetime, cost, and sustainability of the overall system, the investigations are recommended.

Overall System Simulation for the Proof of Scalability

The functionality of the system has so far been tested using a hardware test setup consisting of four battery nodes and a load. To validate the scalability of the system, measurements with more participating nodes are required. This can be done most efficiently by simulation. While individual components for the overall simulation of the system have already been implemented in Modelica, a composition of the subcomponents has not yet been completed. The overall simulation of the system in Modelica is part of future work. It enables the investigation of the scalability of the system and allows the efficient testing of various loads and consumers.

Integration of Electrochemical Battery Models

The battery simulation package PyBaMM is a promising way to integrate battery aging into further investigations. The PyBaMM models take into account electrochemical aspects in addition to the usual electrical aspects. First attempts to integrate the models into the Modelica simulation have already been conducted. It turned out that the most effective variant is to use a co-simulation with TCP/IP connection between the PyBaMM and Modelica simulations. Completion of the co-simulation environment and intensive testing are recommended for further work, as they can also provide a significant contribution to the study of the effect of load distribution control on battery degradation.
Furthermore, porting the PyBaMM models to microcontrollers for improved state of health determination is an interesting extension of the DBMS.

Improvement of the DC-DC Converter Hardware and EMC Investigations

This work focused on proving the functionality of the DBMS rather than optimally designing the DC-DC converters. More detailed loss considerations of the DC-DC converters and their components, improved selection of electronic components considering system efficiency and lifetime and intensive EMC tests are part of future work.
The proposed decentralized battery management system offers the possibility to combine various batteries including new and second life ones in a system, taking into account reliability and optimized battery operation. Batteries are increasingly used as energy storage devices for a variety of different applications, leading to an growth in the number of second life batteries. From an economical and sustainable point of view, the consideration and integration of second life batteries is necessary to reduce the negative financial and ecological impact of prematurely disposed batteries. The introduction of the EU battery passport [545] is very promising especially for the use of used batteries and also offers valuable opportunities for the proposed DBMS.

List of Figures

1.1 Global average land-sea temperature anomaly 1
1.2 Annual CO_2 emissions 2
1.3 World population 2
1.4 Block diagram of a battery management system. 3
1.5 Forecast of global new lithium-ion capacity and the available second-life battery capacity 4
1.6 Exemplary representation of circulating currents 5
1.7 Methodology: Applied Research Design 6
1.8 Assignment of the individual chapters to the research questions . . . 9

2.1 Basic structure of a battery cell [34]. 11
2.2 Basic Cell Chemistry of Lithium-based cells 15
2.3 Positive electrode materials of lithium-based cells 16
2.4 Negative electrode materials of lithium-based cells 17
2.5 Electrolytes for lithium-based cells 17
2.6 Overview of battery safety hazard categories. 21
2.7 Subdivision of the operating areas into optimized operating area (OOA), safe operating area (SOA) and hazardous area 22
2.8 Thévenin equivalent circuit model of a battery [192, 193] 24
2.9 Capacity fade over the lifetime of a battery. 29
2.10 Shifting the knee point 29
2.11 Interdependencies and interaction of lithium-ion battery cell degradation mechanisms including their causes and effects. [190]. 31

3.1 Principle architecture of a battery management system indicating participants, communication and power flow. The participants consist of a variable number of heterogeneous batteries, variable loads and renewable energy generators. 34
3.2 Simplified block diagram of a battery management system based on centralized topology, which records the operating data of the individual cells, monitors them and coordinates the system control. 35
3.3 Block diagram of a battery management system based on a modular topology. 36
3.4 Block diagram of a battery management system based on a distributed topology 37
3.5 Block diagram of a decentralized battery management system 38
3.6 Overview of the decentralized battery management system with battery state-aware load distribution: The local control units are the basis for distributed control and battery state-dependent load sharing. 39

3.7 The Local Control Units (LCUs) consist of microcontrollers, current, voltage and temperature sensors and relays. The operating parameters are recorded and managed by the LCUs. This allows to apply predictive energy management strategies and helps to estimate the residual value of the batteries. 40

4.1 Test setup for the comparative analysis of CAN, CAN FD and Ethernet 46
4.2 Structure and size of the User Datagram Protocol (UDP), CAN FD and CAN frame 46
4.3 Layer of the Osi model covered by CAN (FD) and Ethernet 47
4.4 Overview of the software components and the interfaces between them required for the comparative analysis between CAN, CAN FD and Ethernet. 49
4.5 Block diagram of the hardware components for CAN, CAN FD and Ethernet communication 50
4.6 Measurement of message processing time 51
4.7 Init and message processing time for varying user data byte 54
4.8 Processor Times for a periodic send interval of 10 ms 55
4.9 Processor times for a periodic send interval of 0.02 ms 56
4.10 Power consumption of the CAN (FD) and Ethernet 57
4.11 Comparison of the power consumption of the CAN (FD) and Ethernet divided into run, idle and sleep mode 58
4.12 Test-setup 59
4.13 Analysis of the utilization of the RX-FIFO 60
4.14 Decision matrix for the selection of the communication technology . 64

5.1 Existing leader election algorithms can be divided into static and dynamic ones based on the repetition frequency. They can further be classified into criterion-based and random. 69
5.2 System overview and properties of the election participants 70
5.3 Election messages based on the CAN (FD) format 70
5.4 System states of the leader election 73
5.5 State diagram Big LEA-CAN 74
5.6 Activity Diagram Big LEA-CAN 75
5.7 Activity diagram CAN handler Big LEA-CAN 76
5.8 Position change management level 78
5.9 State diagram Small LEA-CAN 79
5.10 Activity diagram small LEA-CAN 79
5.11 Activity diagamm CAN handler Small LEA-CAN 80
5.12 Structure of election messages 81
5.13 Message and time complexity of Big LEA-CAN 82
5.14 Sequence diagram of the Big LEA-CAN 85
5.15 Message and time complexity of Small LEA-CAN 86
5.16 Block diagram of the hardware test setup to verify LEA 86
5.17 Hardware test setup to verify LEA 88

6.1 Decentralized Battery Management (DBMS) system architecture consisting of battery, generator and load nodes. The control is distributed in a local and global level. 90

6.2 Centralized, distributed, and hierarchical control strategies require global communication between nodes, while decentralized control operates communication-less. 91
6.3 Existing control strategies can be categorized in centralized, decentralized, distributed and hierarchical ones. Common strategies mainly consider battery nodes in the control, while it is also possible to consider load and generation nodes. 92
6.4 Simplified representation of the main control objective. The main control objective is to maintain the DC power line voltage at a certain predefined setpoint for a given load and generation by controlling the battery currents. Batteries can supply missing energy (discharging, positive currents) or absorb excessive one (charging, negative currents). 94
6.5 The system objectives, the control objective, and the constraints mandatorily affect each control strategy, while the optimizations are optionally considered. 95
6.6 The slope of the droop curves of the local droop based controllers for the battery nodes and thus the value of the virtual internal resistances determine the discharge current and are adjusted according to the battery state. In local measurements, the actual DC power line voltage is acquired and compared with the stored droop characteristic to specify the output current. In this scenario, Battery 1 supplies the majority of the required power. 96
6.7 The cascaded control of the DBMS consists of an outer, global control loop and several inner, local control loops (Fig. 6.1). The microcontroller of the temporary leader is the global controller and it takes into account the battery states, the measured generation and power consumption as measured disturbances (feedforward control) and the measured actual values (feedback control) for the specification of the actuating variables. Furthermore the temporary leader steers its own DC-DC converter to adjust the remaining control deviation. 97
6.8 State diagram of the global control level with state transitions T_1 and T_2 (Equations 6.1, 6.2.) 100
6.9 Estimation of the characteristics of the control strategies at the global control level: The droop-based control is characterized mainly by robustness and lower system requirements, while the communication-based control strategy provides more precise setpoint specifications and takes battery conditions into account more effectively. 100
6.10 The task of the local control loop is to control to the setpoint w specified by the global control level (Fig. 6.7). The actuator is the DC-DC converter whose control variable y is specified using either a digital or analog controller. 101
6.11 The bidirectional DC-DC converter used in the DBMS consists of two phase-shifted channels which in turn are based on half bridges. [336]. 101

6.12 In the analog, hardware-based control, a voltage reference V_{ISETA} is specified for the subsequent current controller. Input signals are once the feedback output voltage, downscaled via a voltage divider, and a reference voltage specified via the DAC of the microcontroller. Both droop- and communication-based control can be implemented in analog mode. 102
6.13 The digital adaptive controller offers increased flexibility. Depending on the type of control disturbances, the controller parameters and types can be changed during active operation. Several controller implementations can be realized by software. The microcontroller directly generates a PWM signal for the subsequent current controller. 103
6.14 Operating states of the DBMS and the respective transfer conditions, which are defined in Tab. 5.1. *Transfer to the state error operation is possible from all operating states. 104
6.15 Overview of the entire controller design process and assignment of the individual chapters. 105

7.1 In the decentralized battery management system, bidirectional DC-DC converters with wide input voltage ranges and adjustable current limits ($|I_{\mathrm{Safe}}|$) realize the power flow between different batteries with varying safe operating areas (SOA) and SoC dependent output voltages. Appropriate controllers are mandatory for precise current sharing between the parallel connected converters. 108
7.2 Circuit of one of the two half bridges of the bidirectional DC-DC converter together with the current controller LM5170. 111
7.3 Waveforms of the inductor currents in continuous conduction mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM), where d_{CCM} and dDCM are the duty cycles which determine the on-times of the switches. 112
7.4 Selection of the basic transfer functions of a DC-DC converter for voltage and average current mode control, where ∂V is the output voltage, ∂I is the output current, ∂d is the duty cycle and $\partial V_{\mathrm{g}}(t)$ is the small-signal disturbance input. [356] 113
7.5 Equivalent circuit diagram of an ideal buck converter. The input capacitor is assumed to be free of losses and is replaced by an ideal voltage source. [356] 114
7.6 Equivalent circuit diagram of the output low-pass of the DC-DC converter in buck mode and in CCM. [356] 114
7.7 Bode plots of the derived, calculated transfer function $G_{\mathrm{id}}(s)$ (exact Equ. (7.8) and approximated Equ. (7.15)), whereby the resonant behavior is neglected in the approximation. The straight lines are approximations. The largest part of a phase shift caused by a complex pole is limited to a frequency range whose width depends on the pole damping [382]. Here, the pole damping is 0.16. Equation (7.11) defines the pole positions. 117
7.8 Equivalent circuit diagram of the output low-pass filter forming the basis for deriving the voltage transfer function. [356] 118
7.9 Bode plots of the calculated transfer function of the output current to the output voltage $G_{\mathrm{vi}}(s)$ (Equ. (7.16)). 119

7.10 Equivalent circuit diagram of the DC-DC converter in buck mode and in DCM. The values of the equivalent circuit elements are defined in Table 7.1. [356] 120
7.11 Simplified small-signal equivalent circuit in buck mode and in DCM neglecting the influence of the input voltage change $\partial V_{\mathrm{HV}} = 0$. [356] 120
7.12 Bode plots of the derived, calculated duty cycle to current transfer function $G_{\mathrm{id}}(s)$ (Equ. (7.22)) in DCM. Equation (7.25) gives the definition of the poles. 121
7.13 Ideal boost converter, where the input capacitor is assumed to be lossfree and is replaced by an ideal voltage source. [356] 123
7.14 Waveforms of the inductor currents in continuous conduction mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM), where d_{CCM} and d_{DCM} are the duty cycles which determine the on-times of the switches. 123
7.15 Small-signal equivalent circuit of the DC-DC converter in boost mode and in CCM, whereby $D' = (1-d)$. [356] 124
7.16 Bode plots of the exact (Equ. 7.32) and approximated (Equ. 7.37) calculated current transfer functions $G_{\mathrm{id}}(s)$. The exact one considers high frequency behavior. The straight lines are approximations. . . 126
7.17 Bode plots of the current to voltage transfer function $G_{\mathrm{vi}}(s)$ (Equ. (7.40)). The straight lines are approximations. 128
7.18 Small-signal equivalent circuit of the bidirectional DC-DC converter in boost mode and DCM. The values of the equivalent circuit elements are defined in Table 7.2. [356] 129
7.19 Simplified small-signal equivalent circuit for the analysis of the current to output behavior in boost mode and DCM. [356] 129
7.20 Bode plots of the duty cycle to current transfer function $G_{\mathrm{id}}(s)$ (Equ. (7.41)) in DCM. The straight lines are approximations. 130
7.21 Calculated poles of the duty cycle to transfer functions in DCM (marked blue) and CCM (marked black). 132

8.1 Overview of the operating modes of the bidirectional DC-DC converter. 136
8.2 Principle of the voltage control approaches direct duty cycle control (DDCC) and voltage feedforward control (VFC). The difference between the setpoint voltage V_{set} and the output voltage v_{out} and the sawtooth voltage v_{st} are the input signals of the comparator, that generates the PWM signal to control the transistor. [385] 139
8.3 Principle of the Peak Current Mode Control (PCMC): The voltage controller output v_{c} corresponds to the difference between the actual voltage and the setpoint value and is the input signal of the comparator. To account for the current control, the voltage v_{Shunt} is also applied to the input of the comparator. Slope compensation is used to stabilize the current control in case of duty cycles greater than 0.5 for continuous conduction mode. This prevents subharmonic oscillations and consequently spikes in the measured current. [385] 140

8.4 Principle of the Average Current Mode Control (ACMC): The voltage controller compares the actual voltage value v_{out} with the setpoint V_{set}. The additional current controller subsequently compares the current-proportional setpoint $v_{i,set}$ with the current voltage across the shunt resistor v_{Shunt} and generates the controller output v_c. The following comparator generates corresponding switching pulses to control the power transistor until v_{Shunt} corresponds to the value $v_{i,set}$ and the required average current value is reached. [385] 141
8.5 Control loop of the Direct Duty Cycle Control (DDCC) for voltage control of the bidirectional DC-DC converter. 142
8.6 Cascaded control loop: For voltage and current control, an outer voltage control loop is placed around the inner current control loop (ACMC). The measured output voltage v_{out} is compared with the setpoint voltage V_{set}. The voltage controller $G_V(s)$ processes the error signal and produces the reference signal $v_{i,set}$ for the current control loop. The reference signal is compared with the voltage across the shunt resistor v_{Shunt}. The current controller processes the error signal and produces the controller output signal v_c, which in turn is used for generating the switching signal. 143
8.7 Principle circuit diagram of the Average Current Mode Control using hardware based current and voltage controllers. [385] 143
8.8 Block diagramm of the inner average current mode control and the outer voltage control loop with the small-signal model of the DC-DC converter and the relevant transfer functions, which are described in Chapter 7. [387] 148
8.9 Block diagram of the voltage control loop with the closed inner current control. [387] 149
8.10 Functional diagram of the common control block of the ACMC integrated circuit (IC) LM5170 [388]. The main functions include fault detection, overvoltage protection, buck or boost selection, and analog or digital control option. (Picture slightly adapted from [388]) 151
8.11 Functional diagram of one of the two channel average current mode control units of the LM5170 [388]. Main functions are the control of the two MOSFETs, the generation of the ramp signal and the measurement of the controller output. (Picture slightly adapted from [388]) 152
8.12 To generate the switching edges $v_G(t)$, the controller output is connected to the non-inverting input of an operational amplifier. The voltage of the sawtooth generator is applied to the inverting input. . 153
8.13 Calculated Bode diagram of the closed current control loop of the buck converter in the CCM. The closed current control loop with the approximated $G_{id,A}(s)$ (Equ. (7.9) on p. 7.9)) and the exact $G_{id}(s)$ (Equ. (7.8) on p. 7.8)) current to duty cycle transfer function is shown. 155
8.14 Bode diagram of the controlled open loop at a crossover frequency of $f_c = 1\,kHz$ and an approximation with $\frac{2\pi f_c}{s}$ 157
8.15 General structure of an analog controller 158

8.16 Magnitude and phase response of the closed-loop current control loop in buck mode and CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equations (7.19), (8.35), (8.39), and (8.37) were used. 165
8.17 Magnitude and phase response of the current to voltage transfer function G_vi in buck mode and in CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The analog controller was used during the measurements. The equation (7.27) is the basis for the calculated results. 165
8.18 Magnitude and phase response of the open loop of the voltage control in buck mode and CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used. 165
8.19 Magnitude and phase response of the open loop of the voltage control in buck mode and CCM at a load resistance of $R_\mathrm{l} = 2\,\Omega$. The hardware measurements were acquired using the digital controller. For the calculation the equation (8.51) was used. 166
8.20 Measured and calculated magnitude and phase response of the closed current loop of the buck converter in DCM mode at a load resistance of $R_\mathrm{l} = 24\,\Omega$. The equations (7.22), (8.35), (8.39), and (8.37) were used for the calculation. Hardware measurements were acquired using the analog controller. 166
8.21 Measured and calculated magnitude and phase response of the current to voltage transfer function G_vi of the buck converter in DCM at a load resistance of $R_\mathrm{l} = 24\,\Omega$. The analog controller was used for the hardware measurements and the calculation is based on the equation (7.27). 166
8.22 Magnitude and phase response of the open loop of the voltage control in buck mode and DCM at a load resistance of $R_\mathrm{l} = 24\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used. 167
8.23 Measured and calculated magnitude and phase response of the closed-loop current control circuit of the boost converter in CCM mode at a load resistance of $R_\mathrm{l} = 6\,\Omega$. The calculations were conducted using the equations (7.32), (8.35) and (8.39) and (8.37). 167
8.24 Measured and calculated magnitude and phase response of the current to voltage transfer function G_vi of the boost converter in CCM mode at a load resistance of $R_\mathrm{l} = 6\,\Omega$. For the calculation equation (7.40) was used. 167
8.25 Magnitude and phase response of the open loop of the voltage control in boost mode and CCM at a load resistance of $R_\mathrm{l} = 6\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used. 168
8.26 Magnitude and phase response of the open loop of the voltage control in boost mode and CCM at a load resistance of $R_\mathrm{l} = 6\,\Omega$. The hardware measurements were acquired using the digital controller. For the calculation the equation (8.51) was used. 168

8.27 Measured and calculated magnitude and phase response of the closed loop current control circuit of the boost converter in DCM mode at a load resistance of $R_l = 24\,\Omega$. Equations (7.41), (8.35), (8.39), and (8.37) served for the calculation. 168
8.28 Measured and calculated (Equation (7.54)) magnitude and phase response of the current to voltage transfer function G_{vi} of the boost converter in DCM mode at a load resistance of $R_l = 24\,\Omega$. 169
8.29 Magnitude and phase response of the open loop of the voltage control in boost mode and DCM at a load resistance of $R_l = 24\,\Omega$. The hardware measurements were acquired using the analog controller. For the calculation the equation (8.51) was used. 169

9.1 Block diagram of the central control limit with individual voltage feedback path and dynamic voltage reference for two DC-DC converters connected in parallel. [427–430] 175
9.2 Overview of load distribution control strategies. 176
9.3 Overview and categorization of common strategies to manage heterogeneity in battery systems. 178
9.4 Equivalent circuit diagram of the droop control where the load sharing between the DC-DC converters, in this case two, is set via the droop resistances r_{d1}, r_{d2}. 180
9.5 For higher output powers, the droop resistor is implemented virtually in order to reduce the power dissipation. The reference voltage is adjusted using the virtual resistance according to Equation (9.3). . . 181
9.6 Course of the current distribution error over the droop resistor [471] 182
9.7 Droop control methods to reduce the error [471], black curve based on Equation (9.4), red and blue curve based on Equation (9.3). . . . 182
9.8 Example of the implementation of the droop-based control at local level. Two software variables v_{ref} and r_d are used to set the level of the voltage to be controlled and the slope of the droop characteristic. 183
9.9 General control loop of the parallel connection of structurally identical DC-DC converters with current control and a droop based control for voltage control and current distribution. In this case a parallel connection of two DC-DC converters is considered. 183
9.10 Circuit for the implementation of analog control. Since the control paths for buck and boost mode are different, two separate controllers are required, which differ in the dimensioning of the electrical components. The droop control is realized by a virtual impedance. A reference voltage determined according to Equation (9.4) is specified via the digital to analog converter of the microcontroller. 184
9.11 Merging the controls for buck and boost mode. The resulting voltage divider is referred to as G_{Merge} hereafter. 184
9.12 First hardware implementation of the controller shutdown circuit causing offset voltages. 185
9.13 In subsequent hardware implementations, an analog switch is used to change between the controllers according to buck and boost mode. 186
9.14 Circuit to limit the output signal. 186

9.15 Structure of the load distribution control and average current mode control with outer voltage control: An additional superimposed control loop has been introduced for load distribution according to the distribution factor α_i. 187
9.16 Complete control loop of the load distribution control with summarized, closed inner current control loop H_s. 188
9.17 Parallel connection of two converters with identical output capacitance C 190
9.18 Control loop of the Direct Duty Cycle Control (DDCC) for voltage control of the bidirectional DC-DC converter. 193

10.1 For the safe operation of heterogeneous battery systems, it is necessary to limit the battery currents ($I_{i,\max}$) according to the deviating Safe Operating Areas (SOAs). The total current is divided among the batteries connected in parallel according to the distribution factors (α_i). The distribution factors can take into account additional system aspects such as low power dissipation by considering the switching losses of the DC-DC converters. 196
10.2 The three different batteries all exhibit a SoC of 50 percent. Different nominal (C_N) and actual capacities (C_{act}) show that distribution factors based simply on the SoC are not sufficient. The SoC itself is not indicative of the remaining discharge (C_{rem}) or charge capacity ($C_{act} - C_{rem}$). 197
10.3 Considering additionally the battery cell dependent safe operating areas, in this example the safe SoC ranges, shows that a more sophisticated load distribution factor taking into account several battery characteristics is required. 198
10.4 For optimized battery operation in terms of degradation reduction, the safe operating area is further restricted to the optimized operating area. The further limitation of the SoC is shown. The optimized operating areas differ depending on the battery chemistry and design. 198
10.5 Negative electrode materials of lithium-based cells 201
10.6 The safe operating area of the batteries must be maintained at all times for reliable operation and high system availability. If more battery charging or discharging energy is available than required, the operating area of the batteries can be further restricted (OOA) and the degradation due to the operation can be taken into account. . . . 203
10.7 State diagramm of the battery operation 204
10.8 The derating factors are determined based on look up tables (LUTs) on the micrcontollers of the LCUs. For a first implementation, temperature, SoC, SoH and the current capacity are used as inputs. Derating factors are defined for charging δ_c and discharging δ_d and for safe and optimized operation. 204
10.9 Activity diagram for determining the derating factor. 206
10.10 For all battery parameters, the current value (in this case the measured temperature) is compared with the look up table (LUT) of the current operating state and the individual derating factor (δ_T) is determined. 206
10.11 Safe operating area of the temperature for the operating state charging for a lithium-ion battery [487]. 207

10.12 Safe operating area of the temperature for the operating state discharging for a lithium-ion battery [487]. 207
10.13 Safe operating area of the temperature for the operating state short term storage for a lithium-ion battery [487]. 207
10.14 Safe operating area of the temperature for the operating state long term storage for a lithium-ion battery [487]. 207
10.15 Safe operating area of the SoC for the operating state charging for a lithium-ion battery [487]. 207
10.16 Safe operating area of the SoC for the various operating state discharging for a lithium-ion battery [487]. 207
10.17 Safe operating area of the SoC for the various operating state storage for a lithium-ion battery [487]. 208
10.18 For battery state aware current derating in a battery system with new and second life batteries, consideration of the SoH is required. . . . 208
10.19 In order to take into account the different capacities of the batteries, the normalized capacity in percent is introduced. 208
10.20 The CAN message contains the current derating factors for safe and optimized operation for the operating states charging and discharging. 208
10.21 The efficiency of the DC-DC converter operating in boost mode with the higher $V_{\text{out}} = 50.5\,V$ at the high voltage side [388]. 209
10.22 The efficiency of the DC-DC converter operating in buck mode with the lower $V_{\text{out}} = 14.5\,V$ at the low voltage side [388]. 209

11.1 The bidirectional, half-bridge-based DC-DC converter is emulated by three different models of varying accuracy. 212
11.2 One of the two half-bridges of the multiphase DC-DC converter under investigation. Table 11.1 lists the properties of the components. 214
11.3 Switching signals of the MOSFET in diode emulation mode: If the current through the inductor reaches the value zero, the sync MOSFET is switched off and negative currents are avoided. [499] 215
11.4 UML class diagram and overview of the composition of the various subclasses of the strictly complementary switching model `ControlledBuckBoost`. 216
11.5 The `ChopperBuckBoost` model forms the switching level of the physical model and represents one of the two half-bridges. 216
11.6 Overview of the model for the bidirectional DC-DC converter together with the interfaces. 218
11.7 Overview of the model `TwoCHController` for modeling the entire control of the DC-DC converter. 219
11.8 The model `controllerAlgorithm` simulates the PID-controller. . . 220
11.9 The model `ControlledBuckBoost` simulates the current controlled DC-DC converter with strictly complementary switching behavior. 220
11.10 To verify the model, in this case `ControlledBuckBoost`, the step response is simulated and compared with the theoretical transfer function. 221
11.11 Comparison of the inductor current over time of the strictly complementary switching model and the theoretical transfer function. . . . 221
11.12 Step reponse of the strictly complementary switching model and the theoretical transfer function, ... 222

11.13 UML class diagram and overview of the composition of the various subclasses of the switching model with diode emulated mode `ControlledBuckBoost`. 223
11.14 Overview of the model `CurrentDirectionCorrection` for the diode emulated mode. In this case, the switching threshold for diode emulation is 0.4 A instead of 0 A in order to reduce the deviation. . 223
11.15 The model `DiodeModeGen` generates the switching signals for the MOSFETs according to the diode emulated mode (Fig. 11.3). 224
11.16 Comparison of the inductor current over time of the switching model with diode emulated mode and the theoretical transfer function. . . . 224
11.17 Step response of the switching model with diode emulated mode and the theoretical transfer function. 225
11.18 Detailed analysis of the step response showing significant deviation of the model using diode emulated mode. There is a deviation of approximately 0.4 V with the sign depending on the PWM phase. . . 225
11.19 Reduction of the deviation by adjusting the current thresholds. . . . 226
11.20 Hierarchical overview of the classes of the averaging model. 227
11.21 The model `DutyCycleWithLosses` determines the averaged output current and voltage according to the equations (11.3) and (11.4). `DutyVoltage` corresponds to $V_{\text{av,real}}$ and `DutyCurrent` to $I_{\text{av,ideal}}$ . . 227
11.22 The model `CHBuckBoostAveraged` is the averaging model of one of the two half bridges. The MOSFETs are replaced by current and voltage sources which provide the average values. 228
11.23 Comparison of the inductor current over time of the averaging model and the theoretical transfer function. 229
11.24 Step response of the averaging model and the theoretical transfer function. 229
11.25 Comparison of the required computation time in relation to the simulation progress of the three proposed models. 230
11.26 Possible use case of the averaging model: simulation of load sharing between two DC-DC converters connected in parallel, where one (`controlledBiChopper1`) consumes 30 percent of the charging current and the other one (`controlledBiChopper`) 70 percent. . . . 231
11.27 Step response of the parallel connection of two DC-DC converters with load current sharing using the averaging models. 232

12.1 Overview of the decentralized battery management system (top) and detailed presentation of a component with a local control unit (LCU) (bottom). . . 234
12.2 Functional description and correlation of the simulation [237], the test framework and the hardware. 235
12.3 Test architecture for several DUTs, possibly of mixed types. 236
12.4 Connection of a hardware DUT_i to the software simulation. 237
12.5 Software design of the test framework. 238
12.6 Extract and syntax example of the SCPI to configure the electronic load . . 239
12.7 Overview of the software and hardware components of the test framework 240
12.8 Load test with continuous load change 241
12.9 Efficiency of the DC-DC converter [520] 241
12.10 Voltage at the input of the DUT [520] 241
12.11 Current at the input of the DUT [520] 241
12.12 Voltage at the output of the DUT [520] 241

12.13 Current at the output of the DUT [520] . . . 241
12.14 Measurement of the response time considering the networked control of the DC-DC converter[520] . . . 242
12.15 The test setup consists of the LCU using a Cortex-M4 microcontroller ①, the DC-DC converter to be tested [520] ②, which is connected to the electronic load [521] ④ via power lines ③. A CAN-to-USB interface ⑤ and a CAN line ⑥ are used for data transfer between the PC ⑦ and the DUT ①–④. . . . 242
12.16 Load test with abrupt load jump . . . 244
12.17 Voltage at the output of the DUT [522] . . . 244
12.18 The Cortex-M7 based LCU ① is attached to the DC-DC converter [522] under test ②. . . . 245

13.1 Overview of all hardware components of the decentralized battery management system. . . . 249
13.2 Development over time and overview of the different DC-DC converter types which can be used in the DBMS . . . 251
13.3 The voltage and current values are specified via PWM signals. The voltage control is two-stage while the current limitation is part of the feedback line of the buck converter. . . . 252
13.4 Structure of the Modbus RTU protocol for controlling the DC-DC converter DPS5015 [525]. . . . 253
13.5 Customized feedback loop for adjustable output voltages. . . . 254
13.6 The final version of the local control unit is realized as a single PCB combining the power and control circuits. It includes a multiphase, bidirectional DC-DC converter with controller and corresponding sensor modules. Furthermore, a microcontroller with corresponding communication interfaces and an external ADC are integrated on the board. . . . 256
13.7 The power circuit of the bidirectional DC-DC converter consists of two parallel connected channels with measuring units on the low and high voltage side. . . . 256
13.8 Each channel of the power circuit corresponds to a half bridge. The MOSFETs are controlled by the DC-DC converter controller (Fig. 13.10). For the feedback control the instantaneous value of the current is given by a shunt based measurement. . . . 256
13.9 Two analog switches are used for switching between analog and digital control. According to the specification of the microcontroller, the ISETA for the analog control or the ISETD for the digital control is passed through to the controller. [526] . . . 257
13.10 DC-DC Control with LM5170 . . . 258
13.11 Additional sensing modules based on the IC INA228 [527] are inserted at the HV and LV side. In addition to current, voltage and power, energy, charge and temperature are also recorded. The analog values are converted with a 20 bit delta sigma ADC. Furthermore, the sensing module has an I^2C interface which is connected to the microcontroller. . . . 260
13.12 The voltages on the HV and LV side are adjusted via appropriate voltage dividers and connected to the analog inputs of the microcontroller. They are necessary for the digital control. . . . 260

13.13 The external ADC120 is mainly used for improved resolution of the current measurement values. Internally, the conversion method sukszessive approximation is used. Via an SPI interface, conversions are triggered and digital values are sent to the microcontroller [529]. 261
13.14 Overview of the timers relevant for the control and their frequency. Timers A and B are high resolution timers. 262
13.15 Overview of the main input and output signals of the microcontroller and part of the peripheral units used. [530] 263
13.16 Local and global communication interfaces. 263
13.17 Unassembled PCB (20 cm x 15 cm) of the LCU. Figure 13.6 shows an abstracted overview of the LCU. 264
13.18 Block diagram of the load box CAN FD: The load box consists of a microcontroller [530], four sensing modules based on the IC INA 226 [532] together with a shunt resistor, four relays [533] connected to the GPIO pins of the microcontroller via darlington transistors [534], a real time clock [535], a CAN FD Interface [536], a power supply for the microcontroller [537] and connectors [538]. 265
13.19 Abstracted overview of the software running on the microcontroller of the load box. 266
13.20 Block diagram of the display unit: The microcontroller controls the LEDs and the LC-display via an SPI interface. It receives the data via the UART interface from the microcontroller of the LCU. [539–544] 266
13.21 Block diagram of the CAN (FD) data logger. All the messages are logged and stored sorted by their user ID in a database. Additionally the actual state of the batteries can be monitored vie the web interface. 267
13.22 Hardware implementation (20 cm x 15 cm) of the local control unit 268
13.23 Hardware test setup 269

14.1 Test setup to validate the functionality and the control in buck mode 272
14.2 Test setup to validate the functionality and the control in boost mode 273
14.3 Four DC-DC converters connected in parallel operate in boost mode using droop-based control. All DC-DC converters have identical droop resistance ($R_{\mathrm{d}} = 0.1\,\Omega$) and individual output characteristics are not considered ($V_{\mathrm{ref}} = 2.05\,V$). The DC-DC converter ID1 has an incorrect LV measurement. The DC-DC converter ID4 has a lower internal resistance compared to the remaining ones, which leads to an increased total gain resulting in high output currents and fluctuations at the high voltage. 276
14.4 Four DC-DC converters are connected in parallel and operate in boost mode. For load distribution, the droop-based analog control is used with equal droop resistors with considering individual output characteristics ($R_{\mathrm{d,ID1-4}} = 0.1\,\Omega$, $V_{\mathrm{ref,ID1}} = 2\,V$, $V_{\mathrm{ref,ID2}} = 1.87\,V$, $V_{\mathrm{ref,ID3}} = 2.02\,V$, $V_{\mathrm{ref,ID4}} = 2\,V$). The LV measurement of the DC-DC converter with the ID1 is incorrect. The DC-DC converters do not exhibit equal output currents due to varying output characteristics and measurement tolerances. 277

14.5 Four parallel connected DC-DC converters, which operate with analog, droop-based control in boost mode, are connected at the HV-side to an ohmic load and at the LV-side to an electronic supply. The reference voltages are adjusted in order to change the output behavior of the DC-DC converters and the droop resistors are different ($R_{\mathrm{d,ID1}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID1}} = 2V$, $R_{\mathrm{d,ID2}} = 0.3\,\Omega$, $V_{\mathrm{ref,ID2}} = 1.87V$, $R_{\mathrm{d,ID3}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID3}} = 2.02V$, $R_{\mathrm{d,ID4}} = 1.2\,\Omega$, $V_{\mathrm{ref,ID4}} = 2V$). . . 278
14.6 Four DC-DC converters connected in parallel operate in boost mode using the droop based control. An ohmic load is connected at the HV-side. Both the droop resistors and the reference voltages are individual adapted ($R_{\mathrm{d,ID1}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID1}} = 2V$, $R_{\mathrm{d,ID2}} = 0.3\,\Omega$, $V_{\mathrm{ref,ID2}} = 1.87V$, $R_{\mathrm{d,ID3}} = 0.7\,\Omega$, $V_{\mathrm{ref,ID3}} = 2.02V$, $R_{\mathrm{d,ID4}} = 1.2\,\Omega$, $V_{\mathrm{ref,ID4}} = 2V$). 279
14.7 Measurement over a duration of $200\,s$: Four parallel connected DC-DC converters, which operate with analog, droop-based control in buck mode, are connected at the HV-side to an electronic supply and at the LV-side to an electronic load which generates rectangular load jumps between $6A$ and $10A$. The reference voltages and the droop resistors are identical. Fluctuations at the HV-side are due to interference of the electronic supply and load. 280
14.8 Excerpt of the measurement in Fig.14.7: Four parallel connected DC-DC converters, which operate with analog, droop-based control in buck mode, are connected at the HV-side to an electronic supply and at the LV-side to an electronic load which generates rectangular load jumps between $6A$ and $10A$. The reference voltages and the droop resistors are identical. Fluctuations at the HV-side are due to interference of the electronic supply and load. 281
14.9 Excerpt of the measurement in Fig.14.7: Four parallel connected DC-DC converters, which operate with analog, droop-based control in buck mode, are connected at the HV-side to an electronic supply and at the LV-side to an electronic load which generates rectangular load jumps between $6A$ and $10A$. The reference voltages and the droop resistors are identical. Fluctuations at the HV-side are due to interference of the electronic supply and load. 282
14.10 Two DC-DC converters (ID 3, ID 4) are connected in parallel and operate in boost mode. They are connected to a ohmic load at the HV-side. The digital load distribution control without FMAC with fixed sharing factors of $\alpha_{\mathrm{ID\,3}} = 20\%$ and $\alpha_{\mathrm{ID\,4}} = 80\%$ is used. The load sharing gain factor is high at 0.3. The sharing accuracy is increased. However, the high gain factor also leads to high output currents and eventual to the occurrence of the overvoltage protection state. At the time $t = 11\,s$ the overvoltage protection leads to the deactivation of the DC-DC converter ID 3. The DC-DC converter ID 4 takes over a majority of the load current and the high side voltage remains at $23\,V$. 287

14.11 Digital load sharing control without FMAC with a parallel connection of two DC-DC converters (ID 3, ID 4) and a fixed load sharing of 20% (ID 3) and 80% (ID 4). The load sharing gain factor of 0.25 results in higher current distribution accuracy. Due to the lower gain factor, the output currents are also lower and consequently the probability of the occurrence of the overvoltage protection state is also lower. The higher gain factor still results in voltage fluctuations. 288
14.12 The two DC-DC converters (ID 3, ID 4) connected in parallel operate in boost mode. At the HV-side an electronic load is connected generating rectangular load steps from $3A$ to $9A$. The digital load distribtution control with fixed sharing factors of 30% (ID 4) and 70% (ID 3) and a gain factor of 0.25 is used. With the high voltage to be regulated, overshoots and undershoots of up to $\delta V = 1.2V$ occur at the time of the load current change. Reducing the gain factor results in a reduction of the magnitude of these. 289
14.13 Two DC-DC converters (ID 3, ID 4) are connected in parallel and connected to a ohmic load at the HV-side. They operate in boost mode. Communication based digital control without FMAC is used and a fixed load sharing of 30% (ID 3) and 70% (ID 4). The gain factor of the load distribution is low with 0.1. Deviations in load distribution occur and amount to up to 5%, especially at low currents. This results in a load sharing of 25% (ID 3) and 75% (ID 4). An ohmic load is used. 290
14.14 Load sharing between two parallel connected DC-DC converters (ID 1, ID 3) operating in buck mode. The digital load distribution control is used without using the FMAC. A fixed load sharing of 30% (ID 1) and 70% (ID 3) is chosen. The gain factor of the load distribution (g_{dis}) is low and equals 0.1. The actual load distribution is approximately 35% (ID 1) to 65% (ID 3). An ohmic load is used. . 291
14.15 Load sharing between two DC-DC converters connected in parallel (ID 1, ID 3) operating in buck mode. The digital load distribution control is applied without using the FMAC. A fixed load distribution of 30% (ID 1) and 70% (ID 3) is selected. The gain factor of the load sharing (g_{dis}) is low and is 0.1. The accuracy of the load sharing increases with higher load currents. Even high load current jumps, such as 16.5 A at $t \approx 9s$ in this case, do not affect the voltage to be controlled (V_{LV}). An ohmic load is used. 292
14.16 Four DC-DC converters in parallel are connected at the HV-side to an electronic load with a constant current of $12A$. For the control, the communication-based, digital one with FMAC and the following distribution factors is used $\alpha_{\text{ID1}} = 35\%$, $\alpha_{\text{ID2}} = 25\%$, $\alpha_{\text{ID3}} = 20\%$, $\alpha_{\text{ID4}} = 20\%$. 293
14.17 Excerpt of Fig. 14.16: Four DC-DC converters in parallel are connected at the HV-side to an electronic load with a constant current of $12A$. For the control, the communication-based, digital one with FMAC and the following distribution factors is used $\alpha_{\text{ID1}} = 35\%$, $\alpha_{\text{ID2}} = 25\%$, $\alpha_{\text{ID3}} = 20\%$, $\alpha_{\text{ID4}} = 20\%$. 294

14.18 Two DC-DC converters operating in buck mode are connected at the LV-side with an electronic load which first generates a constant load current of $11A$, then suddenly drops to $3A$ and ramps up to $11A$ again. Communication-based, digital control with FMAC is used and an identical distribution factor of $\alpha = 50\%$. Deviations in the load current distribution occur over the entire load current range, with a maximum of 3% or $0.5A$. The load change from $11A$ to $3A$ at $t = 6.5s$ results in a voltage rise to a maximum of $13.6V$. 295

14.19 Two DC-DC converters operating in buck mode are connected at the LV-side with an electronic load which generates rectangular load steps between $63A$ and $13A$. Communication-based, digital control with FMAC and identical distribution factors of $\alpha = 50\%$ is used. Deviations in the load current distribution occur over the entire load current range, with a maximum of 3% or $0.5A$. When the load current value changes, voltage deviations of $\pm 0.3V$ occur. 296

14.20 Four DC-DC converters connected in parallel operate in boost mode and are connected on the HV-side with an electronic load which generates a load current of $11A$. Communication-based digital control is used and the values of the distribution factors are changed. Initially, the distribution factors are $\alpha_{ID1} = 70\%$, $\alpha_{ID2} = 10\%$, $\alpha_{ID3} = 10\%$, $\alpha_{ID4} = 10\%$. At time $t = 42.9s$ they are changed to $\alpha = 25\%$ each and at time $t = 60.7s$ to $\alpha_{ID1} = 20\%$, $\alpha_{ID2} = 25\%$, $\alpha_{ID3} = 5\%$, $\alpha_{ID4} = 50\%$. The current changes without significant delay and the deviations are small. 298

14.21 Four DC-DC converters connected in parallel operate in boost mode and are connected at the HV-side to an electronic load which generates a rectangular load current of $6A$ and $13A$. For the control, the communication-based digital one with FMAC is used. Initially, all distribution factors are identical and equal to $\alpha = 25\%$. At time $t = 9.2s$, the value of the distribution factors changes to $\alpha_{ID1} = 15\%$, $\alpha_{ID2} = 25\%$, $\alpha_{ID3} = 7\%$, $\alpha_{ID4} = 53\%$. The quantization errors that occur when using the FMAC and their effects on the output currents are evident. The voltage to be controlled (V_{HV}) remains stable. Fluctuations on the LV-side are due to interferences between the electronic load and supply. 299

14.22 Four parallel DC-DC converters in buck mode are connected at the LV-side to an electronic load with a constant load current of $14A$. The communication-based digital control with FMAC is used for the control. At the beginning, the distribution factors are $\alpha_{ID1} = 20\%$, $\alpha_{ID2} = 25\%$, $\alpha_{ID3} = 35\%$, $\alpha_{ID4} = 20\%$. At $t = 11s$, they are changed to $\alpha_{ID1} = 10\%$, $\alpha_{ID2} = 25\%$, $\alpha_{ID3} = 5\%$, $\alpha_{ID4} = 60\%$. The change has no effect on the voltage to be controlled and the deviations in the load current distribution are marginal, but increasing with lower output current values. 300

14.23 Four DC-DC converters connected in parallel are connected at the HV-side to an electronic load with a constant load current of $12A$. Initially up to $t = 30s$ the DC-DC converters operate in the droop-based control with adjusted reference voltages and identical droop resistors. After that they change to the communication-based, digital control using the FMAC with a load sharing of $\alpha_{ID1} = 30\%$, $\alpha_{ID2} = 25\%$, $\alpha_{ID3} = 20\%$, $\alpha_{ID4} = 25\%$. The change between the two control methods does not affect the voltage to be controlled (V_{HV}). 301
14.24 Start-up of the system with four DC-DC converters operating in boost mode with droop-based control. The droop resistors used are identical ($R_d = 0.1\Omega$) and individual output characteristics ($V_{ref,ID1} = 2V$, $V_{ref,ID2} = 1.87V$, $V_{ref,ID3} = 2.02V$, $V_{ref,ID3} = 2V$) are considered. The DC-DC converter ID1 has an incorrect LV voltage measurement. The output current of the DC-DC converter ID 1 exhibits an overshoot of about $0.5A$. A possible reason for this is that the DC-DC converters are not started simultaneously. In this case, the DC-DC converter ID 1 starts first and measures the largest deviation in comparison to the remaining ones started slightly later. 304
14.25 Start-up of the system consisting of four parallel connected DC-DC converters and an electronic load at the HV-side which generates a ramped load current (0 to $10A$ in $5s$). The election process was completed approximately at $t = 17s$ and the control scheme switched from droop to communication-based control. The distribution factors are initially all identical and equal to $\alpha = 25\%$. At $t = 40s$ they are changed to $\alpha_{ID1} = 30\%$, $\alpha_{ID2} = 20\%$, $\alpha_{ID3} = 25\%$, $\alpha_{ID4} = 25\%$. For the digital control, the FMAC of the microcontroller is used. 305
14.26 Four parallel DC-DC converters operating in boost mode are connected at the HV-side with an electronic load which generates rectangular load steps between $6A$ and $13A$. Initially, the DC-DC converters operate in droop mode with adjusted reference voltages and different droop resistors ($R_{d,ID1} = 0.1\Omega$, $V_{ref,ID1} = 2V$, $R_{d,ID2} = 0.7\Omega$, $V_{ref,ID2} = 1.87V$, $R_{d,ID3} = 0.7\Omega$, $V_{ref,ID3} = 2.02V$, $R_{d,ID4} = 0.7\Omega$, $V_{ref,ID4} = 2V$). Afterwards they switch to digital control with FMAC with identical division factors of $\alpha = 25\%$. Fluctuations on the LV-side occur due to interference between the electronic supply and load. 306
14.27 Parallel connection of four DC-DC converters operating in buck mode. The droop-based control with adapted droop resistors and reference voltages is used ($R_{d,ID1} = 0.7\Omega$, $V_{ref,ID1} = 2V$, $R_{d,ID2} = 0.3\Omega$, $V_{ref,ID2} = 1.87V$, $R_{d,ID3} = 1.2\Omega$, $V_{ref,ID3} = 2.02V$, $R_{d,ID4} = 0.7\Omega$, $V_{ref,ID4} = 2V$). The DC-DC converter ID 2 is deactivated and the remaining ones take over the load current. No significant voltage (V_{LV}) changes occur. The LV-measurement of the DC-DC converter 1 is incorrect. 309

14.28 Incorrect total current: The three DC-DC converters operating in buck mode are connected in parallel and use the communication-based digital control with direct calculation by the microcontroller with an erroneous fixed value for the total current of $2A$. The division factors are identical with the value 33%. An electronic load connected at the LV-side is generating rectangular load jumps between $5A$ and $8A$. The voltage control to the set point shows no significant deviation while deviations occur in the load current distribution. This proofs that the voltage control is independent of the load current distribution control. 310

A.1 Step response in buck mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. 393

A.2 Closed current control loop in buck mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. Up to a frequency of 3 kHz the gain is approximately constant and is $G_0 = 22\,dB$. At a frequency of $f_\mathrm{p} = 14.5\,kHz$ there is a conjugate complex pole with an increase of $4.5\,dB$ over G_0 (total $26.5\,dB$) and a subsequent magnitude decrease of $-40\frac{dB}{dec}$. The phase change results in $-180\frac{^\circ}{dec}$. A zero at a frequency of $f_\mathrm{z} = 2.8\,kHz$ attenuates the decay of the gain to $-20\frac{dB}{dec}$ and causes a phase change of $+90^\circ$ and a resulting decay of the phase of $-90\frac{^\circ}{dec}$. The crossover frequency is $f_\mathrm{c} = 170\,kHz$. The phase and magnitude reserve are satisfactory for stability. For the position of the poles and zeros, a comparison with the Bode diagrams of the duty cycle to current transfer function $G_\mathrm{id}(s)$ in figure 7.7 on p.117 is helpful. 394

A.3 Output current to output voltage transfer function $G_\mathrm{vi}(s)$ in buck mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. Up to a frequency of $50\,Hz$, the gain is approximately constant and is $G_0 = 22\,dB$. At a frequency $f_p = 20\,Hz$ a pole position occurs and consequently a decrease in the magnitude $-20\frac{dB}{dec}$ of and a phase change of $-90\frac{^\circ}{dec}$. At a frequency of $f_z = 400\,Hz$ and $f_z = 10\,kHz$, a zero occurs respectively with a magnitude change of $+20\frac{dB}{dec}$and a phase change of $+90\frac{^\circ}{dec}$. The crossover frequency is $f_\mathrm{c} = 181\,Hz$. For the position of the poles and zeros, Bode plots of the calculated transfer function of the output current to the output voltage $G_\mathrm{vi}(s)$ in figure 7.9 on p.119 are helpful. 395

A.4 Open uncontrolled control loop in buck mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. 396

A.5 The open controlled control loop in buck mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$ approximately exhibits the behavior of an I-compensator. The crossover frequency is $f_\mathrm{c} = 2\,kHz$. 396

A.6 Step response in buck mode and DCM with a load resistance of $R_\mathrm{l} = 1\,k\Omega$. 397

A.7 Closed current control loop in buck mode and DCM with a load resistance of $R_\mathrm{l} = 1\,k\Omega$. Up to a frequency of $200\,Hz$ the gain is approximately constant and equals $G_0 = 22.4\,dB$. At a frequency $f_p = 100\,Hz$ a pole position occurs followed by a magnitude decrease of $-20\frac{dB}{dec}$ of and a phase change of $-90\frac{^\circ}{dec}$. Two zeros occur at a frequency of $f_z = 2\,kHz$ and $f_z = 5\,kHz$ respectively causing a magnitude change of $+20\frac{dB}{dec}$ and a phase change of $+90\frac{^\circ}{dec}$. Consequently, two pole positions occur in the frequency range between $f_p = 50\,kHz$ and $f_p = 100\,kHz$. The crossover frequency is $f_\mathrm{c} = 6.75\,kHz$. For the position of the poles and zeros, Bode plots of the calculated duty cycle to current $G_\mathrm{id}(s)$ in figure 7.12 on p.121 are helpful. 397
A.8 Output current to output voltage transfer function $G_\mathrm{vi}(s)$ in buck mode and DCM with a load resistance of $R_\mathrm{l} = 1\,k\Omega$. Up to a frequency of $1\,kHz$, the gain decreases with $-20\frac{dB}{dec}$. The phase is approximately constant at $-90\circ$. The pole responsible for this occurs at very low frequencies and is not recognizable within the bode plot. At a frequency of $f_z = 2\,kHz$ a zero occurs and causes a magnitude change of $+20\frac{dB}{dec}$ and a phase change of $+90\frac{^\circ}{dec}$. The crossover frequency is $f_\mathrm{c} = 210\,Hz$. For the position of the poles and zeros, Bode plots of the calculated transfer function of the output current to the output voltage $G_\mathrm{vi}(s)$ in figure 7.9 on p.119 are helpful. 398
A.9 Open uncontrolled control loop in buck mode and DCM with a load resistance of $R_\mathrm{l} = 1\,k\Omega$. 399
A.10 Open uncontrolled control loop in buck mode and DCM with a load resistance of $R_\mathrm{l} = 1\,k\Omega$. The orange line shows the approximation. It shows approximately the behavior of an I-compensator. The crossover frequency is $f_\mathrm{c} \approx 1\,kHz$. 399
A.11 Step response in boost mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. 400
A.12 Closed current control loop in boost mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. Up to a frequency of $5\,kHz$ the gain is approximately constant and equal to $G_0 = 22.5\,dB$. The phase is constantly 0° within that frequency range. At a frequency of approximately $f_\mathrm{p} = 20\,kHz$ a pole occurs and leads to a change in the magnitude and phase response. The magnitude decreases with $-20\frac{dB}{dec}$ and the phase with $-90\frac{^\circ}{dec}$. The crossover frequency is $f_\mathrm{c} = 278\,kHz$. For the position of the poles and zeros, Bode plots of the calculated duty cycle to current transfer functions $G_\mathrm{id}(s)$ in figure 7.16 on p.126 are helpful. 400
A.13 Output current to output voltage transfer function $G_\mathrm{vi}(s)$ in boost mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. For the position of the pole and zeros, Bode plots of the calculated transfer function of the output current to the output voltage $G_\mathrm{vi}(s)$ in figure 7.17 on p.128 are helpful. 401
A.14 Open uncontrolled control loop in boost mode and DCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. 401
A.15 Open controlled control loop in boost mode and DCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. 402

A.16 Step response in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$. 402
A.17 Closed current control loop in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$. For the position of the poles and zeros, Bode plots of the calculated duty cycle to current transfer functions $G_{id}(s)$ in figure 7.20 on p.130 are helpful. 403
A.18 Output current to output voltage transfer function $G_{vi}(s)$ in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$. 403
A.19 Open uncontrolled control loop in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$. 404
A.20 Open controlled control loop in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$. 404

List of Tables

2.1 Applications, commonly used electrode materials therein and their electrical characteristics. [37–42] 13
2.2 Overview of a selection of common post-lithium battery systems, their key advantages and disadvantages as well as their gravimetric capacity [26, 145]. 20

3.1 Evaluation of existing battery management system topologies in terms of reliability, scalability and flexibility. 39

4.1 Measured message processing times for various transmission rates and user data bytes. 53
4.2 Current consumption of the peripheral units 58
4.3 BER of CAN and Ethernet for different environments [277]. 59
4.4 Comparison of the message processing time and the message unpacking time. 60
4.5 Summary of the comparative analysis of CAN, CAN FD and Ethernet. 61
4.6 Summary of the results of the comparative analysis of CAN, CAN FD and Ethernet. 63

5.1 Transfer conditions (T_i) of the state machine in case of leader election 73
5.2 Composition of the priority identifiers of the election messages for the Big and Small LEA-CAN 81
5.3 Minimal and maximal length in bit of election messages 84
5.4 Transmission duration of CAN (FD) messages 84
5.5 Error handling of the implemented LEA 87

6.1 Description of the transfer conditions and assignment of the control strategies to the different operating states. 104

7.1 Specification of the equivalent circuit elements. d is the duty cycle, T_s is the period, and $V = V_{HV}$ is the small-signal voltage change [356]. 118
7.2 Specification of the equivalent circuit elements. d is the duty cycle of the transistor, T_s is the period, and V is the small-signal voltage change [356]. 127
7.3 Poles and zeroes of the transfer functions for CCM and DCM in buck [383] and in boost [384] mode of a bidirectional DC-DC converter. 134

8.1 Key figures and components values for each of the two channels . . 160

10.1 Most common battery hazards, their consequences and parameters to be monitored in order to avoid them. 203

11.1 Component dimensioning of the two half bridges [499] 214
11.2 Relation between duty cycle and the control signals of the transistors 218

12.1 Instructions and examples of the transmission protocol 240

13.1 Overview of different DC-DC converters, which have been adapted to the requirements of the DBMS [388, 520, 523, 524]. 250
13.2 Electronic features of the DC-DC converter D3806 [520]. 252
13.3 Electronic features of the DC-DC converter DPS5015 [524]. 253
13.4 Electronic features of the DC-DC converter LM3150 [523] 253
13.5 Ratio between microcontroller voltage and output voltage 254
13.6 Electronic features of the bidirectional DC-DC converter based on the chip LM5170 [335]. 255
13.7 Function table for the analog switch of the ISET switch circuit [526]. 257

14.1 Mean and maximum deviation of the measurement shown in figure 14.16 on p. 293. 285

Abbreviations

MOSFET Metal Oxide Semiconductor Field Effect Transistor 123

ACMC Average Current Mode Control 125

ADC Analog Digital Converter 291

AHB Advanced high-performance bus 66

APB Advanced periperhal bus 66

BCM Boundary Conduction Mode 123

BER Bit Error Rates 51

BMS Battery Management System 3

BoL Begin of Life 32

CAN Controller Area Network xx

CAN XL Controller Area Network Extra Long 69

CAN (FD) Controller Area Network and Controller Area Network Flexible Data-rate 53

CAN FD Controller Area Network Flexible Data-rate xx

CCM Continuous Conduction Mode xxii

CMC Current Mode Control 125

CO_2 Carbon Dioxide 1

COTF Control to Output Transfer Function 125

CRC Cyclic Redundancy Check 55

DAC Digital Analog Converter 285

DBMS Decentralized Battery Management System 8

DC Direct Current 4

DCA Direct Code Analysis 65

DCM Discontinuous Conduction Mode xxii

DDCC Direct Duty Cycle Control 154

DIP Dual In-line Package 297

EEE Energy Efficient Ethernet 69

EMI Electromagnetic Interference 38

EoL End of Life 33

FIFO First In First Out xx

FPGA Field Programmable Gate Array 198

FreeRTOS Free Real Time Operating System 55

GPIO General Purpose Input Output 57

HAL Hardware Abstraction Layer 56

I^2C Inter-Integrated Circuit 285

ID Identifier 76

IEEE Institute of Electrical and Electronics Engineers 69

IP Internet Protocol 54

LA Lead Acid 14

LCO Lithium Cobalt Oxide 16

LCU Local Control Unit 45

LEA Leader Election Algorithm 74

LEA-CAN Controller Area Network (CAN and CAN FD) based Leader Election Algorithm 75

LFP Lithium iron phosphate 16

LMO Lithium Manganese Oxide 16

LNO Lithium Nickel Oxide 17

LNO Nickel Cobalt Aluminum Oxide 16

LOTF Line to Output Transfer Function 125

lwIP Lightweight Internet Protocol 55

MOST Media Oriented Systems Transport 55

Na-$NiCl_2$ Sodium Nickel Chloride 15

NaS Sodium Sulfur 15

NiCd Nickel Cadmium 14

NiMH Nickel Metal Hydride 14

NMC Nickel Manganese Cobalt Oxide 16

NW Node Weight 76

OOA Optimized Operating Area 11

OSI Open Systems Interconnection 54

PCB Printed Circuit Board 10

PCC Power Consumption Calculator 58

PCMC Peak Current Mode Control 125

PHY Physical Layer 56

PWM Pulse Width Modulation 122

RER Residual Error Rates 51

RHPZ Right Half Plane Zero 145

RPE Residual Package Error 59

RTSP Real-Time Streaming Protocol 54

RUL Remaining Useful Life 32

SEI Solid Electrolyte Interphase 20

SLI Starting Lighting Ignition 14

SOA Safe Operating Area 3

SoC State of Charge 3

SoE State of Energy 31

SoF State of Function 30

SoH State of Health 3

SoP State of Power 28

SoS State of Safety 30

SPI Serial Peripheral Interface 297

TCP Transmission Control Protocol 53

TP Twisted Pair 53

TSN Time Sensitive Networking 69

UART Universal Asynchronous Receiver / Transmitter 285

UDP User Datagram Protocol 53

USB Universal Serial Bus 57

UTP Unshielded Twisted Pair 57

VFC Voltage Feedforward Control 155

Symbols

Symbol	Description	Unit
A_i	Possible error patterns	
C_N	Nominal capacity	Ah
C_grav	Gravimetric capacity	$\frac{mAh}{g}$
C_rem	Actual available discharge capacity	Ah
C_vol	Volumetric capacity	$\frac{mAh}{cm^3}$
C_T	Theoretical capacity	$C = Ah$
C_act	Actual capacity	Ah
C_rel	Released capacity	Ah
C	Capacitor	F
D	Hamming distance	
D	Discriminant	
E_act	Actual vailable energy	Wh
E_grav	Gravimetric energy density	$\frac{Wh}{kg}$
F	Faraday constant, electric charge per mole of elementary charges	96485.309 $\frac{C}{mol}$
$G_\mathrm{C}(s)$	Transfer function of the load current distribution controller	
$G_\mathrm{I}(s)$	Transfer function of the current controller	
$G_\mathrm{PWM}(s)$	Transfer function of the PWM generator	
$G_\mathrm{V}(s)$	Transfer function of the voltage controller	
$G_\mathrm{c,i}$	Closed current control loop	
$G_\mathrm{meas}(s)$	Transfer function of the measurement (feedback)	
$G_\mathrm{o,i}(s)$	Open current control loop	
G_PWM	Transfer function PWM generator	
$G_\mathrm{id,A}(s)$	Approximation of the duty cycle to current transfer function neglecting the resonance overshoot	
$G_\mathrm{id,hf}(s)$	Duty cycle to current transfer function at high frequencies	
$G_\mathrm{id,lf}(s)$	Duty cycle to current transfer function at low frequencies	
$G_\mathrm{id}(s)$	Duty cycle to current transfer function	
$G_\mathrm{ig}(s)$	Input voltage disturbances to voltage transfer function	
$G_\mathrm{o,c}$	Open controlled loop	
$G_\mathrm{o,u}$	Open uncontrolled loop	
$G_\mathrm{o,v}$	Open loop of the voltage control	
$G_\mathrm{vd}(s)$	Duty cycle to voltage transfer function	
$G_\mathrm{vg}(s)$	Input voltage disturbances to voltage transfer function	
$G_\mathrm{vi}(s)$	Output current to output voltage transfer function	
H_s	Transfer function of the closed current control loop	
$I_\mathrm{L,set}$	Static setpoint current through the inductor	A
I_L	Static current through the inductor	A
I_out	Static output current	A
I_LV	Static current at the low side of the DC-DC converter	A
I	Static current	A
K	Gain factor	
K	Gain constant	
Mw	Molecular weight	$\frac{g}{mol}$
N_Data	Length of the data	

Symbol	Description	Unit
PWM_{ISETD}	PWM signal to specify the output current of the DC/DC converter	
P_{lower}	Lower limit of the probability of an undetected error	
P_{upper}	Upper limit of the probability of an undetected error	
P	Static power	W
Q	Electric charge	$C = A \cdot s$
R_{C}	Equivalent parasitic resistance of the capacitor	Ω
R_{Shunt}	Shunt resistor	Ω
R_{l}	Load resistance	Ω
R_{x}	Equivalent parasitic resistance of the shunt and the indcutor	Ω
R	Resistor	Ω
T_{HS}	High side MOSFET	
T_{LS}	Low side MOSFET	
T_i	Transfer conditions for state machines	
T_{s}	Switching periode, periode of the PWM signal to drive the transistors	s
T	Temperature	°C
T	Time constant	
V_{l}	Input voltage	V
V_{ISETA}	Reference voltage to specify the output current of the DC/DC converter	V
V_{Shunt}	Static voltage over the Shunt Resistor	V
V_{e}	Voltage across the inductor	V
$V_{\mathrm{i,set}}$	Static current-proportional setpoint voltage	V
V_{in}	Static input voltage	V
V_{out}	Static output voltage	V
V_{set}	Setpoint voltage	V
V_{st}	Amplitude of the sawtooth voltage	V
V_{HV}	Static voltage at the high side of the DC-DC converter	V
V_{LV}	Static voltage at the low side of the DC-DC converter	V
$V_{\mathrm{g}}(t)$	Static uncontrolled input voltage, small signal disturbance input	V
α	Load distribution factor	
η_{C}	Coulomb efficiency	
ρ	Battery (cell) density	$\frac{kg}{m^3}$
τ	RC time constant	s
d_{CCM}	Duty cycle to determine the on-times of the switches in continuous conduction mode	
d	Duty cycle	
f_{c}	Crossover frequency	Hz
f_{s}	Switching frequency	Hz
f	Hazard function indicating failure probabilities	
$i_{\mathrm{L,BCM}}(t)$	Time varying inductor current in boundary conduction mode	A
$i_{\mathrm{L,CCM}}(t)$	Time varying inductor current in continuous conduction mode	A
$i_{\mathrm{L,DCM}}(t)$	Time varying inductor current in discontinuous conduction mode	A
i_{L}	Time varying current through the inductor	A
i_{out}	Time varying output current	A
i_{LV}	Time varying current at the high side of the DC-DC converter	A
i	Time varying current	A
n	Number of charge carrier or number of paricipants	
p_{error}	Probability of a bit error	
p	Time varying power	W
r_{d}	Variable droop resistor	Ω
r_{CRC}	Degree of the generator polynomial of the CRC	
t	Time	s
v_{Shunt}	Time varying voltage over the Shunt Resistor	V
v_{c}	Controller output voltage	V
$v_{\mathrm{i,set}}$	Current-proportional setpoint voltage	V

Symbol	Description	Unit
v_{in}	Time varying input voltage	V
v_{oc}	Time varying open collector voltage	V
v_{out}	Time varying output voltage	V
v_{st}	Sawtooth voltage	V
$v_{\text{G}}(t)$	PWM signal to drive the transistors	V
v_{HV}	Time varying voltage at the high side of the DC-DC converter	V
v_{LV}	Time varying voltage at the high side of the DC-DC converter	V
$v_{\text{g}}(t)$	Time varying uncontrolled input voltage, small signal disturbance input	V
v	Time varying voltage	V
$\lvert I_{\text{Safe}} \rvert$	Absolute value of the battery (dis)charge current considering the safe operating area	A

References

[1] J. E. Walsh, T. J. Ballinger, E. S. Euskirchen, E. Hanna, J. Mård, J. E. Overland, H. Tangen, and T. Vihma, "Extreme weather and climate events in northern areas: A review", *Earth-Science Reviews*, vol. 209, p. 103 324, 2020, ISSN: 0012-8252. DOI: https://doi.org/10.1016/j.earscirev.2020.103324. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0012825220303706.

[2] H. Ritchie, M. Roser, and P. Rosado, "Co^2 and greenhouse gas emissions", *Our World in Data*, 2020. [Online]. Available: https://ourworldindata.org/co2-and-other-greenhouse-gas-emissions.

[3] A. G. Olabi and M. A. Abdelkareem, "Renewable energy and climate change", *Renewable and Sustainable Energy Reviews*, vol. 158, p. 112 111, 2022, ISSN: 1364-0321. DOI: https://doi.org/10.1016/j.rser.2022.112111. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1364032122000405.

[4] K. O. Yoro and M. O. Daramola, "Co2 emission sources, greenhouse gases, and the global warming effect", in *Advances in Carbon Capture*, M. R. Rahimpour, M. Farsi, and M. A. Makarem, Eds., Woodhead Publishing, 2020, pp. 3–28, ISBN: 978-0-12-819657-1. DOI: https://doi.org/10.1016/B978-0-12-819657-1.00001-3. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128196571000013.

[5] E. Mathieu and L. Rodés-Guirao, "What are the sources for our world in data's population estimates?", *Our World in Data*, 2022, https://ourworldindata.org/population-sources. [Online]. Available: https://ourworldindata.org/grapher/population-regions-with-projections?time=1800..2100.

[6] U. Nations, *Paris agreement*, https://unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement, [Online; accessed October-2022], 2015.

[7] U. Nations, *Kyoto protocol*, https://unfccc.int/kyoto_protocol, [Online; accessed October-2022], 1998.

[8] Y. Santana-Falcón and R. Séférian, "Climate change impacts the vertical structure of marine ecosystem thermal ranges", *Nature Climate Change*, pp. 1–8, 2022. DOI: https://doi.org/10.1038/s41558-022-01476-5.

[9] K. Duffy, T. C. Gouhier, and A. R. Ganguly, "Climate-mediated shifts in temperature fluctuations promote extinction risk", *Nature Climate Change*, 2022. DOI: https://doi.org/10.1038/s41558-022-01490-7.

[10] H. Zhang, M. Väliranta, G. T. Swindles, M. A. Aquino-López, D. Mullan, N. Tan, M. Amesbury, K. V. Babeshko, K. Bao, A. Bobrov, *et al.*, "Recent climate change has driven divergent hydrological shifts in high-latitude peatlands", *Nature communications*, vol. 13, no. 1, pp. 1–7, 2022. DOI: https://doi.org/10.1038/s41467-022-32711-4.

[11] E. Commission, *The european green deal*, https://eur-lex.europa.eu/legal-content/EN/TXT/?qid=1588580774040&uri=CELEX:52019DC0640, [Online; accessed October-2022], 2019.

[12] D. Bundestag, *Bundes-klimaschutzgesetz (ksg)*, [Abschnitt 2, Klimaschutzziele und Jahresemissionsmengen §3 Nationale Klimaschutzziele], 2021.

[13] D. Gielen, F. Boshell, D. Saygin, M. D. Bazilian, N. Wagner, and R. Gorini, "The role of renewable energy in the global energy transformation", *Energy Strategy Reviews*, vol. 24, pp. 38–50, 2019, ISSN: 2211-467X. DOI: https://doi.org/10.1016/j.esr.2019.01.006. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2211467X19300082.

[14] M. A. Destek, M. Manga, O. Cengiz, and G. Destek, "Investigating the potential of renewable energy in establishing global peace: Fresh evidence from top energy consumer countries", *Renewable Energy*, vol. 197, pp. 170–177, 2022.

[15] I. Overland, J. Juraev, and R. Vakulchuk, "Are renewable energy sources more evenly distributed than fossil fuels?", *Renewable Energy*, vol. 200, pp. 379–386, 2022, ISSN: 0960-1481. DOI: https://doi.org/10.1016/j.renene.2022.09.046. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0960148122013969.

[16] T. Z. Ang, M. Salem, M. Kamarol, H. S. Das, M. A. Nazari, and N. Prabaharan, "A comprehensive study of renewable energy sources: Classifications, challenges and suggestions", *Energy Strategy Reviews*, vol. 43, p. 100 939, 2022.

[17] S. R. Sinsel, R. L. Riemke, and V. H. Hoffmann, "Challenges and solution technologies for the integration of variable renewable energy sources—a review", *renewable energy*, vol. 145, pp. 2271–2285, 2020.

[18] I. Worighi, A. Maach, A. Hafid, O. Hegazy, and J. Van Mierlo, "Integrating renewable energy in smart grid system: Architecture, virtualization and analysis", *Sustainable Energy, Grids and Networks*, vol. 18, p. 100 226, 2019.

[19] I. M. Peters, C. Breyer, S. A. Jaffer, S. Kurtz, T. Reindl, R. Sinton, and M. Vetter, "The role of batteries in meeting the pv terawatt challenge", *Joule*, vol. 5, no. 6, pp. 1353–1370, 2021.

[20] J. B. Dunn, L. Gaines, J. C. Kelly, C. James, and K. G. Gallagher, "The significance of li-ion batteries in electric vehicle life-cycle energy and emissions and recycling's role in its reduction", *Energy & Environmental Science*, vol. 8, no. 1, pp. 158–168, 2015.

[21] S. Rothgang, T. Baumhöfer, H. van Hoek, T. Lange, R. W. De Doncker, and D. U. Sauer, "Modular battery design for reliable, flexible and multi-technology energy storage systems", *Applied Energy*, vol. 137, pp. 931–937, 2015.

[22] J. Deng, C. Bae, A. Denlinger, and T. Miller, "Electric vehicles batteries: Requirements and challenges", *Joule*, vol. 4, no. 3, pp. 511–515, 2020.

[23] K. W. See, G. Wang, Y. Zhang, Y. Wang, L. Meng, X. Gu, N. Zhang, K. C. Lim, L. Zhao, and B. Xie, "Critical review and functional safety of a battery management system for large-scale lithium-ion battery pack technologies", *International Journal of Coal Science & Technology*, vol. 9, no. 1, pp. 1–17, 2022.

[24] H. Dai, B. Jiang, X. Hu, X. Lin, X. Wei, and M. Pecht, "Advanced battery management strategies for a sustainable energy future: Multilayer design concepts and research trends", *Renewable and Sustainable Energy Reviews*, vol. 138, p. 110 480, 2021.

[25] G. Xu, X. Du, Z. Li, X. Zhang, M. Zheng, Y. Miao, Y. Gao, and Q. Liu, "Reliability design of battery management system for power battery", *Microelectronics Reliability*, vol. 88, pp. 1286–1292, 2018.

[26] F. Duffner, N. Kronemeyer, J. Tübke, J. Leker, M. Winter, and R. Schmuch, "Post-lithium-ion battery cell production and its compatibility with lithium-ion cell production infrastructure", *Nature Energy*, vol. 6, no. 2, pp. 123–134, 2021.

[27] L. C. Casals, M. Barbero, and C. Corchero, "Reused second life batteries for aggregated demand response services", *Journal of cleaner production*, vol. 212, pp. 99–108, 2019.

[28] E. Martinez-Laserna, I. Gandiaga, E. Sarasketa-Zabala, J. Badeda, D.-I. Stroe, M. Swierczynski, and A. Goikoetxea, "Battery second life: Hype, hope or reality? a critical review of the state of the art", *Renewable and Sustainable Energy Reviews*, vol. 93, pp. 701–718, 2018.

[29] M. Placek, *Estimated capacity of lithium-ion batteries placed on the global market in 2020 with forecast for 2021 through 2030 (in gigawatt hours)*, `https://www.statista.com/statistics/1246914/capacity-of-lithium-ion-batteries-placed-on-the-global-market/`, [Statista, Metals & Electronics], 2022.

[30] B. S. Advisors, "Battery production today and tomorrow", *Study of the battery production market, VII*, 2018. [Online]. Available: `http://www.berylls.com/wp-content/uploads/2018/03/20180308_Studie_E-Mobilitaet_EN.pdf`.

[31] EIA, "Electricity net consumption in germany from 2000 to 2021 (in terawatt-hours)", *Statista*, 2022. [Online]. Available: `https://www.statista.com/statistics/383650/consumption-of-electricity-in-germany/`.

[32] W. Han, A. Kersten, C. Zou, T. Wik, X. Huang, and G. Dong, "Analysis and Estimation of the Maximum Switch Current During Battery System Reconfiguration", *IEEE Transactions on Industrial Electronics*, vol. 69, no. 6, pp. 5931–5941, 2022. DOI: `10.1109/TIE.2021.3091923`.

[33] N. Ghanbari and S. Bhattacharya, "Adaptive Droop Control Method for Suppressing Circulating Currents in DC Microgrids", *IEEE Open Access Journal of Power and Energy*, vol. 7, pp. 100–110, 2020.

[34] D. Linden and T. Reddy, *Handbook of Batteries*. McGraw-Hill Professional, 2001, ISBN: 978-0-07-135978-8.

[35] U. Koehler, "General overview of non-lithium battery systems and their safety issues", *Electrochemical Power Sources: Fundamentals, Systems, and Applications*, pp. 21–46, 2019.

[36] P. Kurzweil and K. Brandt, "Overview of rechargeable lithium battery systems", in *Electrochemical Power Sources: Fundamentals, Systems, and Applications*, Elsevier, 2019, pp. 47–82.

[37] G. E. Blomgren, "The development and future of lithium ion batteries", *Journal of The Electrochemical Society*, vol. 164, no. 1, A5019, 2016.

[38] S. Choi and G. Wang, "Advanced lithium-ion batteries for practical applications: Technology, development, and future perspectives", *Advanced Materials Technologies*, vol. 3, no. 9, p. 1 700 376, 2018.

[39] M. Armand, P. Axmann, D. Bresser, M. Copley, K. Edström, C. Ekberg, D. Guyomard, B. Lestriez, P. Novák, M. Petranikova, *et al.*, "Lithium-ion batteries–current state of the art and anticipated developments", *Journal of Power Sources*, vol. 479, p. 228 708, 2020.

[40] Q. Wang, N. Tian, K. Xu, L. Han, J. Zhang, W. Zhang, S. Guo, and C. You, "A facile method of improving the high rate cycling performance of lini1/3co1/3mn1/3o2 cathode material", *Journal of Alloys and Compounds*, vol. 686, pp. 267–272, 2016.

[41] Y. Deng, C. Yang, K. Zou, X. Qin, Z. Zhao, and G. Chen, "Recent advances of mn-rich life1-ymnypo4 ($0.5 \geq y < 1.0$) cathode materials for high energy density lithium ion batteries", *Advanced Energy Materials*, vol. 7, no. 13, p. 1 601 958, 2017.

[42] K. Brandt and J. Garche, "General overview of li-secondary battery safety issues", *Electrochemical Power Sources: Fundamentals, Systems, and Applications*, pp. 127–141, 2019.

[43] S. Kalluri, M. Yoon, M. Jo, S. Park, S. Myeong, J. Kim, S. X. Dou, Z. Guo, and J. Cho, "Surface engineering strategies of layered licoo2 cathode material to realize high-energy and high-voltage li-ion cells", *Advanced energy materials*, vol. 7, no. 1, p. 1 601 507, 2017.

[44] M. Akhilash, P. S. Salini, B. John, and T. D. Mercy, "A journey through layered cathode materials for lithium ion cells–from lithium cobalt oxide to lithium-rich transition metal oxides", *Journal of Alloys and Compounds*, vol. 869, p. 159 239, 2021.

[45] N. Corporation, *Nanomyte®be-20e*, [Specification Sheet], 2021.

[46] D. Schreiner, J. Lindenblatt, R. Daub, and G. Reinhart, "Simulation of the calendering process of nmc-622 cathodes for lithium-ion batteries", *Energy Technology*, p. 2 200 442, 2022.

[47] S. Liu, L. Xiong, and C. He, "Long cycle life lithium ion battery with lithium nickel cobalt manganese oxide (ncm) cathode", *Journal of Power Sources*, vol. 261, pp. 285–291, 2014.

[48] I. Buchmann, *Batteries in a Portable World - A Handbook on Rechargeable Batteries for Non-Engineers*. 2017, ISBN: 978-0-96-821184-7.

[49] M. Joulié, R. Laucournet, and E. Billy, "Hydrometallurgical process for the recovery of high value metals from spent lithium nickel cobalt aluminum oxide based lithium-ion batteries", *Journal of power sources*, vol. 247, pp. 551–555, 2014.

[50] N. Omar, P. Van Den Bossche, G. Mulder, M. Daowd, J. Timmermans, J. Van Mierlo, and S. Pauwels, "Assessment of performance of lithium iron phosphate oxide, nickel manganese cobalt oxide and nickel cobalt aluminum oxide based cells for using in plug-in battery electric vehicle applications", in *2011 IEEE Vehicle Power and Propulsion Conference*, IEEE, 2011, pp. 1–7.

[51] M.-J. Lee, S. Lee, P. Oh, Y. Kim, and J. Cho, "High performance $limn_2o_4$ cathode materials grown with epitaxial layered nanostructure for li-ion batteries", *Nano letters*, vol. 14, no. 2, pp. 993–999, 2014.

[52] J. Wang and X. Sun, "Olivine lifepo 4: The remaining challenges for future energy storage", *Energy & Environmental Science*, vol. 8, no. 4, pp. 1110–1138, 2015.

[53] J. Hu, W. Huang, L. Yang, and F. Pan, "Structure and performance of the lifepo 4 cathode material: From the bulk to the surface", *Nanoscale*, vol. 12, no. 28, pp. 15 036–15 044, 2020.

[54] H.-S. Kim, B.-W. Cho, and W.-I. Cho, "Cycling performance of $lifepo_4$ cathode material for lithium secondary batteries", *Journal of power sources*, vol. 132, no. 1-2, pp. 235–239, 2004.

[55] B. Wang, J. B. Bates, F. X. Hart, B. C. Sales, R. A. Zuhr, and J. D. Robertson, "Characterization of thin-film rechargeable lithium batteries with lithium cobalt oxide cathodes", *Journal of The Electrochemical Society*, vol. 143, no. 10, p. 3203, 1996.

[56] H. Chen, X. Qiu, W. Zhu, and P. Hagenmuller, "Synthesis and high rate properties of nanoparticled lithium cobalt oxides as the cathode material for lithium-ion battery", *Electrochemistry communications*, vol. 4, no. 6, pp. 488–491, 2002.

[57] L. Wang, B. Chen, J. Ma, G. Cui, and L. Chen, "Reviving lithium cobalt oxide-based lithium secondary batteries-toward a higher energy density", *Chemical Society Reviews*, vol. 47, no. 17, pp. 6505–6602, 2018.

[58] A. Manthiram and J. B. Goodenough, "Layered lithium cobalt oxide cathodes", *Nature Energy*, vol. 6, no. 3, pp. 323–323, 2021.

[59] J. P. Peres, C. Delmas, A. Rougier, M. Broussely, F. Perton, P. Biensan, and P. Willmann, "The relationship between the composition of lithium nickel oxide and the loss of reversibility during the first cycle", *Journal of Physics and Chemistry of Solids*, vol. 57, no. 6-8, pp. 1057–1060, 1996.

[60] D. P. Abraham, R. D. Twesten, M. Balasubramanian, J. Kropf, D. Fischer, J. McBreen, I. Petrov, and K. Amine, "Microscopy and spectroscopy of lithium nickel oxide-based particles used in high power lithium-ion cells", *Journal of The Electrochemical Society*, vol. 150, no. 11, A1450, 2003.

[61] J. Xu, E. Hu, D. Nordlund, A. Mehta, S. N. Ehrlich, X.-Q. Yang, and W. Tong, "Understanding the degradation mechanism of lithium nickel oxide cathodes for li-ion batteries", *ACS applied materials & interfaces*, vol. 8, no. 46, pp. 31 677–31 683, 2016.

[62] D. Wong, B. Shrestha, D. A. Wetz, and J. M. Heinzel, "Impact of high rate discharge on the aging of lithium nickel cobalt aluminum oxide batteries", *Journal of Power Sources*, vol. 280, pp. 363–372, 2015.

[63] P. Gao, Y. Jiang, Y. Zhu, and H. Hu, "Improved cycle performance of nitrogen and phosphorus co-doped carbon coatings on lithium nickel cobalt aluminum oxide battery material", *Journal of Materials Science*, vol. 53, no. 13, pp. 9662–9673, 2018.

[64] J. Wang, S. Yao, Y. Yu, T. Fu, P. Zhang, and J. Zhao, "Improving the stability properties of 5 v lithium nickel manganese oxide spinel by surface coating with cobalt aluminum oxides for lithium ion batteries", *Electrochimica Acta*, vol. 208, pp. 310–317, 2016.

[65] E. Hu, S. M. Bak, S. D. Senanayake, X.-Q. Yang, K.-W. Nam, L. Zhang, and M. Shao, "Thermal stability in the blended lithium manganese oxide–lithium nickel cobalt manganese oxide cathode materials: An in situ time-resolved x-ray diffraction and mass spectroscopy study", *Journal of Power Sources*, vol. 277, pp. 193–197, 2015.

[66] X. Sun, X. Luo, Z. Zhang, F. Meng, and J. Yang, "Life cycle assessment of lithium nickel cobalt manganese oxide (ncm) batteries for electric passenger vehicles", *Journal of Cleaner Production*, vol. 273, p. 123 006, 2020.

[67] S. Chen, X. Zhang, M. Xia, K. Wei, L. Zhang, X. Zhang, Y. Cui, and J. Shu, "Issues and challenges of layered lithium nickel cobalt manganese oxides for lithium-ion batteries", *Journal of Electroanalytical Chemistry*, vol. 895, p. 115 412, 2021.

[68] C. S. Johnson, J. S. Kim, C. Lefief, N. Li, J. T. Vaughey, and M. M. Thackeray, "The significance of the li2mno3 component in 'composite'xli2mno3·(1-x) limn0. 5ni0. 5o2 electrodes", *Electrochemistry Communications*, vol. 6, no. 10, pp. 1085–1091, 2004.

[69] J.-S. Kim, C. S. Johnson, J. T. Vaughey, M. M. Thackeray, S. A. Hackney, W. Yoon, and C. P. Grey, "Electrochemical and structural properties of x li2m'o_3 · (1- x) limn$_{0.5}$ni$_{0.5}o_2$ electrodes for lithium batteries (m'= ti, mn, zr; $0 \leq x \leq 0.3$)", *Chemistry of Materials*, vol. 16, no. 10, pp. 1996–2006, 2004.

[70] W. C. West, J. Soler, M. C. Smart, B. V. Ratnakumar, S. Firdosy, V. Ravi, M. S. Anderson, J. Hrbacek, E. S. Lee, and A. Manthiram, "Electrochemical behavior of layered solid solution li$_2$mno$_3$- limo$_2$ (m=ni, mn, co) li-ion cathodes with and without alumina coatings", *Journal of the Electrochemical Society*, vol. 158, no. 8, A883, 2011.

[71] H. Yu and H. Zhou, "High-energy cathode materials (li$_2$mno$_3$– limo$_2$) for lithium-ion batteries", *The journal of physical chemistry letters*, vol. 4, no. 8, pp. 1268–1280, 2013.

[72] R. Gummow, A. De Kock, and M. Thackeray, "Improved capacity retention in rechargeable 4 v lithium/lithium-manganese oxide (spinel) cells", *Solid State Ionics*, vol. 69, no. 1, pp. 59–67, 1994.

[73] K. Amine, J. Liu, S. Kang, I. Belharouak, Y. Hyung, D. Vissers, and G. Henriksen, "Improved lithium manganese oxide spinel/graphite li-ion cells for high-power applications", *Journal of power sources*, vol. 129, no. 1, pp. 14–19, 2004.

[74] L. Jaber-Ansari, K. P. Puntambekar, S. Kim, M. Aykol, L. Luo, J. Wu, B. D. Myers, H. Iddir, J. T. Russell, S. J. Saldaña, *et al.*, "Suppressing manganese dissolution from lithium manganese oxide spinel cathodes with single-layer graphene", *Advanced Energy Materials*, vol. 5, no. 17, p. 1 500 646, 2015.

[75] F. Cheng and J. Chen, "Transition metal vanadium oxides and vanadate materials for lithium batteries", *Journal of Materials Chemistry*, vol. 21, no. 27, pp. 9841–9848, 2011.

[76] H. Zhao, L. Pan, S. Xing, J. Luo, and J. Xu, "Vanadium oxides–reduced graphene oxide composite for lithium-ion batteries and supercapacitors with improved electrochemical performance", *Journal of Power Sources*, vol. 222, pp. 21–31, 2013.

[77] D. McNulty, D. Buckley, and C. O'Dwyer, "Synthesis and electrochemical properties of vanadium oxide materials and structures as li-ion battery positive electrodes", *Journal of Power Sources*, vol. 267, pp. 831–873, 2014.

[78] H. Liu, Z. Zhu, Q. Yan, S. Yu, X. He, Y. Chen, R. Zhang, L. Ma, T. Liu, M. Li, *et al.*, "A disordered rock salt anode for fast-charging lithium-ion batteries", *Nature*, vol. 585, no. 7823, pp. 63–67, 2020.

[79] G. X. Wang, S. Needham, J. Yao, J. Z. Wang, R. S. Liu, and H. K. Liu, "A study on lifepo$_4$ and its doped derivatives as cathode materials for lithium-ion batteries", *Journal of power sources*, vol. 159, no. 1, pp. 282–286, 2006.

[80] J. Hassoun, F. Bonaccorso, M. Agostini, M. Angelucci, M. G. Betti, R. Cingolani, M. Gemmi, C. Mariani, S. Panero, V. Pellegrini, *et al.*, "An advanced lithium-ion battery based on a graphene anode and a lithium iron phosphate cathode", *Nano letters*, vol. 14, no. 8, pp. 4901–4906, 2014.

[81] J.-K. Kim, J.-W. Choi, G. Chauhan, J.-H. Ahn, G.-C. Hwang, J.-B. Choi, and H.-J. Ahn, "Enhancement of electrochemical performance of lithium iron phosphate by controlled sol–gel synthesis", *Electrochimica Acta*, vol. 53, no. 28, pp. 8258–8264, 2008.

[82] N. Khasanova, O. Drozhzhin, D. Storozhilova, C. Delmas, and E. Antipov, "New form of li2fepo4f as cathode material for li-ion batteries", *Chemistry of Materials*, vol. 24, no. 22, pp. 4271–4273, 2012.

[83] Z.-W. Bai, M. Shao, and G. Chen, "New insight of nalifepo4f as a high voltage cathode material for lithium-ion battery", in *ECS Meeting Abstracts*, IOP Publishing, 2019, p. 1516.

[84] W. Sukkabot, "Structural and electronic properties of non-metal doping in li2fepo4f compound: Spin density functional theory", *Philosophical Magazine*, vol. 100, no. 24, pp. 3155–3164, 2020.

[85] H. Wang, H. Zhang, Y. Cheng, K. Feng, X. Li, and H. Zhang, "All-nasicon lvp-ltp aqueous lithium ion battery with excellent stability and low-temperature performance", *Electrochimica Acta*, vol. 278, pp. 279–289, 2018.

[86] M. Moustafa, M. Sanad, and M. Hassaan, "Nasicon-type lithium iron germanium phosphate glass ceramic nanocomposites as anode materials for lithium ion batteries", *Journal of Alloys and Compounds*, vol. 845, p. 156 338, 2020.

[87] M. Hou, F. Liang, K. Chen, Y. Dai, and D. Xue, "Challenges and perspectives of nasicon-type solid electrolytes for all-solid-state lithium batteries", *Nanotechnology*, vol. 31, no. 13, p. 132 003, 2020.

[88] Z.-E. Yu, Y. Lyu, Z. Zou, N. Su, B. He, S. Wang, S. Shi, and B. Guo, "Understanding the structural evolution and storage mechanism of nasicon-structure mg0. 5ti2 (po4) 3 for li-ion and na-ion batteries", *ACS Sustainable Chemistry & Engineering*, vol. 9, no. 40, pp. 13 414–13 423, 2021.

[89] G. L. Holleck and J. R. Driscoll, "Transition metal sulfides as cathodes for secondary lithium batteries—ii. titanium sulfides", *Electrochimica Acta*, vol. 22, no. 6, pp. 647–655, 1977.

[90] X. Xu, W. Liu, Y. Kim, and J. Cho, "Nanostructured transition metal sulfides for lithium ion batteries: Progress and challenges", *Nano Today*, vol. 9, no. 5, pp. 604–630, 2014.

[91] J. Zhao, Y. Zhang, Y. Wang, H. Li, and Y. Peng, "The application of nanostructured transition metal sulfides as anodes for lithium ion batteries", *Journal of energy chemistry*, vol. 27, no. 6, pp. 1536–1554, 2018.

[92] Y. P. Wu, C. Jiang, C. Wan, and R. Holze, "Modified natural graphite as anode material for lithium ion batteries", *Journal of power sources*, vol. 111, no. 2, pp. 329–334, 2002.

[93] V. Srinivasan and J. Newman, "Design and optimization of a natural graphite/iron phosphate lithium-ion cell", *Journal of the Electrochemical Society*, vol. 151, no. 10, A1530, 2004.

[94] L. Zhao, B. Ding, X.-Y. Qin, Z. Wang, W. Lv, Y.-B. He, Q.-H. Yang, and F. Kang, "Revisiting the roles of natural graphite in ongoing lithium-ion batteries", *Advanced Materials*, vol. 34, no. 18, p. 2 106 704, 2022.

[95] J. Li, K. Xie, Y. Lai, F. Li, X. Hao, X. Chen, Y. Liu, *et al.*, "Lithium oxalyldifluoroborate/carbonate electrolytes for lifepo4/artificial graphite lithium-ion cells", *Journal of Power Sources*, vol. 195, no. 16, pp. 5344–5350, 2010.

[96] C. Ma, Y. Zhao, J. Li, Y. Song, J. Shi, Q. Guo, and L. Liu, "Synthesis and electrochemical properties of artificial graphite as an anode for high-performance lithium-ion batteries", *Carbon*, vol. 64, pp. 553–556, 2013.

[97] F. Zou, H. C. Nallan, A. Dolocan, Q. Xie, J. Li, B. M. Coffey, J. G. Ekerdt, and A. Manthiram, "Long-life lini0. 5mn1. 5o4/graphite lithium-ion cells with an artificial graphite-electrolyte interface", *Energy Storage Materials*, vol. 43, pp. 499–508, 2021.

[98] M. Schroeder, M. Winter, S. Passerini, and A. Balducci, "On the cycling stability of lithium-ion capacitors containing soft carbon as anodic material", *Journal of Power Sources*, vol. 238, pp. 388–394, 2013.

[99] B. Sun, Q. Zhang, H. Xiang, F. Han, W. Tang, G. Yuan, Y. Cong, C. Fan, A. Westwood, and X. Li, "Enhanced active sulfur in soft carbon via synergistic doping effect for ultra–stable lithium–ion batteries", *Energy Storage Materials*, vol. 24, pp. 450–457, 2020.

[100] H. Sun, X. He, J. Ren, J. Li, C. Jiang, and C. Wan, "Hard carbon/lithium composite anode materials for li-ion batteries", *Electrochimica acta*, vol. 52, no. 13, pp. 4312–4316, 2007.

[101] H. Fujimoto, K. Tokumitsu, A. Mabuchi, N. Chinnasamy, and T. Kasuh, "The anode performance of the hard carbon for the lithium ion battery derived from the oxygen-containing aromatic precursors", *Journal of Power Sources*, vol. 195, no. 21, pp. 7452–7456, 2010.

[102] J. Wang, J.-L. Liu, Y.-G. Wang, C.-X. Wang, and Y.-Y. Xia, "Pitch modified hard carbons as negative materials for lithium-ion batteries", *Electrochimica acta*, vol. 74, pp. 1–7, 2012.

[103] L.-F. Zhao, Z. Hu, W.-H. Lai, Y. Tao, J. Peng, Z.-C. Miao, Y.-X. Wang, S.-L. Chou, H.-K. Liu, and S.-X. Dou, "Hard carbon anodes: Fundamental understanding and commercial perspectives for na-ion batteries beyond li-ion and k-ion counterparts", *Advanced Energy Materials*, vol. 11, no. 1, p. 2 002 704, 2021.

[104] B. T. Hang, T. Doi, S. Okada, and J.-I. Yamaki, "Effect of carbonaceous materials on electrochemical properties of nano-sized fe2o3-loaded carbon as a lithium battery negative electrode", *Journal of Power Sources*, vol. 174, no. 2, pp. 493–500, 2007.

[105] A. Y. Shenouda and K. R. Murali, "Electrochemical properties of doped lithium titanate compounds and their performance in lithium rechargeable batteries", *Journal of Power Sources*, vol. 176, no. 1, pp. 332–339, 2008.

[106] C. P. Sandhya, B. John, and C. Gouri, "Lithium titanate as anode material for lithium-ion cells: A review", *Ionics*, vol. 20, no. 5, pp. 601–620, 2014.

[107] S. Wang, W. Quan, Z. Zhu, Y. Yang, Q. Liu, Y. Ren, X. Zhang, R. Xu, Y. Hong, Z. Zhang, *et al.*, "Lithium titanate hydrates with superfast and stable cycling in lithium ion batteries", *Nature communications*, vol. 8, no. 1, pp. 1–8, 2017.

[108] H. Yan, D. Zhang, X. Duo, X. Sheng, *et al.*, "A review of spinel lithium titanate (li4ti5o12) as electrode material for advanced energy storage devices", *Ceramics International*, vol. 47, no. 5, pp. 5870–5895, 2021.

[109] Y. Liu, L. Wang, K. Jiang, and S. Yang, "Electro-deposition preparation of self-standing cu-sn alloy anode electrode for lithium ion battery", *Journal of Alloys and Compounds*, vol. 775, pp. 818–825, 2019.

[110] B. T. Heligman, K. J. Kreder III, and A. Manthiram, "Zn-sn interdigitated eutectic alloy anodes with high volumetric capacity for lithium-ion batteries", *Joule*, vol. 3, no. 4, pp. 1051–1063, 2019.

[111] S. Liang, Y.-J. Cheng, J. Zhu, Y. Xia, and P. Müller-Buschbaum, "A chronicle review of nonsilicon (sn, sb, ge)-based lithium/sodium-ion battery alloying anodes", *Small Methods*, vol. 4, no. 8, p. 2 000 218, 2020.

[112] E. Lökçü and M. Anik, "Synthesis and electrochemical performance of lithium silicide based alloy anodes for li–ion oxygen batteries", *International Journal of Hydrogen Energy*, vol. 46, no. 18, pp. 10 624–10 631, 2021.

[113] Z. Lu, Q. Liang, B. Wang, Y. Tao, Y. Zhao, W. Lv, D. Liu, C. Zhang, Z. Weng, J. Liang, *et al.*, "Graphitic carbon nitride induced micro-electric field for dendrite-free lithium metal anodes", *Advanced Energy Materials*, vol. 9, no. 7, p. 1 803 186, 2019.

[114] M. Lei, J.-G. Wang, L. Ren, D. Nan, C. Shen, K. Xie, and X. Liu, "Highly lithiophilic cobalt nitride nanobrush as a stable host for high-performance lithium metal anodes", *ACS applied materials & interfaces*, vol. 11, no. 34, pp. 30 992–30 998, 2019.

[115] J. Zhu, J. Chen, Y. Luo, S. Sun, L. Qin, H. Xu, P. Zhang, W. Zhang, W. Tian, and Z. Sun, "Lithiophilic metallic nitrides modified nickel foam by plasma for stable lithium metal anode", *Energy Storage Materials*, vol. 23, pp. 539–546, 2019.

[116] D. Xia, M. Gao H.and Li, F. Gong, and M. Li, "Transition metal vanadates electrodes in lithium-ion batteries: A holistic review", *Energy Storage Materials*, vol. 35, pp. 169–191, 2021.

[117] F. Gong, D. D. Xia, Q. Zhou, J. Liao, and M. Wu, "Novel spherical cobalt/nickel mixed-vanadates as high-capacity anodes in lithium ion batteries", *Journal of Alloys and Compounds*, vol. 766, pp. 442–449, 2018.

[118] S.-H. Ng, J. Wang, D. Wexler, K. Konstantinov, Z.-P. Guo, and H.-K. Liu, "Highly reversible lithium storage in spheroidal carbon-coated silicon nanocomposites as anodes for lithium-ion batteries", *Angewandte Chemie International Edition*, vol. 45, no. 41, pp. 6896–6899, 2006.

[119] T. Stephenson, Z. Li, B. Olsen, and D. Mitlin, "Lithium ion battery applications of molybdenum disulfide (mos 2) nanocomposites", *Energy & Environmental Science*, vol. 7, no. 1, pp. 209–231, 2014.

[120] A. Eftekhari, "Lifepo4/c nanocomposites for lithium-ion batteries", *Journal of Power Sources*, vol. 343, pp. 395–411, 2017.

[121] T.-F. Yi, H. M. K. Sari, X. Li, F. Wang, Y.-R. Zhu, J. Hu, J. Zhang, and X. Li, "A review of niobium oxides based nanocomposites for lithium-ion batteries, sodium-ion batteries and supercapacitors", *Nano Energy*, vol. 85, p. 105 955, 2021.

[122] P. Ping, Q. Wang, J. Sun, X. Feng, and C. Chen, "Effect of sulfites on the performance of libob/γ-butyrolactone electrolytes", *Journal of Power Sources*, vol. 196, no. 2, pp. 776–783, 2011.

[123] T. J. Carter, R. Mohtadi, T. S. Arthur, F. Mizuno, R. Zhang, S. Shirai, and J. W. Kampf, "Boron clusters as highly stable magnesium-battery electrolytes", *Angewandte Chemie*, vol. 126, no. 12, pp. 3237–3241, 2014.

[124] V. R. Koch and J. H. Young, "2-methyltetrahydrofuran—lithium hexafluoroarsenate: A superior electrolyte for the secondary lithium electrode", *Science*, vol. 204, no. 4392, pp. 499–501, 1979.

[125] X. Liu, X. Shen, H. Li, P. Li, L. Luo, H. Fan, X. Feng, W. Chen, X. Ai, H. Yang, *et al.*, "Ethylene carbonate-free propylene carbonate-based electrolytes with excellent electrochemical compatibility for li-ion batteries through engineering electrolyte solvation structure", *Advanced Energy Materials*, vol. 11, no. 19, p. 2 003 905, 2021.

[126] A. Suzumura, H. Ohno, N. Kikkawa, and K. Takechi, "Finding a novel electrolyte solution of lithium-ion batteries using an autonomous search system based on ensemble optimization", *Journal of Power Sources*, vol. 541, p. 231 698, 2022.

[127] D. Aurbach, B. Markovsky, A. Shechter, Y. Ein-Eli, and H. Cohen, "A comparative study of synthetic graphite and li electrodes in electrolyte solutions based on ethylene carbonate-dimethyl carbonate mixtures", *Journal of the Electrochemical Society*, vol. 143, no. 12, p. 3809, 1996.

[128] Y. Wu, D. Ren, X. Liu, G.-L. Xu, X. Feng, Y. Zheng, Y. Li, M. Yang, Y. Peng, X. Han, *et al.*, "High-voltage and high-safety practical lithium batteries with ethylene carbonate-free electrolyte", *Advanced Energy Materials*, vol. 11, no. 47, p. 2 102 299, 2021.

[129] J.-W. Liu, X.-H. Li, Z.-X. Wang, H.-J. Guo, W.-J. Peng, Y.-H. Zhang, and Q.-Y. Hu, "Preparation and characterization of lithium hexafluorophosphate for lithium-ion battery electrolyte", *Transactions of Nonferrous Metals Society of China*, vol. 20, no. 2, pp. 344–348, 2010.

[130] G. Nikiforidis, M. Raghibi, A. Sayegh, and M. Anouti, "Low-concentrated lithium hexafluorophosphate ternary-based electrolyte for a reliable and safe nmc/graphite lithium-ion battery", *The Journal of Physical Chemistry Letters*, vol. 12, no. 7, pp. 1911–1917, 2021.

[131] E. Paillard, F. Alloin, L. Cointeaux, C. Iojoiu, and J.-Y. Sanchez, "Poly (oxyethylene) electrolytes based on lithium nitrophenyl sulfonamide and hexanitrodiphenylamide", *Electrochimica acta*, vol. 57, pp. 20–26, 2011.

[132] H. Xiang, P. Shi, P. Bhattacharya, X. Chen, D. Mei, M. E. Bowden, J. Zheng, J.-G. Zhang, and W. Xu, "Enhanced charging capability of lithium metal batteries based on lithium bis (trifluoromethanesulfonyl) imide-lithium bis (oxalato) borate dual-salt electrolytes", *Journal of Power Sources*, vol. 318, pp. 170–177, 2016.

[133] T. Schedlbauer, S. Krüger, R. Schmitz, R. Schmitz, C. Schreiner, H. Gores, S. Passerini, and M. Winter, "Lithium difluoro (oxalato) borate: A promising salt for lithium metal based secondary batteries?", *Electrochimica Acta*, vol. 92, pp. 102–107, 2013.

[134] X. Zuo, C. Fan, J. Liu, X. Xiao, J. Wu, and J. Nan, "Lithium tetrafluoroborate as an electrolyte additive to improve the high voltage performance of lithium-ion battery", *Journal of The Electrochemical Society*, vol. 160, no. 8, A1199, 2013.

[135] Y. Katayama, I. Konishiike, T. Miura, and T. Kishi, "Redox reaction in 1-ethyl-3-methylimidazolium–iron chlorides molten salt system for battery application", *Journal of power sources*, vol. 109, no. 2, pp. 327–332, 2002.

[136] W. Wang, T. Yang, S. Li, W. Fan, X. Zhao, C. Fan, L. Yu, S. Zhou, X. Zuo, R. Zeng, *et al.*, "1-ethyl-3-methylimidazolium tetrafluoroborate (emi-bf4) as an ionic liquid-type electrolyte additive to enhance the low-temperature performance of lini0. 5co0. 2mn0. 3o2/graphite batteries", *Electrochimica Acta*, vol. 317, pp. 146–154, 2019.

[137] R. Yunis, D. Al-Masri, A. F. Hollenkamp, C. M. Doherty, H. Zhu, and J. M. Pringle, "Plastic crystals utilising small ammonium cations and sulfonylimide anions as electrolytes for lithium batteries", *Journal of The Electrochemical Society*, vol. 167, no. 7, p. 070 529, 2020.

[138] D. Voropaeva, D. Golubenko, A. Merkel, and A. Yaroslavtsev, "Membranes with novel highly-delocalized sulfonylimide anions for lithium-ion batteries", *Journal of Membrane Science*, vol. 601, p. 117 918, 2020.

[139] S. S. Zhang, "A review on electrolyte additives for lithium-ion batteries", *Journal of Power Sources*, vol. 162, no. 2, pp. 1379–1394, 2006.

[140] M. Mishra, C.-W. Hsu, P. C. Rath, J. Patra, H.-Z. Lai, T.-L. Chang, C.-Y. Wang, T.-Y. Wu, T.-C. Lee, and J.-K. Chang, "Ga-doped lithium lanthanum zirconium oxide electrolyte for solid-state li batteries", *Electrochimica Acta*, vol. 353, p. 136 536, 2020.

[141] V. Lacivita, A. S. Westover, A. Kercher, N. D. Phillip, G. Yang, G. Veith, G. Ceder, and N. J. Dudney, "Resolving the amorphous structure of lithium phosphorus oxynitride (lipon)", *Journal of the American Chemical Society*, vol. 140, no. 35, pp. 11 029–11 038, 2018.

[142] A. Hayashi and M. Tatsumisago, "Sulfide-glass electrolytes for all-solid-state batteries", *Encyclopedia of Glass Science, Technology, History, and Culture*, vol. 2, pp. 1125–1134, 2021.

[143] S. N. Johari, N. A. Tajuddin, H. Hanibah, and S. K. Deraman, "A review: Ionic conductivity of solid polymer electrolyte based polyethylene oxide", *Int. J. Electrochem. Sci*, vol. 16, no. 2, 2021.

[144] W.-Q. Ding, F. Lv, N. Xu, M.-T. Wu, J. Liu, and X.-P. Gao, "Polyethylene oxide-based solid-state composite polymer electrolytes for rechargeable lithium batteries", *ACS Applied Energy Materials*, vol. 4, no. 5, pp. 4581–4601, 2021.

[145] J. W. Choi and D. Aurbach, "Promise and reality of post-lithium-ion batteries with high energy densities", *Nature Reviews Materials*, vol. 1, no. 4, pp. 1–16, 2016.

[146] T. L. Kulova, V. N. Fateev, E. A. Seregina, and A. S. Grigoriev, "A brief review of post-lithium-ion batteries", *Int. J. Electrochem. Sci*, vol. 15, no. 8, pp. 7242–7259, 2020.

[147] E. Quartarone and P. Mustarelli, "Emerging trends in the design of electrolytes for lithium and post-lithium batteries", *Journal of the Electrochemical Society*, vol. 167, no. 5, p. 050 508, 2020.

[148] M. Walter, M. V. Kovalenko, and K. V. Kravchyk, "Challenges and benefits of post-lithium-ion batteries", *New Journal of Chemistry*, vol. 44, no. 5, pp. 1677–1683, 2020.

[149] Y. Cui, "Silicon anodes", *Nature Energy*, vol. 6, no. 10, pp. 995–996, 2021.

[150] J. Kim, J. Ma, H. Yoon, J. Jang, S. Suh, H. Park, J. Song, J. H. Kim, J. Park, J.-J. Woo, *et al.*, "Viable post-electrode-engineering for the complete integrity of large-volume-change lithium-ion battery anodes", *Journal of Materials Chemistry A*, vol. 10, no. 16, pp. 9091–9102, 2022.

[151] A. Manthiram, J. C. Knight, S.-T. Myung, S.-M. Oh, and Y.-K. Sun, "Nickel-rich and lithium-rich layered oxide cathodes: Progress and perspectives", *Advanced Energy Materials*, vol. 6, no. 1, p. 1 501 010, 2016.

[152] B. Jeevanantham and M. K. Shobana, "Enhanced cathode materials for advanced lithium-ion batteries using nickel-rich and lithium/manganese-rich linixmnycozo2", *Journal of Energy Storage*, vol. 54, p. 105 353, 2022.

[153] H. J. Song, S. H. Oh, Y. Lee, J. Kim, and T. Yim, "Dually modified cathode-electrolyte interphases layers by calcium phosphate on the surface of nickel-rich layered oxide cathode for lithium-ion batteries", *Journal of Power Sources*, vol. 483, p. 229 218, 2021.

[154] D. Lin, Y. Liu, and Y. Cui, "Reviving the lithium metal anode for high-energy batteries", *Nature nanotechnology*, vol. 12, no. 3, pp. 194–206, 2017.

[155] H. Yuan, X. Ding, T. Liu, J. Nai, Y. Wang, Y. Liu, C. Liu, and X. Tao, "A review of concepts and contributions in lithium metal anode development", *Materials Today*, 2022.

[156] Z. Wang, Y. Cao, J. Zhou, J. Liu, X. Shen, H. Ji, C. Yan, and T. Qian, "Processing robust lithium metal anode for high-security batteries: A minireview", *Energy Storage Materials*, 2022.

[157] A. N. Singh, M. Islam, A. Meena, M. Faizan, D. Han, C. Bathula, A. Hajibabaei, R. Anand, and K.-W. Nam, "Unleashing the potential of sodium-ion batteries: Current state and future directions for sustainable energy storage", *Advanced Functional Materials*, vol. 33, no. 46, p. 2 304 617, 2023.

[158] H. Moon, A. Innocenti, H. Liu, H. Zhang, M. Weil, M. Zarrabeitia, and S. Passerini, "Bio-waste-derived hard carbon anodes through a sustainable and cost-effective synthesis process for sodium-ion batteries", *ChemSusChem*, vol. 16, no. 1, e202201713, 2023.

[159] L. Wang, J. Wang, X. Zhang, Y. Ren, P. Zuo, G. Yin, and J. Wang, "Unravelling the origin of irreversible capacity loss in nanio2 for high voltage sodium ion batteries", *Nano Energy*, vol. 34, pp. 215–223, 2017.

[160] M. Sawicki and L. L. Shaw, "Advances and challenges of sodium ion batteries as post lithium ion batteries", *RSC Advances*, vol. 5, no. 65, pp. 53 129–53 154, 2015.

[161] W. Zuo, A. Innocenti, M. Zarrabeitia, D. Bresser, Y. Yang, and S. Passerini, "Layered oxide cathodes for sodium-ion batteries: Storage mechanism, electrochemistry, and techno-economics", *Accounts of Chemical Research*, vol. 56, no. 3, pp. 284–296, 2023.

[162] M. Zhao, B.-Q. Li, H.-J. Peng, H. Yuan, J.-Y. Wei, and J.-Q. Huang, "Lithium–sulfur batteries under lean electrolyte conditions: Challenges and opportunities", *Angewandte Chemie International Edition*, vol. 59, no. 31, pp. 12 636–12 652, 2020.

[163] S. Dörfler, S. Walus, J. Locke, A. Fotouhi, D. J. Auger, N. Shateri, T. Abendroth, P. Härtel, H. Althues, and S. Kaskel, "Recent progress and emerging application areas for lithium–sulfur battery technology", *Energy Technology*, vol. 9, no. 1, p. 2 000 694, 2021.

[164] A. Varzi, K. Thanner, R. Scipioni, D. Di Lecce, J. Hassoun, S. Dörfler, H. Altheus, S. Kaskel, C. Prehal, and S. A. Freunberger, "Current status and future perspectives of lithium metal batteries", *Journal of Power Sources*, vol. 480, p. 228 803, 2020.

[165] Y. Zhao, Y. Ye, F. Wu, Y. Li, L. Li, and R. Chen, "Anode interface engineering and architecture design for high-performance lithium–sulfur batteries", *Advanced Materials*, vol. 31, no. 12, p. 1 806 532, 2019.

[166] M. Wild, "Anode–electrolyte interface", *Lithium–Sulfur Batteries*, pp. 121–127, 2019.

[167] H. Zhao, N. Deng, J. Yan, W. Kang, J. Ju, Y. Ruan, X. Wang, X. Zhuang, Q. Li, and B. Cheng, "A review on anode for lithium-sulfur batteries: Progress and prospects", *Chemical Engineering Journal*, vol. 347, pp. 343–365, 2018.

[168] D. Wang, L.-J. Jhang, R. Kou, M. Liao, S. Zheng, H. Jiang, P. Shi, G.-X. Li, K. Meng, and D. Wang, "Realizing high-capacity all-solid-state lithium-sulfur batteries using a low-density inorganic solid-state electrolyte", *Nature communications*, vol. 14, no. 1, p. 1895, 2023.

[169] E. Umeshbabu, B. Zheng, and Y. Yang, "Recent progress in all-solid-state lithium- sulfur batteries using high li-ion conductive solid electrolytes", *Electrochemical Energy Reviews*, vol. 2, pp. 199–230, 2019.

[170] J. O. Park, M. Kim, J.-H. Kim, K. H. Choi, H. C. Lee, W. Choi, S. B. Ma, and D. Im, "A 1000 wh kg- 1 li–air battery: Cell design and performance", *Journal of Power Sources*, vol. 419, pp. 112–118, 2019.

[171] K. Chen, D.-Y. Yang, G. Huang, and X.-B. Zhang, "Lithium–air batteries: Air-electrochemistry and anode stabilization", *Accounts of Chemical Research*, vol. 54, no. 3, pp. 632–641, 2021.

[172] X. Liu, H. Jiao, M. Wang, W. Song, J. Xue, and S. Jiao, "Current progresses and future prospects on aluminium–air batteries", *International Materials Reviews*, vol. 67, no. 7, pp. 734–764, 2022.

[173] S. Huang, Z. Wang, Y. Von Lim, Y. Wang, Y. Li, D. Zhang, and H. Y. Yang, "Recent advances in heterostructure engineering for lithium–sulfur batteries", *Advanced Energy Materials*, vol. 11, no. 10, p. 2 003 689, 2021.

[174] J. He and A. Manthiram, "A review on the status and challenges of electrocatalysts in lithium-sulfur batteries", *Energy Storage Materials*, vol. 20, pp. 55–70, 2019.

[175] K. Takada, "Progress and prospective of solid-state lithium batteries", *Acta Materialia*, vol. 61, no. 3, pp. 759–770, 2013.

[176] L. Ye and X. Li, "A dynamic stability design strategy for lithium metal solid state batteries", *Nature*, vol. 593, no. 7858, pp. 218–222, 2021.

[177] C. Li, Z. Wang, Z. He, Y. Li, J. Mao, K. Dai, C. Yan, and J. Zheng, "An advance review of solid-state battery: Challenges, progress and prospects", *Sustainable Materials and Technologies*, vol. 29, e00297, 2021.

[178] M. Rahman, X. Wang, C. Wen, *et al.*, "A review of high energy density lithium–air battery technology", *Journal of Applied Electrochemistry*, vol. 44, no. 1, pp. 5–22, 2014.

[179] C. Shen, J. Xie, T. Liu, M. Zhang, P. Andrei, L. Dong, M. Hendrickson, E. J. Plichta, and J. P. Zheng, "Influence of pore size on discharge capacity in li-air batteries with hierarchically macroporous carbon nanotube foams as cathodes", *Journal of The Electrochemical Society*, vol. 165, no. 11, A2833, 2018.

[180] N. Imanishi and O. Yamamoto, "Perspectives and challenges of rechargeable lithium–air batteries", *Materials Today Advances*, vol. 4, p. 100 031, 2019.

[181] X. Yin, S. Sarkar, S. Shi, Q.-A. Huang, H. Zhao, L. Yan, Y. Zhao, and J. Zhang, "Recent progress in advanced organic electrode materials for sodium-ion batteries: Synthesis, mechanisms, challenges and perspectives", *Advanced Functional Materials*, vol. 30, no. 11, p. 1 908 445, 2020.

[182] A. Eftekhari and D.-W. Kim, "Sodium-ion batteries: New opportunities beyond energy storage by lithium", *Journal of Power Sources*, vol. 395, pp. 336–348, 2018.

[183] A. Jana, R. Paul, and A. K. Roy, "Architectural design and promises of carbon materials for energy conversion and storage: In laboratory and industry", in *Carbon Based Nanomaterials for Advanced Thermal and Electrochemical Energy Storage and Conversion*, Elsevier, 2019, pp. 25–61.

[184] S. Kim, S. Qu, R. Zhang, and P. V. Braun, "High volumetric and gravimetric capacity electrodeposited mesostructured sb2o3 sodium ion battery anodes", *Small*, vol. 15, no. 23, p. 1 900 258, 2019.

[185] J. Neubauer, K. Smith, E. Wood, and A. Pesaran, "Identifying and overcoming critical barriers to widespread second use of pev batteries", National Renewable Energy Lab.(NREL), Golden, CO (United States), Tech. Rep., 2015.

[186] S. F. Schuster, T. Bach, E. Fleder, J. Müller, M. Brand, G. Sextl, and A. Jossen, "Nonlinear aging characteristics of lithium-ion cells under different operational conditions", *Journal of Energy Storage*, vol. 1, pp. 44–53, 2015.

[187] A. Barai, K. Uddin, M. Dubarry, L. Somerville, A. McGordon, P. Jennings, and I. Bloom, "A comparison of methodologies for the non-invasive characterisation of commercial li-ion cells", *Progress in Energy and Combustion Science*, vol. 72, pp. 1–31, 2019.

[188] A. Kampker, H. H. Heimes, C. Offermanns, J. Vienenkötter, M. Frank, and D. Holz, "Identification of challenges for second-life battery systems—a literature review", *World Electric Vehicle Journal*, vol. 14, no. 4, p. 80, 2023.

[189] J. Zhu, I. Mathews, D. Ren, W. Li, D. Cogswell, B. Xing, T. Sedlatschek, S. N. R. Kantareddy, M. Yi, T. Gao, *et al.*, "End-of-life or second-life options for retired electric vehicle batteries", *Cell Reports Physical Science*, vol. 2, no. 8, 2021.

[190] C. R. Birkl, M. R. Roberts, E. McTurk, P. G. Bruce, and D. A. Howey, "Degradation diagnostics for lithium ion cells", *Journal of Power Sources*, vol. 341, pp. 373–386, 2017.

[191] J. S. Edge, S. O'Kane, R. Prosser, N. D. Kirkaldy, A. N. Patel, A. Hales, A. Ghosh, W. Ai, J. Chen, J. Yang, *et al.*, "Lithium ion battery degradation: What you need to know", *Physical Chemistry Chemical Physics*, vol. 23, no. 14, pp. 8200–8221, 2021.

[192] E. Warburg, "Ueber das verhalten sogenannter unpolarisirbarer elektroden gegen wechselstrom", *Annalen der Physik*, vol. 303, no. 3, pp. 493–499, 1899.

[193] E. Neumann, "Ueber die polarisationscapacität umkehrbarer elektroden", *Annalen der Physik*, vol. 303, no. 3, pp. 500–534, 1899.

[194] T. Wik, B. Fridholm, and H. Kuusisto, "Implementation and robustness of an analytically based battery state of power", *Journal of Power Sources*, vol. 287, pp. 448–457, 2015.

[195] R. Xiong, J. Cao, Q. Yu, H. He, and F. Sun, "Critical review on the battery state of charge estimation methods for electric vehicles", *IEEE Access*, vol. 6, pp. 1832–1843, 2018. DOI: 10.1109/ACCESS.2017.2780258.

[196] M. A. Hannan, M. H. Lipu, A. Hussain, and A. Mohamed, "A review of lithium-ion battery state of charge estimation and management system in electric vehicle applications: Challenges and recommendations", *Renewable and Sustainable Energy Reviews*, vol. 78, pp. 834–854, 2017.

[197] A. Barai, K. Uddin, W. Widanalage, A. McGordon, and P. Jennings, "The effect of average cycling current on total energy of lithium-ion batteries for electric vehicles", *Journal of Power Sources*, vol. 303, pp. 81–85, 2016.

[198] E. Cabrera-Castillo, F. Niedermeier, and A. Jossen, "Calculation of the state of safety (sos) for lithium ion batteries", *Journal of Power Sources*, vol. 324, pp. 509–520, 2016.

[199] S. Park, J. Ahn, T. Kang, S. Park, Y. Kim, I. Cho, and J. Kim, "Review of state-of-the-art battery state estimation technologies for battery management systems of stationary energy storage systems", *Journal of Power Electronics*, vol. 20, no. 6, pp. 1526–1540, 2020.

[200] Y. Gan, J. Wang, J. Liang, Z. Huang, and M. Hu, "Development of thermal equivalent circuit model of heat pipe-based thermal management system for a battery module with cylindrical cells", *Applied Thermal Engineering*, vol. 164, p. 114 523, 2020.

[201] H. Wang, S. Wang, X. Feng, X. Zhang, K. Dai, J. Sheng, Z. Zhao, Z. Du, Z. Zhang, K. Shen, *et al.*, "An experimental study on the thermal characteristics of the cell-to-pack system", *Energy*, vol. 227, p. 120 338, 2021.

[202] K. Liu, X. Tang, R. Teodorescu, F. Gao, and J. Meng, "Future ageing trajectory prediction for lithium-ion battery considering the knee point effect", *IEEE Transactions on Energy Conversion*, vol. 37, no. 2, pp. 1282–1291, 2022. DOI: 10.1109/TEC.2021.3130600.

[203] I. Buchberger, S. Seidlmayer, A. Pokharel, M. Piana, J. Hattendorff, P. Kudejova, R. Gilles, and H. A. Gasteiger, "Aging analysis of graphite/lini1/3mn1/3co1/3o2 cells using xrd, pgaa, and ac impedance", *Journal of The Electrochemical Society*, vol. 162, no. 14, A2737, 2015.

[204] P. Keil and A. Jossen, "Charging protocols for lithium-ion batteries and their impact on cycle life—an experimental study with different 18650 high-power cells", *Journal of Energy Storage*, vol. 6, pp. 125–141, 2016.

[205] G. Coppez, S. Chowdhury, and S. Chowdhury, "The importance of energy storage in renewable power generation: A review", in *45th International Universities Power Engineering Conference UPEC2010*, IEEE, 2010, pp. 1–5.

[206] G. Coppez, S. Chowdhury, and S. Chowdhury, "Review of battery storage optimisation in distributed generation", in *2010 Joint International Conference on Power Electronics, Drives and Energy Systems & 2010 Power India*, IEEE, 2010, pp. 1–6.

[207] H. Rahimi-Eichi, U. Ojha, F. Baronti, and M.-Y. Chow, "Battery management system: An overview of its application in the smart grid and electric vehicles", *IEEE industrial electronics magazine*, vol. 7, no. 2, pp. 4–16, 2013.

[208] M. Lelie, T. Braun, M. Knips, H. Nordmann, F. Ringbeck, H. Zappen, and D. U. Sauer, "Battery management system hardware concepts: An overview", *Applied Sciences*, vol. 8, no. 4, p. 534, 2018.

[209] R. Xiong and R. Xiong, "Battery SOC and SOH estimation", *Battery Management Algorithm for Electric Vehicles*, pp. 107–165, 2020.

[210] C. Bonfiglio and W. Roessler, "A cost optimized battery management system with active cell balancing for lithium ion battery stacks", in *2009 IEEE vehicle power and propulsion conference*, IEEE, 2009, pp. 304–309.

[211] A. Zhang, S. Song, C. Wang, J. Zhang, K. Wang, and L. Li, "Research of battery management system for integrated power supply", in *2017 Chinese Automation Congress (CAC)*, IEEE, 2017, pp. 3178–3181.

[212] M. Bowkett, K. Thanapalan, T. Stockley, M. Hathway, and J. Williams, "Design and implementation of an optimal battery management system for hybrid electric vehicles", in *2013 19th International Conference on Automation and Computing*, IEEE, 2013, pp. 1–5.

[213] T. A. Stuart and W. Zhu, "Modularized battery management for large lithium ion cells", *Journal of Power Sources*, vol. 196, no. 1, pp. 458–464, 2011.

[214] I. Pavić, M. Beus, V. Bobanac, and H. Pandžić, "Decentralized Master-Slave Communication and Control Architecture of a Battery Swapping Station", in *2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe)*, IEEE, 2018, pp. 1–6.

[215] K. Čermák and M. Bartl, "Decentralized Battery Management System", in *Proceedings of the 2014 15th International Scientific Conference on Electric Power Engineering (EPE)*, IEEE, 2014, pp. 599–603.

[216] C.-S. Karavas, G. Kyriakarakos, K. G. Arvanitis, and G. Papadakis, "A multi-agent decentralized energy management system based on distributed intelligence for the design and control of autonomous polygeneration microgrids", *Energy Conversion and Management*, vol. 103, pp. 166–179, 2015.

[217] H. Mahmood, D. Michaelson, and J. Jiang, "Decentralized Power Management of a PV/Battery Hybrid Unit in a Droop-Controlled Islanded Microgrid", *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7215–7229, 2015.

[218] D. Andrea, *Battery Management Systems for Large Lithium-Ion Battery Packs*. Artech house, 2010.

[219] X.-f. Wan, J.-p. Wu, and H.-l. Hu, "The smart battery management system", in *2009 International Conference on Test and Measurement*, IEEE, vol. 1, 2009, pp. 29–32.

[220] T. Instruments, *Multicell 36-v to 48-v battery management system reference design*, TI Designs: TIDA-00792, 2017.

[221] C.-H. Kim, M.-Y. Kim, and G.-W. Moon, "A Modularized Charge Equalizer Using a Battery Monitoring IC for Series-Connected Li-Ion Battery Strings in Electric Vehicles", *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3779–3787, 2012.

[222] L. Linlin, Z. Xu, X. Jing, X. Shuntao, *et al.*, "Research on dynamic equalization for lithium battery management system", in *2017 29th Chinese Control And Decision Conference (CCDC)*, IEEE, 2017, pp. 6884–6888.

[223] V. Lorentz, M. Wenger, M. Giegerich, S. Zeltner, M. März, and L. Frey, "Smart battery cell monitoring with contactless data transmission", in *Advanced Microsystems for Automotive Applications 2012: Smart Systems for Safe, Sustainable and Networked Vehicles*, Springer, 2012, pp. 15–26.

[224] D. F. Frost and D. A. Howey, "Completely Decentralized Active Balancing Battery Management System", *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 729–738, 2017.

[225] S. M. Chowdhury, M. O. Badawy, Y. Sozer, and J. A. D. A. Garcia, "A novel battery management system using the duality of the adaptive droop control theory", *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 5078–5088, 2019.

[226] J. Yaoqin, L. Dingkun, and P. Shengkui, "Improved droop control of parallel inverter system in standalone microgrid", in 8^{th} *International Conference on Power Electronics-ECCE Asia*, IEEE, 2011, pp. 1506–1513.

[227] T. M. Haileselassie and K. Uhlen, "Impact of DC line voltage drops on power flow of MTDC using droop control", *IEEE Transactions on Power Systems*, vol. 27, no. 3, pp. 1441–1449, 2012.

[228] S. Augustine, M. K. Mishra, and N. Lakshminarasamma, "Adaptive Droop Control Strategy for Load Sharing and Circulating Current Minimization in Low-Voltage Standalone DC Microgrid", *IEEE Transactions on Sustainable Energy*, vol. 6, no. 1, pp. 132–141, 2014.

[229] X. Lu, J. M. Guerrero, K. Sun, and J. C. Vasquez, "An Improved Droop Control Method for DC Microgrids Based on Low Bandwidth Communication With DC Bus Voltage Restoration and Enhanced Current Sharing Accuracy", *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1800–1812, 2013.

[230] T. Faika, T. Kim, and M. Khan, "An Internet of Things (IoT)-Based Network for Dispersed and Decentralized Wireless Battery Management Systems", in *2018 IEEE Transportation electrification conference and expo (ITEC)*, IEEE, 2018, pp. 1060–1064.

[231] S. Steinhorst, M. Lukasiewycz, S. Narayanaswamy, M. Kauer, and S. Chakraborty, "Smart Cells for Embedded Battery Management", in *2014 IEEE International Conference on Cyber-Physical Systems, Networks, and Applications*, IEEE, 2014, pp. 59–64.

[232] G. Merei, D. Magnor, M. Leuthold, and D. U. Sauer, "Optimization of an off-grid hybrid power supply system based on battery aging models for different battery technologies", in *2014 IEEE 36th International Telecommunications Energy Conference (INTELEC)*, IEEE, 2014, pp. 1–6.

[233] T. Alharbi, K. Bhattacharya, and M. Kazerani, "Planning and Operation of Isolated Microgrids Based on Repurposed Electric Vehicle Batteries", *IEEE Transactions on Industrial Informatics*, vol. 15, no. 7, pp. 4319–4331, 2019.

[234] R. Reinhardt, I. Christodoulou, B. A. García, and S. Gasso-Domingo, "Sustainable business model archetypes for the electric vehicle battery second use industry: Towards a conceptual framework", *Journal of Cleaner Production*, vol. 254, p. 119 994, 2020.

[235] A. Al-Nayeem, M. Sun, X. Qiu, L. Sha, S. P. Miller, and D. D. Cofer, "A Formal Architecture Pattern for Real-Time Distributed System", in *2009 30th IEEE Real-Time Systems Symposium*, IEEE, 2009, pp. 161–170.

[236] A. Reindl, T. Langer, H. Meier, and M. Niemetz, "Comparative reliability analysis for single and dual can (fd) systems", in *2022 International Conference on Applied Electronics (AE)*, IEEE, 2022, pp. 1–6.

[237] A. Reindl, H. Meier, and M. Niemetz, "Software Framework for the Simulation of a Decentralized Battery Management System Consisting of Intelligent Battery Cells", in *2019 IEEE Student Conference on Research and Development (SCOReD)*, IEEE, 2019, pp. 75–80.

[238] M. A. Rahman, K. De Craemer, J. Büscher, J. Driesen, P. Coenen, and C. Mol, "Comparative Analysis of Reconfiguration Assisted Management of Battery Storage Systems", in *IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*, IEEE, vol. 1, 2019, pp. 5921–5926.

[239] F. Zhu, G. Liu, C. Tao, K. Wang, and K. Jiang, "Battery management system for li-ion battery", *The Journal of Engineering*, vol. 2017, no. 13, pp. 1437–1440, 2017.

[240] Z. Weijie, S. Youjie, and L. Bo, "Functional safety analysis and design of bms for lithium-ion battery energy storage system", *Energy Storage Science and Technology*, vol. 9, no. 1, p. 271, 2020.

[241] X. Pu, H. Wang, D. Zhao, H. Yang, X. Ai, S. Cao, Z. Chen, and Y. Cao, "Recent Progress in Rechargeable Sodium-Ion Batteries: toward High-Power Applications", *Small*, vol. 15, no. 32, p. 1 805 427, 2019.

[242] H. Du, S. Feng, W. Luo, L. Zhou, and L. Mai, "Advanced Li-Se_xS_y battery system: Electrodes and electrolytes", *Journal of Materials Science & Technology*, vol. 55, pp. 1–15, 2020.

[243] S. Gentil, D. Reynard, and H. H. Girault, "Aqueous organic and redox-mediated redox flow batteries: A review", *Current Opinion in Electrochemistry*, vol. 21, pp. 7–13, 2020.

[244] A. Reindl, V. Schneider, H. Meier, and M. Niemetz, "Software Update of a Decentralized, Intelligent Battery Management System Based on Multi-Microcomputers", in *Tagungsband 2. Symposium Elektronik und Systemintegration ESI 2020:" Intelligente Systeme und ihre Komponenten: Forschung und industrielle Anwendung"*, 2020, pp. 8–19.

[245] S. Syarmila Bt Sameon, S. Yussof, and B. N. Jørgensen, "Comparison between Communication Technology used in Smart Building", in *2020 8th International Conference on Information Technology and Multimedia (ICIMU)*, 2020, pp. 212–217. DOI: 10.1109/ICIMU49871.2020.9243447.

[246] M. Kuzlu and M. Pipattanasomporn, "Assessment of communication technologies and network requirements for different smart grid applications", in *2013 IEEE PES Innovative Smart Grid Technologies Conference (ISGT)*, 2013, pp. 1–6. DOI: 10.1109/ISGT.2013.6497873.

[247] M. Kuzlu, M. Pipattanasomporn, and S. Rahman, "Review of communication technologies for smart homes/building applications", in *2015 IEEE Innovative Smart Grid Technologies - Asia (ISGT ASIA)*, 2015, pp. 1–6. DOI: 10.1109/ISGT-Asia.2015.7437036.

[248] S. P. Ramalingam and P. K. Shanmugam, "A Comprehensive Review on Wired and Wireless Communication Technologies and Challenges in Smart Residential Buildings", *Recent Advances in Computer Science and Communications (Formerly: Recent Patents on Computer Science)*, vol. 15, no. 9, pp. 1140–1167, 2022.

[249] S. V. Singh, A. Khursheed, and Z. Alam, "Wired Communication Technologies and Networks for Smart Grid—A Review", *Cyber Security in Intelligent Computing and Communications*, pp. 183–195, 2022.

[250] Y. Wu, X. Liao, W. Chen, and D. Chen, "A Battery Management System for electric vehicle based on Zigbee and CAN", in *2011 4th International Congress on Image and Signal Processing*, vol. 5, 2011, pp. 2517–2521. DOI: 10.1109/CISP.2011.6100781.

[251] T. Kumtachi, K. Kinoshita, and T. Watanabe, "Reliable Wireless Communications in Battery Management System of Electric Vehicles", in *2017 Tenth International Conference on Mobile Computing and Ubiquitous Network (ICMU)*, 2017, pp. 1–6. DOI: 10.23919/ICMU.2017.8330099.

[252] R. Gozdur, T. Przerywacz, and D. Bogdański, "Low power modular battery management system with a wireless communication interface", *Energies*, vol. 14, no. 19, p. 6320, 2021.

[253] M. Turgut, R. Bayir, and F. Duran, "CAN communication based modular type battery management system for electric vehicles", *Elektronika ir Elektrotechnika*, vol. 24, no. 3, pp. 53–60, 2018.

[254] A. P. Talie, W. A. Pribyl, and G. Hofer, "Electric Vehicle Battery Management System Using Power Line Communication Technique", in *2018 14th conference on Ph. D. Research in Microelectronics and Electronics (PRIME)*, IEEE, 2018, pp. 225–228.

[255] M. S. Saleem, "Development of PLC based Communication Architecture for Battery Management System", in *2020 IEEE 91st Vehicular Technology Conference (VTC2020-Spring)*, 2020, pp. 1–5. DOI: 10.1109/VTC2020-Spring48590.2020.9128451.

[256] E. Choi, H. Song, S. Kang, and J.-W. Choi, "High-Speed, Low-Latency In-Vehicle Network Based on the Bus Topology for Autonomous Vehicles: Automotive Networking and Applications", *IEEE Vehicular Technology Magazine*, vol. 17, no. 1, pp. 74–84, 2022. DOI: 10.1109/MVT.2021.3128876.

[257] H. Salzwedel, "Comparison of can, flexray, and ethernet architectures for the design of abs systems", SAE Technical paper, Tech. Rep., 2011.

[258] T. Steinbach, F. Korf, and T. C. Schmidt, "Comparing time-triggered Ethernet with FlexRay: An evaluation of competing approaches to real-time for in-vehicle networks", in *2010 IEEE International Workshop on Factory Communication Systems Proceedings*, 2010, pp. 199–202. DOI: 10.1109/WFCS.2010.5548606.

[259] K. French, *Energy consumption of in-vehicle communication in electric vehicles: A comparison between can, ethernet and eee*, 2019.

[260] A. Sawant, S. Lenina, and D. Joshi, "CAN, FlexRay, MOST versus ethernet for vehicular networks", *International Journal of Innovations & Advancement in Computer Science*, vol. 4, 2018.

[261] W. Zeng, M. Khalid, and S. Chowdhury, "A qualitative comparison of FlexRay and Ethernet in vehicle networks", in *2015 IEEE 28th Canadian Conference on Electrical and Computer Engineering (CCECE)*, 2015, pp. 571–576. DOI: 10.1109/CCECE.2015.7129338.

[262] G. W. Scheer and D. J. Dolezilek, "Comparing the reliability of Ethernet network topologies in substation control and monitoring networks", in *Western Power Delivery Automation Conference, Spokane, Washington*, 2000.

[263] B. Brahimi, E. Rondeau, and C. Aubrun, "Comparison between networked control system behaviour based on can and switched ethernet networks", *arXiv preprint cs/0611149*, 2006.

[264] X. Wu and L. Xie, "Performance evaluation of industrial ethernet protocols for networked control application", *Control Engineering Practice*, vol. 84, pp. 208–217, 2019.

[265] FreeRTOS$_{TM}$, *Freertos kernel developer docs*, https://www.freertos.org/features.html.

[266] L. W. lwIP Adam Dunkels, *Lwip 2.1.0 | lightweight ip stack*, http://www.nongnu.org/lwip/2_1_x/index.html.

[267] STMicroelectronics, *Lwip 2.1.0 | lightweight ip stack*, https://www.st.com/resource/en/user_manual/um1713-developing-applications-on-stm32cube-with-lwip-tcpip-stack-stmicroelectronics.pdf, DocID025731 Rev 4, 2015.

[268] STMicroelectronics, *Rm0433 reference manual - stm32h742, stm32h743/753 and stm32h750*, https://www.st.com/resource/en/reference_manual/dm00314099-stm32h742-stm32h743-753-and-stm32h750-value-line-advanced-arm-based-32-bit-mcus-stmicroelectronics.pdf, RM0433 Rev 8, 2023.

[269] M. T. Inc., *Mcp2561/2: High-speed can transceiver*, http://ww1.microchip.com/downloads/en/devicedoc/20005167c.pdf, DS20005167C.

[270] I. by HMS Networks, *Usb-to-can fd: Active usb interface*, https://www.ixxat.com/products/automotive-solutions/overview/pc-interfaces/usb-to-can-fd, DS20005167C.

[271] STMicroelectronics, *Um2407 user manual – stm32h7 nucleo-144 boards (mb1364)*, https://www.st.com/resource/en/user_manual/dm00499160-stm32h7-nucleo144-boards-mb1364-stmicroelectronics.pdf, UM2407 Rev 2, 2020.

[272] M. T. Inc., *Mcp2561/2fd: High-speed can flexible data rate transceiver*, https://ww1.microchip.com/downloads/en/DeviceDoc/20005284A.pdf, DS20005284A.

[273] M. T. Inc., *Lan8742a/lan8742ai small footprint rmii 10/100 ethernet transceiver with hp auto-mdix and flexpwr ®technology*, https://ww1.microchip.com/downloads/en/DeviceDoc/20005284A.pdf, DS20005284A.

[274] R. Bosch, "Can specification", *Robert Bosch GmbH, Stuttgart*, 1991.

[275] R. Bosch, "Can with flexible data-rate specification", *Robert Bosch GmbH, Stuttgart*, 2012.

[276] M. Rahmani, W. Hintermaier, B. Muller-Rathgeber, and E. Steinbach, "Error Detection Capabilities of Automotive Network Technologies and Ethernet – A Comparative Study", pp. 674–679, 2007.

[277] A. Kern, "Ethernet and ip for automotive e/e-architectures-technology analysis, migration concepts and infrastructure", Ph.D. dissertation, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), 2012.

[278] J. Ferreira, A. Oliveira, P. Fonseca, and J. A. Fonseca, "An Experiment to Assess Bit Error Rate in CAN", pp. 15–18, 2004.

[279] A. Mutter, *Can xl specifications and test plans*, https://www.can-cia.org/groups/technical-groups/technical-committee-tc/ig-lower-layers/sig-can-xl/, 2020.

[280] N. Balbierer, T. Waas, J. Noebauer, and J. Seitz, "Energy consumption of ethernet compared to automotive bus networks", pp. 61–66, 2011.

[281] L. L. Bello and W. Steiner, "A perspective on ieee time-sensitive networking for industrial communication and automation systems", *Proceedings of the IEEE*, vol. 107, no. 6, pp. 1094–1120, 2019.

[282] M. Kumar and A. R. Molla, "Brief Announcement: On the Message Complexity of Fault-Tolerant Computation: Leader Election and Agreement", *Proceedings of the 2021 ACM Symposium on Principles of Distributed Computing*, pp. 259–262, 2021.

[283] M. A. Haddar, "SEALEA: scalable and energy aware k-leaders election algorithm in IoT wireless sensor networks", *Wireless Personal Communications*, vol. 125, no. 1, pp. 209–229, 2022.

[284] A. Favier, N. Guittonneau, L. Arantes, A. Fladenmuller, J. Lejeune, and P. Sens, "Topology Aware Leader Election Algorithm for Dynamic Networks", *2020 IEEE 25th Pacific Rim International Symposium on Dependable Computing (PRDC)*, pp. 1–10, 2020. DOI: 10.1109/PRDC50213.2020.00011.

[285] A. Favier, L. Arantes, J. Lejeune, and P. Sens, "Centrality-Based Eventual Leader Election in Dynamic Networks", *2021 IEEE 20th International Symposium on Network Computing and Applications (NCA)*, pp. 1–8, 2021. DOI: 10.1109/NCA53618.2021.9685390.

[286] M. Abdullah, I. Al-Kohali, and M. Othman, "An Adaptive Bully Algorithm for Leader Elections in Distributed Systems", *Parallel Computing Technologies: 15th International Conference*, pp. 373–384, 2019.

[287] H. Svensson and T. Arts, "A New Leader Election Implementation", *Proceedings of the 2005 ACM SIGPLAN Workshop*, pp. 35–39, 2005.

[288] J. Maeng and I. Joe, "Energy-Based Leader Election (E-LE) for Group Management of IoT", *Software Engineering Perspectives in Systems: Proceedings of 11th Computer Science On-line Conference 2022, Vol. 1*, pp. 177–184, 2022.

[289] S. Sharma and A. K. Singh, "An election algorithm to ensure the high availability of leader in large mobile ad hoc networks", *International Journal of Parallel, Emergent and Distributed Systems*, vol. 33, no. 2, pp. 172–196, 2018. DOI: 10.1080/17445760.2016.1191077. [Online]. Available: https://doi.org/10.1080/17445760.2016.1191077.

[290] G. N. Frederickson and N. A. Lynch, "Electing a leader in a synchronous ring", *Journal of the ACM (JACM)*, vol. 34, no. 1, pp. 98–115, 1987.

[291] A. Biswas, A. K. Maurya, A. K. Tripathi, and S. Aknine, "FRLLE: a failure rate and load-based leader election algorithm for a bidirectional ring in distributed systems", *The Journal of Supercomputing*, vol. 77, pp. 751–779, 2021.

[292] P. Flocchini, E. Kranakis, D. Krizanc, F. L. Luccio, and N. Santoro, "Sorting and election in anonymous asynchronous rings", *Journal of Parallel and Distributed Computing*, vol. 64, no. 2, pp. 254–265, 2004.

[293] A. Biswas, A. K. Tripathi, and S. Aknine, "Lea-TN: leader election algorithm considering node and link failures in a torus network", *The Journal of Supercomputing*, vol. 77, pp. 13 292–13 329, 2021.

[294] Y. Mo, G. Audrito, S. Dasgupta, and J. Beal, "Near-optimal knowledge-free resilient leader election", *Automatica*, vol. 146, p. 110 583, 2022.

[295] Y. Mo, G. Audrito, S. Dasgupta, and J. Beal, "A Resilient Leader Election Algorithm Using Aggregate Computing Blocks", *IFAC-PapersOnLine*, vol. 53, no. 2, pp. 3336–3341, 2020.

[296] D. R. Kowalski and M. A. Mosteiro, "Time and Communication Complexity of Leader Election in Anonymous Networks", *2021 IEEE 41st International Conference on Distributed Computing Systems (ICDCS)*, pp. 449–460, 2021. DOI: 10.1109/ICDCS51616.2021.00050.

[297] S. Kutten, W. K. Moses Jr, G. Pandurangan, and D. Peleg, "Singularly Optimal Randomized Leader Election", *arXiv preprint arXiv:2008.02782*, 2020.

[298] X. Défago, Y. Emek, S. Kutten, T. Masuzawa, and Y. Tamura, "Communication Efficient Self-Stabilizing Leader Election", *arXiv preprint arXiv:2008.04252*, 2020.

[299] W. Golab, D. Hendler, and P. Woelfel, "An $\mathcal{O}(1)$ RMRs Leader Election Algorithm", *SIAM Journal on Computing*, vol. 39, no. 7, pp. 2726–2760, 2010.

[300] I. Y. Kim and O. De Weck, "Adaptive weighted sum method for multiobjective optimization: a new method for Pareto front generation", *Structural and multidisciplinary optimization*, vol. 31, no. 2, pp. 105–116, 2006.

[301] R. T. Marler and J. S. Arora, "The weighted sum method for multi-objective optimization: New insights", *Structural and multidisciplinary optimization*, vol. 41, pp. 853–862, 2010.

[302] W. Jakob and C. Blume, "Pareto optimization or cascaded weighted sum: A comparison of concepts", *Algorithms*, vol. 7, no. 1, pp. 166–185, 2014.

[303] A. Reindl, D. Wetzel, N. Balbierer, H. Meier, M. Niemetz, and S. Park, "Comparative Analysis of CAN, CAN FD and Ethernet for Networked Control Systems", *embedded world conference digital*, 2021.

[304] S. STM32, *STM32G474: Arm Cortex-M4 32-bit MCU+FPU, 170 MHz/213 DMIPS, 128 KB SRAM*, https://www.st.com/resource/en/datasheet/stm32g474cb.pdf, DS12288 Rev 6, 2021.

[305] D. Wetzel, A. Reindl, H. Meier, M. Niemetz, and M. Farmbauer, "A customized python interface for windows os for a low budget usb-to-can-adapter", in *2022 International Conference on Electrical, Computer and Energy Technologies (ICECET)*, 2022, pp. 1–5. DOI: 10.1109/ICECET55527.2022.9872574.

[306] M. Pagliaro and F. Meneguzzo, "Lithium battery reusing and recycling: A circular economy insight", *Heliyon*, vol. 5, no. 6, 2019.

[307] M. H. S. M. Haram, J. W. Lee, G. Ramasamy, E. E. Ngu, S. P. Thiagarajah, and Y. H. Lee, "Feasibility of utilising second life ev batteries: Applications, lifespan, economics, environmental impact, assessment, and challenges", *Alexandria Engineering Journal*, vol. 60, no. 5, pp. 4517–4536, 2021.

[308] M. Shahjalal, P. K. Roy, T. Shams, A. Fly, J. I. Chowdhury, M. R. Ahmed, and K. Liu, "A review on second-life of li-ion batteries: Prospects, challenges, and issues", *Energy*, vol. 241, p. 122 881, 2022.

[309] A. Singer, "Evaluierung einer modularen umrichtertopologie zur kombination von batteriesystemen, balancing-systemen, umrichtern und ladeschaltungen", Ph.D. dissertation, Neubiberg, Universität der Bundeswehr München, 2019.

[310] W. Han, T. Wik, A. Kersten, G. Dong, and C. Zou, "Next-generation battery management systems: Dynamic reconfiguration", *IEEE Industrial Electronics Magazine*, vol. 14, no. 4, pp. 20–31, 2020.

[311] M. Mühlbauer, O. Bohlen, and M. A. Danzer, "Analysis of power flow control strategies in heterogeneous battery energy storage systems", *Journal of Energy Storage*, vol. 30, p. 101 415, 2020.

[312] M. Bauer, M. Mühlbauer, O. Bohlen, M. A. Danzer, and J. Lygeros, "Power flow in heterogeneous battery systems", *Journal of Energy Storage*, vol. 25, p. 100 816, 2019.

[313] M. Mühlbauer, F. Rang, H. Palm, O. Bohlen, and M. A. Danzer, "Pareto-optimal power flow control in heterogeneous battery energy storage systems", *Journal of Energy Storage*, vol. 48, p. 103 803, 2022.

[314] C. N. Truong, "Assessment and optimization of operating stationary battery storage systems", Ph.D. dissertation, Technische Universität München, 2019.

[315] A. Reindl, H. Meier, and M. Niemetz, "Scalable, decentralized battery management system based on self-organizing nodes", in *International Conference on Architecture of Computing Systems*, Springer, 2020, pp. 171–184.

[316] M. Mehdi, C.-H. Kim, and M. Saad, "Robust centralized control for dc islanded microgrid considering communication network delay", *IEEE Access*, vol. 8, pp. 77 765–77 778, 2020.

[317] A. Khorsandi, M. Ashourloo, and H. Mokhtari, "A decentralized control method for a low-voltage dc microgrid", *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 793–801, 2014.

[318] C. Guo, J. Liao, and Y. Zhang, "Adaptive droop control of unbalanced voltage in the multi-node bipolar dc microgrid based on fuzzy control", *International Journal of Electrical Power & Energy Systems*, vol. 142, p. 108 300, 2022.

[319] S. Ansari, J. Zhang, and R. E. Singh, "A review of stabilization methods for dcmg with cpl, the role of bandwidth limits and droop control", *Protection and Control of Modern Power Systems*, vol. 7, no. 1, pp. 1–12, 2022.

[320] X. Tian, Y. Wang, F. Wang, and Z. Guo, "An adaptive nonlinear droop control for accurate load current sharing and dc bus voltage compensation in a dc power system", *Journal of Power Electronics*, vol. 22, no. 2, pp. 308–317, 2022.

[321] R. Dadi, K. Meenakshy, and S. K. Damodaran, "A review on secondary control methods in dc microgrid", *Journal of Operation and Automation in Power Engineering*, vol. 11, no. 2, pp. 105–112, 2023.

[322] S. Moayedi, V. Nasirian, F. L. Lewis, and A. Davoudi, "Team-oriented load sharing in parallel dc–dc converters", *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 479–490, 2014.

[323] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. De Vicuña, and M. Castilla, "Hierarchical control of droop-controlled ac and dc microgrids—a general approach toward standardization", *IEEE Transactions on industrial electronics*, vol. 58, no. 1, pp. 158–172, 2010.

[324] A. Bidram and A. Davoudi, "Hierarchical structure of microgrids control system", *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 1963–1976, 2012.

[325] X. Li and D. Zhang, "Coordinated control and energy management strategies for hundred megawatt-level battery energy storage stations based on multi-agent theory", in *2018 International Conference on Advanced Mechatronic Systems (ICAMechS)*, IEEE, 2018, pp. 1–5.

[326] M. Vašak, A. Banjac, N. Hure, H. Novak, D. Marušić, and V. Lešić, "Modular hierarchical model predictive control for coordinated and holistic energy management of buildings", *IEEE Transactions on Energy Conversion*, vol. 36, no. 4, pp. 2670–2682, 2021.

[327] X. Huang, W. Liu, A. B. Acharya, J. Meng, R. Teodorescu, and D.-I. Stroe, "Effect of pulsed current on charging performance of lithium-ion batteries", *IEEE Transactions on Industrial Electronics*, vol. 69, no. 10, pp. 10 144–10 153, 2021.

[328] X. Huang, "The effects of pulsed charging current on the performance and lifetime of lithium-ion batteries", 2021.

[329] Q. Lin, J. Wang, R. Xiong, W. Shen, and H. He, "Towards a smarter battery management system: A critical review on optimal charging methods of lithium ion batteries", *Energy*, vol. 183, pp. 220–234, 2019.

[330] E. Wikner and T. Thiringer, "Extending battery lifetime by avoiding high soc", *Applied Sciences*, vol. 8, no. 10, p. 1825, 2018.

[331] E. Wikner, E. Björklund, J. Fridner, D. Brandell, and T. Thiringer, "How the utilised soc window in commercial li-ion pouch cells influence battery ageing", *Journal of Power Sources Advances*, vol. 8, p. 100 054, 2021.

[332] W. Yu, H. Qian, and J.-S. Lai, "Design of high-efficiency bidirectional dc–dc converter and high-precision efficiency measurement", *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 650–658, 2009.

[333] V. Nasirian, A. Davoudi, F. L. Lewis, and J. M. Guerrero, "Distributed adaptive droop control for dc distribution systems", *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 944–956, 2014.

[334] N. Bhatt, R. Sondhi, and S. Arora, "Droop control strategies for microgrid: A review", *Advances in Renewable Energy and Electric Vehicles*, pp. 149–162, 2022.

[335] Texas Instruments, *LM5170 48V-12V Bidirectional Converter Evaluation Module: LM5170 EVM-BIDIR datasheet*, Datasheet, 2016.

[336] M. Jupke, A. Reindl, H. Meier, and M. Niemetz, "Bidirectional dc-dc converter with digital droop parameterization", in *2021 International Conference on Applied Electronics (AE)*, IEEE, 2021, pp. 1–6.

[337] K. Aström, "Theory and applications of adaptive control", *IFAC Proceedings Volumes*, vol. 14, no. 2, pp. 737–748, 1981.

[338] S.-Y. Cheong and M. G. Safonov, "Bumpless transfer for adaptive switching controls", *IFAC Proceedings Volumes*, vol. 41, no. 2, pp. 14 415–14 420, 2008.

[339] J. Shi and J. Zhao, "State bumpless transfer control for a class of switched descriptor systems", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 9, pp. 3846–3856, 2021.

[340] Int. Energy Agency (IEA), *Global ev outlook 2020: Entering the decade of electric drive?*, 2020.

[341] P. H. H. Engel and G. Siccardo, *Second-life ev batteries: The newest value pool in energy storage*, 2019.

[342] Berylls Strategy Advisors, *Projected global second life battery capacity from 2023 to 2030 (in gigawatt hours)*, 2023.

[343] L. Chang, C. Ma, Y. Zhang, H. Li, and L. Xiao, "Experimental assessment of the discharge characteristics of multi-type retired lithium-ion batteries in parallel for echelon utilization", *Journal of Energy Storage*, 2022.

[344] W. Han and A. Kersten, "Analysis and estimation of the maximum circulating current during the parallel operation of reconfigurable battery systems", *2020 IEEE Transportation Electrification Conf. & Expo (ITEC)*, 2020. DOI: 10.1109/ITEC48692.2020.9161478.

[345] R. Erickson and D. Maksimovic, "High efficiency dc-dc converters for battery-operated systems with energy management", *Worldwide wireless communications, annual reviews on telecommunications*, pp. 1–10, 1995.

[346] Q. Xu, N. Vafamand, L. Chen, T. Dragičević, L. Xie, and F. Blaabjerg, "Review on advanced control technologies for bidirectional dc/dc converters in dc microgrids", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1205–1221, 2021. DOI: 10.1109/JESTPE.2020.2978064.

[347] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages", *IEEE power electronics specialists Conf.*, 1976.

[348] G. W. Wester and R. D. Middlebrook, "Low-frequency characterization of switched dc-dc converters", *IEEE Trans. on Aerospace and electronic Systems*, 1973.

[349] W. M. Polivka, P. R. Chetty, and R. D. Middlebrook, "State-Space Average modelling of converters with parasitics and storage-time modulation", *IEEE Power Electronics Specialists Conf.*, 1980. DOI: 10.1109/PESC.1980.7089440.

[350] J. Mahdavi, A. Emadi, and H. Toliyat, "Application of state space averaging method to sliding mode control of PWM DC/DC converters", *IEEE Industry Applications Conf.*, 1997. DOI: 10.1109/IAS.1997.628957.

[351] R. H. Tan and L. Y. H. Hoo, "DC-DC converter modeling and simulation using state space approach", *IEEE Conf. on Energy Conversion*, 2015. DOI: 10.1109/CENCON.2015.7409511.

[352] C. Rim, G. Joung, and G.-H. Cho, "A state space modeling of non-ideal DC-DC converters", *IEEE Power Electronics Specialists Conf.*, 1988.

[353] I. Zafrany and S. Ben-Yaakov, "Generalized switched inductor model (GSIM): accounting for conduction losses", *IEEE Trans. on Aerospace and Electronic Systems*, 2002.

[354] I. Zafrany and S. Ben-Yaakov, "Average modeling, analysis and simulation of current shared DC-DC converters", *IEEE Power Electronics Specialists Conf.*, 1998. DOI: 10.1109/PESC.1998.701966.

[355] S. Ben-Yaakov, "The unified switched inductor model", *Convention of Electrical and Electronics Engineers*, 1991. DOI: 10.1109/EEIS.1991.217704.

[356] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer, 2001.

[357] R. W. Erickson, "DC–DC power converters", *Wiley encyclopedia of electrical and electronics engineering*, 2001.

[358] V. Dijk et al., "PWM-switch modeling of DC-DC converters", *IEEE Trans. on Power Electronics*, 1995. DOI: 10.1109/63.471285.

[359] D. Tannir, Y. Wang, and P. Li, "Accurate modeling of nonideal low-power PWM DC-DC converters operating in CCM and DCM using enhanced circuit-averaging techniques", *ACM Trans. on Design Automation of Electronic Systems*, 2016.

[360] J. Chen, R. Erickson, and D. Maksimovic, "Averaged switch modeling of boundary conduction mode DC-to-DC converters", *Conf. of the IEEE Industrial Electronics Society*, 2001.

[361] T.-F. Wu and Y.-K. Chen, "An alternative approach to systematically modeling PWM DC/DC converters in DCM based on the graft scheme", *IEEE Power Electronics Specialists Conf.*, 1997.

[362] H. Abdel-Gawad and V. Sood, "Small-signal analysis of boost converter, including parasitics, operating in CCM", *IEEE power India Int. Conf.*, pp. 1–5, 2014.

[363] A. Ayachit, A. Reatti, and M. K. Kazimierczuk, "Small-signal modeling of the PWM boost DC-DC converter at boundary-conduction mode by circuit averaging technique", *IEEE Int. Symposium on Circuits and Systems*, 2015.

[364] A. Ayachit and M. K. Kazimierczuk, "Averaged small-signal model of pwm dc-dc converters in ccm including switching power loss", *IEEE Trans. on Circuits and Systems*, 2018.

[365] A. Chadha and M. K. Kazimierczuk, "Small-signal modeling of open-loop PWM tapped-inductor buck DC–DC converter in CCM", *IEEE Trans. on Industrial Electronics*, 2020.

[366] A. Reatti and M. K. Kazimierczuk, "Small-signal model of pwm converters for discontinuous conduction mode and its application for boost converter", *IEEE Trans. on Circuits and Systems*, 2003.

[367] A. Davoudi, J. Jatskevich, and T. De Rybel, "Numerical state-space average-value modeling of PWM DC-DC converters operating in DCM and CCM", *IEEE Trans. on power electronics*, 2006.

[368] J. Han, B. Zhang, and D. Qiu, "Bi-switching Status Modeling Method for DC–DC Converters in CCM and DCM Operations", *IEEE Trans. on Power Electronics*, 2017. DOI: 10.1109/TPEL.2016.2574894.

[369] W. Jiang, Y.-f. Zhou, and J.-n. Chen, "Modeling and simulation of Boost converter in CCM and DCM", *Int. Conf. on Power Electronics and Intelligent Transportation System*, 2009. DOI: 10.1109/PEITS.2009.5406859.

[370] H. Kanaan and K. Al-Haddad, "Modeling and Simulation of DC-DC Power Converters in CCM and DCM Using the Switching Functions Approach: Application to the Buck and Cùk Converters", *Int. Conf. on Power Electronics and Drives Systems*, 2005. DOI: 10.1109/PEDS.2005.1619732.

[371] Y. Wang, D. Gao, D. A. Tannir, and P. Li, "Multi-harmonic nonlinear modeling of low-power PWM DC-DC converters operating in CCM and DCM", *Design, Automation and Test Conf. (DATE)*, 2016.

[372] P. Wang, X. Chen, C. Tong, P. Jia, and C. Wen, "Large- and Small-Signal Average-Value Modeling of Dual-Active-Bridge DC–DC Converter With Triple-Phase-Shift Control", *IEEE Trans. on Power Electronics*, 2021. DOI: 10.1109/TPEL.2021.3052459.

[373] F. Krismer and J. W. Kolar, "Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge", *IEEE Trans. on power electronics*, 2009.

[374] K. Xiangli, S. Li, and K. M. Smedley, "Decoupled PWM plus phase-shift control for a dual-half-bridge bidirectional DC–DC converter", *IEEE Trans. on Power Electronics*, 2017.

[375] A. A. Gómez, A. Rodríguez, M. M. Hernando, D. G. Lamar, J. Sebastián, I. Ayarzaguena, J. M. Bermejo, I. Larrazabal, D. Ortega, and F. Vázquez, "Dynamic average small signal model of the SAB converter", *European Conf. on Power Electronics and Applications*, 2022.

[376] H. Li, D. Liu, F. Peng, and G.-J. Su, "Small signal analysis of a dual half bridge isolated ZVS bi-directional DC-DC converter for electrical vehicle applications", *Ppower Electronics Specialists Conf.*, 2005.

[377] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge DC–DC converter", *IEEE Trans. on power electronics*, 2011.

[378] A. Luchetta, S. Manetti, M. C. Piccirilli, A. Reatti, and M. K. Kazimierczuk, "Effects of parasitic components on diode duty cycle and small-signal model of PWM DC-DC buck converter in DCM", *Int. Conf. on Environment and Electrical Engineering*, 2015.

[379] G. Nirgude, R. Tirumala, and N. Mohan, "A new, large-signal average model for single-switch DC-DC converters operating in both CCM and DCM", *Annual Power Electronics Specialists Conf.*, 2001.

[380] N. Femia and V. Tucci, "On the modeling of pwm converters for large signal analysis in discontinuous conduction mode", *IEEE Trans. on Power Electronics*, 1994.

[381] B. Bryant and M. Kazimierczuk, "Open-loop power-stage transfer functions relevant to current-mode control of boost PWM converter operating in CCM", *IEEE Trans. on Circuits and Systems I: Regular Papers*, 2005. DOI: 10.1109/TCSI.2005.852919.

[382] F. Zach, *Leistungselektronik: Ein Handbuch*. Springer, 2015, ISBN: 9783658048990.

[383] A. Reindl, F. Lausser, L. Eriksson, S. Park, M. Niemetz, and H. Meier, "Control Oriented Mathematical Modeling of a Bidirectional DC-DC Converter - Part 1: Buck Mode",

[384] A. Reindl, F. Lausser, L. Eriksson, S. Park, M. Niemetz, and H. Meier, "Control Oriented Mathematical Modeling of a Bidirectional DC-DC Converter - Part 2: Boost Mode",

[385] F. Zach, *Leistungselektronik: Ein Handbuch Band 1/Band 2*. Springer-Verlag, 2015, vol. 2.

[386] L. Dixon, "Average current mode control of switching power supplies", in *Unitrode Power Supply Design Seminar Handbook*, Unitrode Corporation Merrimack, NH, USA, 1990, pp. 5–1.

[387] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[388] Texas Instruments Incorporated, *LM5170-Q1 Multiphase Bidirectional Current Controller*, Texas Instruments Incorporated, Ed., 2016. [Online]. Available: %5Curl%7Bhttps://www.ti.com/product/LM5170-Q1?qgpn=lm5170-q1%7D.

[389] M. Schuck and R. C. N. Pilawa-Podgurski, "Current ripple cancellation for asymmetric multiphase interleaved dc-dc switching converters", *2013 IEEE Power and Energy Conference at Illinois (PECI)*, pp. 162–168, 2013.

[390] *Dc/dc converter stability measurement*, https://www.omicron-lab.com/applications/detail/news/dcdc-converter-stability-measurement, [Online; accessed 22-04-2023].

[391] I. Batarseh, K. Siri, and H. Lee, "Investigation of the output droop characteristics of parallel-connnected dc-dc converters", in *Proceedings of 1994 Power Electronics Specialist Conference - PESC'94*, vol. 2, 1994, 1342–1351 vol.2. DOI: 10.1109/PESC.1994.373859.

[392] D. Cheng, X. Liu, and Y. Lee, "Parallel operation of dc-dc converters with synchronous rectifiers", in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No. 98CH36196)*, IEEE, vol. 2, 1998, pp. 1225–1229.

[393] L. Qu, D. Zhang, and Z. Bao, "Output current-differential control scheme for input-series–output-parallel-connected modular dc–dc converters", *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5699–5711, 2017. DOI: 10.1109/TPEL.2016.2607459.

[394] Y. Huang and K. T. Chi, "Circuit theoretic classification of parallel connected dc–dc converters", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1099–1108, 2007.

[395] D. S. Garabandic and T. B. Petrovic, "Modeling parallel operating pwm dc/dc power supplies", *IEEE Transactions on Industrial Electronics*, vol. 42, no. 5, pp. 545–551, 1995.

[396] S. Luo, Z. Ye, R.-L. Lin, and F. C. Lee, "A classification and evaluation of paralleling methods for power supply modules", in *30th Annual IEEE Power Electronics Specialists Conference. Record.(Cat. No. 99CH36321)*, IEEE, vol. 2, 1999, pp. 901–908.

[397] A. Bogza and D. Floricau, "The parallel connection of phase-shifted full-bridge dc-dc converters", *Rev. Roum. Sci. Techn.–Électrotechn. Et Énerg*, vol. 65, no. 4, pp. 229–234, 2020.

[398] S. Dahale, A. Das, N. M. Pindoriya, and S. Rajendran, "An overview of dc-dc converter topologies and controls in dc microgrid", in *2017 7th International Conference on Power Systems (ICPS)*, IEEE, 2017, pp. 410–415.

[399] M. Su, Z. Liu, Y. Sun, H. Han, and X. Hou, "Stability analysis and stabilization methods of dc microgrid with multiple parallel-connected dc–dc converters loaded by cpls", *IEEE Transactions on Smart Grid*, vol. 9, no. 1, pp. 132–142, 2018. DOI: 10.1109/TSG.2016.2546551.

[400] V. P. Oberto, M. D. Depexe, T. C. Naidon, and A. Campos, "An improved droop control strategy for load current sharing in output parallel-connected dc-dc converters", in *2014 11th IEEE/IAS International Conference on Industry Applications*, 2014, pp. 1–7. DOI: 10.1109/INDUSCON.2014.7059404.

[401] D. Schweiner, D. Kováč, P. Jacko, J. Molnár, and O. Kravets, "Droop methods for parallel co-working of dc/dc converters", in *2017 International Conference on Modern Electrical and Energy Systems (MEES)*, IEEE, 2017, pp. 268–271.

[402] V. Thomas, K. S., and A. S., "Control of parallel dc-dc converters in a dc microgrid using virtual output impedance method", in *2016 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)*, 2016, pp. 587–591. DOI: 10.1109/AEEICB.2016.7538358.

[403] A. Tuladhar and H. Jin, "A novel control technique to operate dc/dc converters in parallel with no control interconnections", in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No. 98CH36196)*, IEEE, vol. 1, 1998, pp. 892–898.

[404] S. Golestan, M. Joorabian, H. Rastegar, A. Roshan, and J. M. Guerrero, "Droop based control of parallel-connected single-phase inverters in dq rotating frame", in *2009 IEEE International Conference on Industrial Technology*, IEEE, 2009, pp. 1–6.

[405] M. López, L. G. de Vicuña, M. Castilla, P. Gayà, and O. López, "Current distribution control design for paralleled dc/dc converters using sliding-mode control", *IEEE Transactions on Industrial Electronics*, vol. 51, no. 2, pp. 419–428, 2004.

[406] I. Kondratiev and R. Dougal, "Current distribution control design for paralleled dc/dc converters using synergetic control theory", in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 851–857. DOI: 10.1109/PESC.2007.4342099.

[407] H. Wang, M. Han, R. Han, J. M. Guerrero, and J. C. Vasquez, "A decentralized current-sharing controller endows fast transient response to parallel dc–dc converters", *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4362–4372, 2018. DOI: 10.1109/TPEL.2017.2714342.

[408] Y. Liu, Y. Han, C. Lin, P. Yang, and C. Wang, "Design and implementation of droop control strategy for dc microgrid based on multiple dc/dc converters", in *2019 IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia)*, IEEE, 2019, pp. 3896–3901.

[409] S. Augustine, M. K. Mishra, and N. Lakshminarasamma, "An improved droop control algorithm for load sharing and circulating current control for parallel dc-dc converters in standalone dc microgrid", in *2014 Annual International Conference on Emerging Research Areas: Magnetics, Machines and Drives (AICERA/iCMMD)*, 2014, pp. 1–6. DOI: 10.1109/AICERA.2014.6908222.

[410] C. Zhang, P. Li, and Y. Guo, "Bidirectional dc/dc and soc drooping control for dc microgrid application", *Electronics*, vol. 9, no. 2, 2020, ISSN: 2079-9292. DOI: 10.3390/electronics9020225. [Online]. Available: https://www.mdpi.com/2079-9292/9/2/225.

[411] Shivam and R. Dahiya, "Distributed control for dc microgrid based on optimized droop parameters", *IETE journal of research*, vol. 66, no. 2, pp. 192–203, 2020.

[412] N. Ghanbari and S. Bhattacharya, "Suppressing circulating currents of battery management systems in droop based microgrids", in *2020 IEEE Transportation Electrification Conference & Expo (ITEC)*, 2020, pp. 871–876. DOI: 10.1109/ITEC48692.2020.9161652.

[413] L. Meng, T. Dragicevic, J. C. Vasquez, and J. M. Guerrero, "Tertiary and secondary control levels for efficiency optimization and system damping in droop controlled dc–dc converters", *IEEE Transactions on Smart Grid*, vol. 6, no. 6, pp. 2615–2626, 2015. DOI: 10.1109/TSG.2015.2435055.

[414] J. Zhao and F. Dörfler, "Distributed control and optimization in dc microgrids", *Automatica*, vol. 61, pp. 18–26, 2015.

[415] M. Srinivasan and A. Kwasinski, "Control analysis of parallel dc-dc converters in a dc microgrid with constant power loads", *International Journal of Electrical Power & Energy Systems*, vol. 122, p. 106 207, 2020, ISSN: 0142-0615. DOI: https://doi.org/10.1016/j.ijepes.2020.106207. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0142061519334040.

[416] K. Siri, C. Lee, and T.-E. Wu, "Current distribution control for parallel connected converters. i", *IEEE Transactions on Aerospace and Electronic Systems*, vol. 28, no. 3, pp. 829–840, 1992.

[417] B. Suprianto, M. Ashari, M. Purnomo, M. Pujiantara, and H. S. Atmojo, "Uniform current distribution control using fuzzy logic for parallel connected non identic dc-dc converters", in *Second International Conference on Innovative Computing, Informatio and Control (ICICIC 2007)*, IEEE, 2007, pp. 435–435.

[418] J. M. Guerrero, L. G. De Vicuña, J. Miret, J. Matas, and O. López, "Parallel operation of charge-controlled dc-dc converters", in *Industrial Electronics, 2002. ISIE 2002. Proceedings of the 2002 IEEE International Symposium on*, IEEE, vol. 4, 2002, pp. 1086–1090.

[419] L. Qu, D. Zhang, and Z. Bao, "Output current-differential control scheme for input-series–output-parallel-connected modular dc–dc converters", *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5699–5711, 2016.

[420] S. K. Mazumder, M. Tahir, and K. Acharya, "Master–slave current-sharing control of a parallel dc–dc converter system over an rf communication interface", *IEEE transactions on industrial electronics*, vol. 55, no. 1, pp. 59–66, 2008.

[421] A. Elbkosh, D. Giaouris, V. Pickert, B. Zahawi, and S. Banerjee, "Stability analysis and control of bifurcations of parallel connected dc/dc converters using the monodromy matrix", in *2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2008, pp. 556–559. DOI: 10.1109/ISCAS.2008.4541478.

[422] A. Khalil, O. Mohamed, and J. Wang, "Networked control of parallel dc/dc buck converters", in *2015 IEEE Jordan conference on applied electrical engineering and computing technologies (AEECT)*, IEEE, 2015, pp. 1–6.

[423] E. De Din, H. A. B. Siddique, M. Cupelli, A. Monti, and R. W. De Doncker, "Voltage control of parallel-connected dual-active bridge converters for shipboard applications", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 664–673, 2018. DOI: 10.1109/JESTPE.2017.2786350.

[424] S.-Y. Chen, B.-C. Yang, T.-A. Pu, C.-H. Chang, and R.-C. Lin, "Active current sharing of a parallel dc-dc converters system using bat algorithm optimized two-dof pid control", *IEEE Access*, vol. 7, pp. 84 757–84 769, 2019.

[425] T. Ouchi, A. Kanoda, and N. Takahashi, "Parallel bi-directional dc-dc converter for energy storage system", in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014-ECCE ASIA)*, IEEE, 2014, pp. 3920–3927.

[426] P. Li and B. Lehman, "A design method for paralleling current mode controlled dc-dc converters", *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 748–756, 2004.

[427] T. Wu, K. Siri, and J. Banda, "The central-limit control and impact of cable resistance in current distribution for parallel-connected dc-dc converters", in *Proceedings of 1994 Power Electronics Specialist Conference - PESC'94*, vol. 1, 1994, 694–702 vol.1. DOI: 10.1109/PESC.1994.349662.

[428] K. Siri and J. Banda, "Current distribution for parallel-connected dc power sources without remote sensing", in *Proceedings of Intelec 94*, 1994, pp. 196–203. DOI: 10.1109/INTLEC.1994.396655.

[429] J. Banda and K. Siri, "Improved central-limit control for parallel-operation of dc-dc power converters", in *Proceedings of PESC '95 - Power Electronics Specialist Conference*, vol. 2, 1995, 1104–1110 vol.2. DOI: 10.1109/PESC.1995.474953.

[430] K. Siri, C. Lee, and T.-E. Wu, "Current distribution control for parallel connected converters. i", *IEEE Transactions on Aerospace and Electronic Systems*, vol. 28, no. 3, pp. 829–840, 1992. DOI: 10.1109/7.256303.

[431] C. Terlizzi, S. Bifaretti, and A. Lampasi, "Current sharing control strategy for parallel-connected h-bridges dc-dc converter: Modelling, analysis and hil test", in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 2777–2783. DOI: 10.1109/ECCE47101.2021.9595565.

[432] M. S. Sadabadi, "A distributed control strategy for parallel dc-dc converters", *IEEE Control Systems Letters*, vol. 5, no. 4, pp. 1231–1236, 2021. DOI: 10.1109/LCSYS.2020.3025411.

[433] M. S. Sadabadi, N. Mijatovic, J.-F. Trégouët, and T. Dragičević, "Distributed control of parallel dc–dc converters under fdi attacks on actuators", *IEEE Transactions on Industrial Electronics*, vol. 69, no. 10, pp. 10 478–10 488, 2022. DOI: 10.1109/TIE.2021.3123613.

[434] H. Yang, Q. Fu, B. Wang, Y. Chen, and Y. Su, "Communication-free interleaving control of parallel-connected dc-dc converters", *Electronics*, vol. 12, no. 9, p. 2111, 2023.

[435] V. Chunkag, Y. Kanthaphayao, and U. Kamnarn, "Distributed control system for a parallel-connected ac/dc converters", *IET Power Electronics*, vol. 6, no. 3, pp. 446–456, 2013.

[436] V. Oberto, M. Depexe, T. Naidon, and A. Campos, "A decentralized current sharing control strategy for output parallel-connected dc-dc converters with true redundancy", in *2014 11th IEEE/IAS International Conference on Industry Applications*, IEEE, 2014, pp. 1–8.

[437] K. Sun, L. Zhang, Y. Xing, and J. M. Guerrero, "A distributed control strategy based on dc bus signaling for modular photovoltaic generation systems with battery energy storage", *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 3032–3045, 2011.

[438] P. D. Garcia, P. Cortizo, B. De Menezes, and M. S. Mendes, "Sliding mode control for current distribution in dc-to-dc converters connected in parallel", in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, IEEE, vol. 2, 1996, pp. 1513–1518.

[439] P. Donoso-Garcia, P. C. Cortizo, B. R. de Menezes, and M. S. Mendes, "Sliding-mode control for current distribution in parallel-connected dc–dc converters", *IEE Proceedings-Electric Power Applications*, vol. 145, no. 4, pp. 333–338, 1998.

[440] V. J. Thottuvelil and G. C. Verghese, "Analysis and control design of paralleled dc/dc converters with current sharing", in *Proceedings of APEC 97-Applied Power Electronics Conference*, IEEE, vol. 2, 1997, pp. 638–646.

[441] I. Kondratiev, E. Santi, R. Dougal, and G. Veselov, "Synergetic control for m-parallel connected dc-dc buck converters", in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, vol. 1, 2004, 182–188 Vol.1. DOI: 10.1109/PESC.2004.1355739.

[442] J. Hamar and A. Toth, "Agent-based control of parallel dc-dc converters", in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–10.

[443] M. Gray, Z. Gao, and R. Button, "Distributed, master-less control of modular dc-dc converters", in *2nd International Energy Conversion Engineering Conference*, 2004, p. 5733.

[444] L. Meng, T. Dragicevic, J. M. Guerrero, and J. C. Vasquez, "Optimization with system damping restoration for droop controlled dc-dc converters", in *2013 IEEE Energy Conversion Congress and Exposition*, IEEE, 2013, pp. 65–72.

[445] S. Moayedi, V. Nasirian, F. L. Lewis, and A. Davoudi, "Team-oriented load sharing in parallel dc–dc converters", *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 479–490, 2015. DOI: 10.1109/TIA.2014.2336982.

[446] Z. M. Pinter, D. Papageorgiou, G. Rohde, M. Marinelli, and C. Træholt, "Review of control algorithms for reconfigurable battery systems with an industrial example", in *2021 56th International Universities Power Engineering Conference (UPEC)*, IEEE, 2021, pp. 1–6.

[447] S. Ci, N. Lin, and D. Wu, "Reconfigurable battery techniques and systems: A survey", *IEEE Access*, vol. 4, pp. 1175–1189, 2016. DOI: 10.1109/ACCESS.2016.2545338.

[448] C. Wang, G. Yin, F. Lin, M. P. Polis, C. Zhang, J. Jiang, *et al.*, "Balanced control strategies for interconnected heterogeneous battery systems", *IEEE Transactions on Sustainable Energy*, vol. 7, no. 1, pp. 189–199, 2015.

[449] Z. M. Pinter, D. Papageorgiou, G. Rohde, M. Marinelli, and C. Træholt, "Review of control algorithms for reconfigurable battery systems with an industrial example", in *2021 56th International Universities Power Engineering Conference (UPEC)*, 2021, pp. 1–6. DOI: 10.1109/UPEC50034.2021.9548259.

[450] G. Gunlu, "Dynamically reconfigurable independent cellular switching circuits for managing battery modules", *IEEE Transactions on Energy Conversion*, vol. 32, no. 1, pp. 194–201, 2016.

[451] M. M. U. Rehman, F. Zhang, R. Zane, and D. Maksimovic, "Control of bidirectional dc/dc converters in reconfigurable, modular battery systems", in *2017 IEEE applied power electronics conference and exposition (APEC)*, IEEE, 2017, pp. 1277–1283.

[452] S. Wang, L. Lu, X. Han, M. Ouyang, and X. Feng, "Virtual-battery based droop control and energy storage system size optimization of a dc microgrid for electric vehicle fast charging station", *Applied Energy*, vol. 259, p. 114 146, 2020, ISSN: 0306-2619. DOI: https://doi.org/10.1016/j.apenergy.2019.114146. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0306261919318331.

[453] K. Bi, W. Yang, D. Xu, and W. Yan, "Dynamic soc balance strategy for modular energy storage system based on adaptive droop control", *IEEE Access*, vol. 8, pp. 41 418–41 431, 2020.

[454] P. Monica and M. Kowsalya, "Current sharing control of parallel bidirectional dc-dc converter for energy storage applications in islanded microgrid", in *2019 IEEE 13th International Conference on Power Electronics and Drive Systems (PEDS)*, IEEE, 2019, pp. 1–6.

[455] T. Morstyn, B. Hredzak, and V. G. Agelidis, "Cooperative multi-agent control of heterogeneous storage devices distributed in a dc microgrid", *IEEE Transactions on Power Systems*, vol. 31, no. 4, pp. 2974–2986, 2015.

[456] Y. Zhang, Y. Song, and S. Fei, "Consensus design for heterogeneous battery energy storage systems with droop control considering geographical factor", *Applied Sciences*, vol. 10, no. 2, p. 726, 2020.

[457] J. Khazaei and D. H. Nguyen, "Multi-agent consensus design for heterogeneous energy storage devices with droop control in smart grids", *IEEE Transactions on Smart Grid*, vol. 10, no. 2, pp. 1395–1404, 2019. DOI: 10.1109/TSG.2017.2765241.

[458] W. Pinthurat and B. Hredzak, "Fully decentralized control strategy for heterogeneous energy storage systems distributed in islanded dc datacentre microgrid", *Energy*, vol. 231, p. 120 914, 2021, ISSN: 0360-5442. DOI: https://doi.org/10.1016/j.energy.2021.120914. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0360544221011622.

[459] R. Zhang, B. Hredzak, and T. Morstyn, "Distributed control with virtual capacitance for the voltage restorations, state of charge balancing, and load allocations of heterogeneous energy storages in a dc datacenter microgrid", *IEEE Transactions on Energy Conversion*, vol. 34, no. 3, pp. 1296–1308, 2019. DOI: 10.1109/TEC.2018.2889065.

[460] Y. Qian, Y. Yang, C. Qi, and T. Xia, "Distributed voltage and energy control for heterogeneous battery energy storage systems with actuator faults via dynamic triggered mechanism", in *2022 41st Chinese Control Conference (CCC)*, 2022, pp. 4419–4424. DOI: 10.23919/CCC55666.2022.9902774.

[461] J. Hu and A. Lanzon, "Distributed finite-time consensus control for heterogeneous battery energy storage systems in droop-controlled microgrids", *IEEE Transactions on Smart Grid*, vol. 10, no. 5, pp. 4751–4761, 2019. DOI: 10.1109/TSG.2018.2868112.

[462] V. Vaishnav, D. Sharma, and A. Jain, "Control of heterogeneous battery energy storage systems-based microgrid connected via detail-balanced communication topology", *IEEE Control Systems Letters*, vol. 7, pp. 733–738, 2023. DOI: 10.1109/LCSYS.2022.3223305.

[463] L. Ding, D. Yue, and Q.-L. Han, "Distributed secondary control for microgrids with heterogeneous battery energy storage systems under switching communication topology", in *IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*, IEEE, vol. 1, 2019, pp. 6249–6254.

[464] Y. Kim, J. Koh, Q. Xie, Y. Wang, N. Chang, and M. Pedram, "A scalable and flexible hybrid energy storage system design and implementation", *Journal of Power Sources*, vol. 255, pp. 410–422, 2014, ISSN: 0378-7753. DOI: https://doi.org/10.1016/j.jpowsour.2013.12.102. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378775313020910.

[465] R. Zhang, B. Hredzak, and T. Morstyn, "Cooperative control of distributed heterogeneous energy storage devices with virtual impedance", in *2017 IEEE Innovative Smart Grid Technologies-Asia (ISGT-Asia)*, IEEE, 2017, pp. 1–6.

[466] Y. Cao and J. A. A. Qahouq, "Hierarchical soc balancing controller for battery energy storage system", *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9386–9397, 2020.

[467] M. Rasheed, H. Wang, R. Zane, D. Maksimovic, K. Afridi, G. L. Plett, and M. S. Trimboli, "Composite hybrid energy storage system utilizing capacitive coupling for hybrid and electric vehicles", in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, 2021, pp. 939–946.

[468] C. Xiang, Y. Wang, S. Hu, and W. Wang, "A new topology and control strategy for a hybrid battery-ultracapacitor energy storage system", *Energies*, vol. 7, no. 5, pp. 2874–2896, 2014.

[469] A. Styler, G. Podnar, P. Dille, M. Duescher, C. Bartley, and I. Nourbakhsh, "Active management of a heterogeneous energy store for electric vehicles", in *2011 IEEE Forum on Integrated and Sustainable Transportation Systems*, 2011, pp. 20–25. DOI: 10.1109/FISTS.2011.5973650.

[470] X. Han, L. Lu, Y. Zheng, X. Feng, Z. Li, J. Li, and M. Ouyang, "A review on the key issues of the lithium ion battery degradation among the whole life cycle", *ETransportation*, vol. 1, p. 100 005, 2019.

[471] A. Khorsandi, M. Ashourloo, and H. Mokhtari, "An adaptive droop control method for low voltage dc microgrids", in *The 5th Annual International Power Electronics, Drive Systems and Technologies Conference (PEDSTC 2014)*, 2014, pp. 84–89. DOI: 10.1109/PEDSTC.2014.6799349.

[472] T. V. Vu, D. Perkins, F. Diaz, D. E. Gonsoulin, C. S. Edrington, and T. Elmezyani, "Robust adaptive droop control for dc microgrids", *Electric Power Systems Research*, vol. 146, pp. 95–106, 2017.

[473] S.-W. Kim, S.-Y. Choi, and R.-Y. Kim, "A novel droop control method for distribution loss minimization in dc microgrids with decentralized communication", in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 456–463. DOI: 10.1109/ICPE.2015.7167825.

[474] F. Leng, C. M. Tan, and M. Pecht, "Effect of temperature on the aging rate of Li–ion battery operating above room temperature", *Scientific reports*, vol. 5, no. 1, p. 12 967, 2015.

[475] A. Smith, J. C. Burns, X. Zhao, D. Xiong, and J. Dahn, "A high precision coulometry study of the sei growth in li/graphite cells", *Journal of The Electrochemical Society*, vol. 158, no. 5, A447, 2011.

[476] S. Zhang, K. Xu, and T. Jow, "The low temperature performance of Li-ion batteries", *Journal of Power Sources*, vol. 115, no. 1, pp. 137–140, 2003.

[477] Z. Li, J. Huang, B. Y. Liaw, V. Metzler, and J. Zhang, "A review of lithium deposition in lithium-ion and lithium metal secondary batteries", *Journal of power sources*, vol. 254, pp. 168–182, 2014.

[478] M. Petzl, M. Kasper, and M. A. Danzer, "Lithium plating in a commercial lithium-ion battery–A low-temperature aging study", *Journal of power sources*, vol. 275, pp. 799–807, 2015.

[479] Y. Chen, Y. Kang, Y. Zhao, L. Wang, J. Liu, Y. Li, Z. Liang, X. He, X. Li, N. Tavajohi, *et al.*, "A review of lithium-ion battery safety concerns: The issues, strategies, and testing standards", *Journal of Energy Chemistry*, vol. 59, pp. 83–99, 2021.

[480] W. Li, S. Lee, and A. Manthiram, "High-nickel nma: A cobalt-free alternative to nmc and nca cathodes for lithium-ion batteries", *Advanced materials*, vol. 32, no. 33, p. 2 002 718, 2020.

[481] T. Nemeth, P. Schröer, M. Kuipers, and D. U. Sauer, "Lithium titanate oxide battery cells for high-power automotive applications–electro-thermal properties, aging behavior and cost considerations", *Journal of energy storage*, vol. 31, p. 101 656, 2020.

[482] H. Ruan, J. V. Barreras, T. Engstrom, Y. Merla, R. Millar, and B. Wu, "Lithium-ion battery lifetime extension: A review of derating methods", *Journal of Power Sources*, vol. 563, p. 232 805, 2023, ISSN: 0378-7753. DOI: https://doi.org/10.1016/j.jpowsour.2023.232805. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378775323001805.

[483] M. Schimpe, J. V. Barreras, B. Wu, and G. J. Offer, "Battery degradation-aware current derating: An effective method to prolong lifetime and ease thermal management", *Journal of The Electrochemical Society*, vol. 168, no. 6, p. 060 506, 2021.

[484] J. V. Barreras, T. Raj, and D. A. Howey, "Derating strategies for lithium-ion batteries in electric vehicles", in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 4956–4961. DOI: 10.1109/IECON.2018.8592901.

[485] N. Collath, B. Tepe, S. Englberger, A. Jossen, and H. Hesse, "Aging aware operation of lithium-ion battery energy storage systems: A review", *Journal of Energy Storage*, vol. 55, p. 105 634, 2022, ISSN: 2352-152X. DOI: https://doi.org/10.1016/j.est.2022.105634. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2352152X2201622X.

[486] M. Mühlbauer, *Evaluation of power flow control strategies for heterogeneous battery energy storage systems*. Universitaet Bayreuth (Germany), 2022.

[487] LTD EEMB CO., "Li-ion Battery Specification - LIR18650", *Datasheet-Document No. ZJQM-RD-SPC-A12112*, 2017.

[488] Y. Mazzi, H. Ben Sassi, A. Gaga, and F. Errahimi, "State of charge estimation of an electric vehicle's battery using tiny neural network embedded on small microcontroller units", *International Journal of Energy Research*, vol. 46, no. 6, pp. 8102–8119, 2022.

[489] G. Crocioni, D. Pau, J.-M. Delorme, and G. Gruosso, "Li-ion batteries parameter estimation with tiny neural networks embedded on intelligent iot microcontrollers", *IEEE Access*, vol. 8, pp. 122 135–122 146, 2020.

[490] M. Rusli, U. Wibawa, R. N. Hasanah, and A. Zainuri, "Parameter estimation of li-polymer battery using non-linear feedback structure aproximation", in *2022 11th Electrical Power, Electronics, Communications, Controls and Informatics Seminar (EECCIS)*, IEEE, 2022, pp. 264–269.

[491] S. Harippriya, E. E. Vigneswaran, and S. Jayanthy, "Battery management system to estimate battery aging using deep learning and machine learning algorithms", in *Journal of Physics: Conference Series*, IOP Publishing, vol. 2325, 2022, p. 012 004.

[492] M. Baumann, C. Weissinger, and H.-G. Herzog, "System identification and modeling of an automotive bidirectional dc/dc converter", in *2019 IEEE Vehicle Power and Propulsion Conference (VPPC)*, IEEE, 2019, pp. 1–5.

[493] F. J. G. Navarro, L. J. Yebra, F. J. G. Medina, and A. Giménez-Fernandez, "Dc-dc linearized converter model for faster simulation of lightweight urban electric vehicles", *IEEE Access*, vol. 8, pp. 85 380–85 394, 2020.

[494] K. Spiliotis, J. E. Gonçalves, W. Van De Sande, S. Ravyts, M. Daenen, D. Saelens, K. Baert, and J. Driesen, "Modeling and validation of a dc/dc power converter for building energy simulations: Application to bipv systems", *Applied energy*, vol. 240, pp. 646–665, 2019.

[495] M. Winter, S. Moser, S. Schoenewolf, J. Taube, and H.-G. Herzog, "Average model of a synchronous half-bridge dc/dc converter considering losses and dynamics", in *Proceedings of the 11th International Modelica Conference, Versailles, France, September 21-23, 2015*, Linköping University Electronic Press, 2015, pp. 479–484.

[496] G. Laera, L. Vanfretti, K. Thomas, and M. Gardner, "Object oriented modeling and control design for power electronics half-bridge converter using modelica", 2020.

[497] M. A. Alharbi, M. Dahidah, S. Ali, S. Ethni, and V. Pickert, "Current ripple minimisation based on phase-shedding of dc-dc interleaved converters for ev charging system", in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 3456–3462. DOI: 10.1109/IECON.2019.8926959.

[498] M. Schuck and R. C. N. Pilawa-Podgurski, "Ripple minimization in asymmetric multiphase interleaved dc-dc switching converters", in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 133–139. DOI: 10.1109/ECCE.2013.6646691.

[499] Texas Instruments Incorporated, *LM5170-Q1 EVM User Guide*, Texas Instruments Incorporated, Ed., 2016. [Online]. Available: %5Curl%7Bhttps://www.ti.com/tool/LM5170EVM-BIDIR%7D.

[500] Texas Instruments Incorporated, *LM5170-Q1 Multiphase Bidirectional Current Controller*, Texas Instruments Incorporated, Ed., 2016. [Online]. Available: %5Curl%7Bhttps://www.ti.com/product/LM5170-Q1?qgpn=lm5170-q1%7D.

[501] A. Reindl, F. Lausser, L. Eriksson, S. Park, M. Niemetz, and H. Meier, "Mathematical Modeling of a Bidirectional DC-DC Converter - Part 1: Buck Mode", *AE 2022: 27th International Conference on Applied Electronics (IEEE), Pilzen, Czech Republic*, 2023 - under review.

[502] A. Reindl, F. Lausser, L. Eriksson, S. Park, M. Niemetz, and H. Meier, "Mathematical Modeling of a Bidirectional DC-DC Converter - Part 2: Boost Mode", *AE 2022: 27th International Conference on Applied Electronics (IEEE), Pilzen, Czech Republic*, 2023 - under review.

[503] E. Surewaard, E. Karden, and M. Tiller, "Advanced electric storage system modeling in modelica", *Paper presented at the 3rd International Modelica Conference*, 2003.

[504] M. A. Hannan, M. M. Hoque, A. Hussain, Y. Yusof, and P. J. Ker, "State-of-the-art and energy management system of lithium-ion batteries in electric vehicle applications: Issues and recommendations", *IEEE Access*, vol. 6, pp. 19 362–19 378, 2018. DOI: 10.1109/ACCESS.2018.2817655.

[505] J.-M. Timmermans, J. Van Mierlo, P. Lataire, F. Van Mulders, and Z. McCaffree, "Test platform for hybrid electric power systems: Development of a hil test platform", in *2007 European Conference on Power Electronics and Applications*, IEEE, 2007, pp. 1–7.

[506] L. Mihet-Popa and V. Groza, "Battery management system test platform developed for electric vehicle applications", in *2015 IEEE 9th International Symposium on Intelligent Signal Processing (WISP) Proceedings*, IEEE, 2015, pp. 1–6.

[507] Y. Li, Z. Sun, and J. Wang, "Design for battery management system hardware-in-loop test platform", in *2009 9th International Conference on Electronic Measurement & Instruments*, IEEE, 2009, pp. 3–399.

[508] S. Jakubek, E. Luchini, A. Oberhummer, and F. Pfister, "A model-based interfacing concept for accurate power hardware-in-the-loop systems", *Mathematical and Computer Modelling of Dynamical Systems*, vol. 22, no. 1, pp. 1–20, 2016.

[509] S. Maxwell, S. R. Islam, M. K. Hossain, and S.-Y. Park, "Capability, compatibility, and usability evaluation of hardware-in-the-loop platforms for dc-dc converter", in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, 2016, pp. 1–6.

[510] R. Subramanian, P. Venhovens, and B. P. Keane, "Accelerated design and optimization of battery management systems using hil simulation and rapid control prototyping", in *2012 IEEE International Electric Vehicle Conference*, IEEE, 2012, pp. 1–5.

[511] S. Chakraborty, M. Mazuela, D.-D. Tran, J. A. Corea-Araujo, Y. Lan, A. A. Loiti, P. Garmier, I. Aizpuru, and O. Hegazy, "Scalable modeling approach and robust hardware-in-the-loop testing of an optimized interleaved bidirectional hv dc/dc converter for electric vehicle drivetrains", *IEEE Access*, vol. 8, pp. 115 515–115 536, 2020.

[512] J. V. Barreras, M. Swierczynski, E. Schaltz, S. J. Andreasen, C. Fleischer, D. U. Sauer, and A. E. Christensen, "Functional analysis of battery management systems using multi-cell hil simulator", in *2015 Tenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, IEEE, 2015, pp. 1–10.

[513] B. Tabbache, Y. Aboub, K. Marouani, A. Kheloui, and M. Benbouzid, "A simple and effective hardware-in-the-loop simulation platform for urban electric vehicles", in *2012 First International Conference on Renewable Energies and Vehicular Technology*, IEEE, 2012, pp. 251–255.

[514] W. C. Lee and D. Drury, "Development of a hardware-in-the-loop simulation system for testing cell balancing circuits", *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5949–5959, 2013.

[515] IXXAT, *CAN-USB Adapter*, `https://www.ixxat.com`.

[516] IEEE, *Standard Digital Interface for Programmable Instrumentation*, IEEE Std 488.2-1992.

[517] Python, *pySerial 3.0*, `https://pythonhosted.org/pyserial/pyserial.html`.

[518] Python, *python-can 3.3.2*, https://python-can.readthedocs.io/en/master/.

[519] Python, *matplotlib 3.3.0*, https://matplotlib.org/Matplotlib.pdf.

[520] MingHe, *D3806: Buck and Boost Modul*, Datasheet.

[521] GW Instek, *Multi-Output Programmable DC Power Supply GPP-2323 datasheet*, https://www.calplus.de/gw-instek-gpp-2323.html.

[522] Joy-it, *DPS 5015 - Programmable Power Supply, Step Down Converter*, Datasheet.

[523] Texas Instruments, *LM3150 Wide-VIN Synchronous Buck Controller*, Datasheet, 2015.

[524] JOY-IT, *DPS5015 Programmable Power Supply*, https://joy-it.net/files/files/Produkte/JT-DPS5015/JT-DPS5015-Anleitung.pdf, Datasheet.

[525] G. Liu, "Dps5015 cnc power communication protocol v1.2", 2018.

[526] Texas Instruments, *TS5A3154 – ANALOG SWITCH*, Datasheet, 2012.

[527] Texas Instruments, *INA228 – 85-V, 20-Bit, Ultra-Precise Power/Energy/Charge Monitor With I^2C Interface*, Datasheet, 2022.

[528] STMicroelectronics, *An5346 - STM32G4 ADC use tips and recommendations*, Application Note, 2019.

[529] STMicroelectronics, *ADC120, 8-channel, 50 ksps to 1 Msps, 12-bit A/D converter*, Datasheet, 2019.

[530] STMicroelectronics, *STM32G474 Arm Cortex-M4 32-bit MCU+FPU, 170 MHz/213 DMIPS, 128 KB SRAM, rich analog, math acc, 184 ps 12 chan Hi-res timer*, Datasheet, 2021.

[531] A. Reindl, T. Langer, H. Meier, and M. Niemetz, "Comparative reliability analysis for single and dual can (fd) systems", in *2022 International Conference on Applied Electronics (AE)*, 2022, pp. 1–6. DOI: 10.1109/AE54730.2022.9920078.

[532] Texas Instruments, *INA226 – High-or Low-Side Measurement, Bi-Directional CURRENT/POWER MONITOR with I^2C Interface*, Datasheet, 2011.

[533] ZETTLER electronics GmbH, *AZ733 DPDT MINIATURE POWER RELAY*, Datasheet, 2010.

[534] Texas Instruments, *ULN200x, ULQ200x High-Voltage, High-Current Darlington Transistor Arrays*, Datasheet, 2019.

[535] Micro Crystals Switzerland, *Application Manual RC-3129-C3 DTCXO Temperature Compensated Real Time Clock/Calendar Module with I^2C Interface*, Application Manual, 2019.

[536] Texas Instruments, *TCAN33x 3.3-VCANTransceivers with CAN FD (Flexible Data Rate)*, Datasheet, 2019.

[537] TRACO Power, *TEC-3 Series 3W DC/DC Converter*, Datasheet, 2022.

[538] Anderson Power, *ASMPR45 Powerpole Connectors - PP15 to PP45*, Datasheet, 2018.

[539] P. Semiconductors, "74HC245; 74HCT245 Octal bus tranceiver; 3-state", en, vol. 2005, p. 23, [Online]. Available: https://www.mouser.com/datasheet/2/302/nxp_74hc_hct245-547458.pdf.

[540] *Iso772x high-speed, robust emc, reinforced and basic dual-channel digital isolators*, en. [Online]. Available: https://www.ti.com/lit/ds/symlink/iso7721.pdf?ts=1628483826520&ref_url=https%253A%252F%252Fwww.ti.com%252Fisolation%252Fproducts.html (visited on 08/09/2021).

[541] *Tpd2e001 low-capacitance 2-channel esd-protection for high-speed data interfaces*, en. [Online]. Available: https://www.ti.com/lit/ds/symlink/tpd2e001.pdf?ts=1628496767820&ref_url=https%253A%252F%252Fwww.google.com%252F (visited on 08/09/2021).

[542] *Ws2812b intelligent control led integrated light source*, en. [Online]. Available: https://cdn-shop.adafruit.com/datasheets/WS2812B.pdf (visited on 08/09/2021).

[543] *Voltage regulator tle 4274 / 3.3v;2.5v*, en. [Online]. Available: https://www.infineon.com/dgdl/Infineon-TLE4274V33-DS-v02_30-EN.pdf?fileId=5546d46258fc0bc101595f8e72d51f99 (visited on 08/09/2021).

[544] *Ultra-low-power arm® cortex®-m4 32-bit mcu+fpu, 100dmips, up to 256kb flash, 64kb sram, usb fs, lcd, ext. smps*, en. [Online]. Available: https://www.st.com/content/ccc/resource/technical/document/datasheet/f7/a0/fc/27/24/4e/4f/3f/DM00257192.pdf/files/DM00257192.pdf/jcr:content/translations/en.DM00257192.pdf (visited on 08/09/2021).

[545] *The battery passport content guidance*, 2023. [Online]. Available: https://thebatterypass.eu/resources/.

A

Appendix A

A.1 Controller Analysis of the Buck Mode

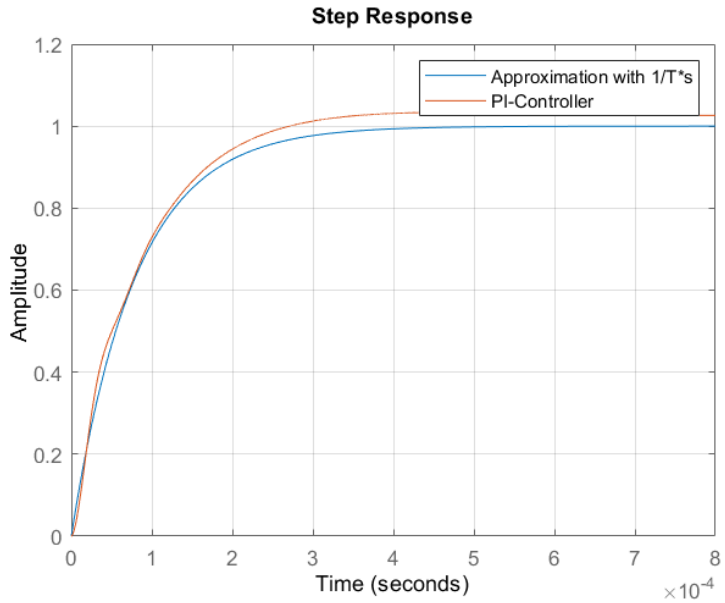


Figure A.1: Step response in buck mode and CCM with a load resistance of $R_l = 2\,\Omega$.

A.2 Controller Analysis of the Boost Mode

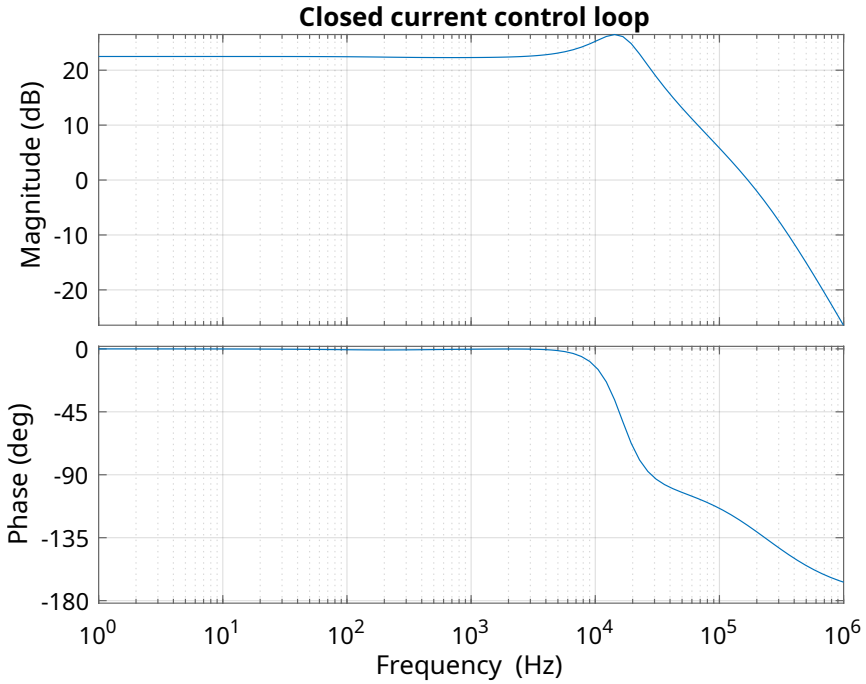


Figure A.2: Closed current control loop in buck mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. Up to a frequency of 3 kHz the gain is approximately constant and is $G_0 = 22\,dB$. At a frequency of $f_\mathrm{p} = 14.5\,kHz$ there is a conjugate complex pole with an increase of $4.5\,dB$ over G_0 (total $26.5\,dB$) and a subsequent magnitude decrease of $-40\frac{dB}{dec}$. The phase change results in $-180\frac{^\circ}{dec}$. A zero at a frequency of $f_\mathrm{z} = 2.8\,kHz$ attenuates the decay of the gain to $-20\frac{dB}{dec}$ and causes a phase change of $+90^\circ$ and a resulting decay of the phase of $-90\frac{^\circ}{dec}$. The crossover frequency is $f_\mathrm{c} = 170\,kHz$. The phase and magnitude reserve are satisfactory for stability. For the position of the poles and zeros, a comparison with the Bode diagrams of the duty cycle to current transfer function $G_\mathrm{id}(s)$ in figure 7.7 on p.117 is helpful.

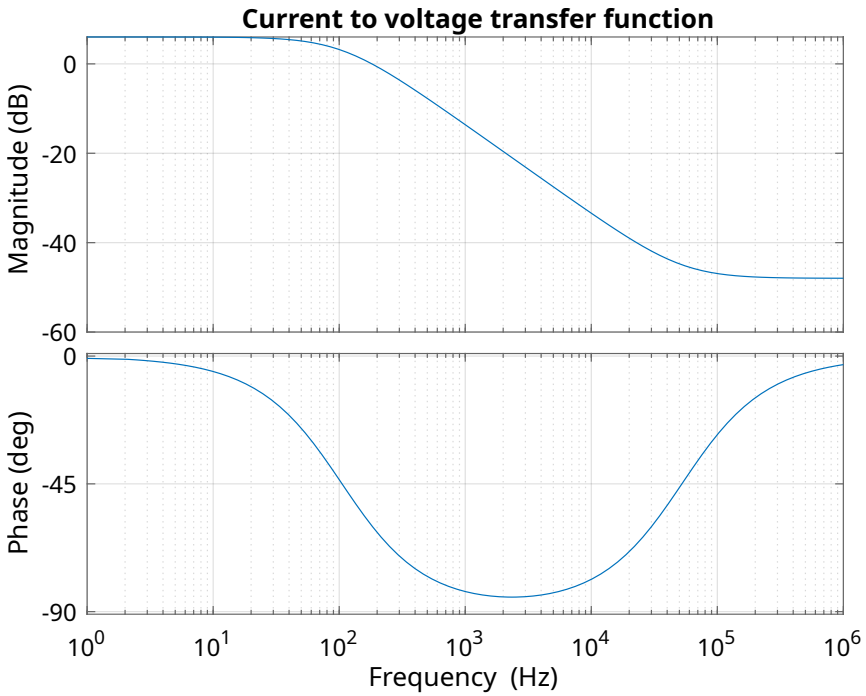


Figure A.3: Output current to output voltage transfer function $G_{\mathrm{vi}}(s)$ in buck mode and CCM with a load resistance of $R_{\mathrm{l}} = 2\,\Omega$. Up to a frequency of $50\,Hz$, the gain is approximately constant and is $G_0 = 22\,dB$. At a frequency $f_p = 20\,Hz$ a pole position occurs and consequently a decrease in the magnitude $-20\frac{dB}{dec}$ of and a phase change of $-90\frac{^\circ}{dec}$. At a frequency of $f_z = 400\,Hz$ and $f_z = 10\,kHz$, a zero occurs respectively with a magnitude change of $+20\frac{dB}{dec}$and a phase change of $+90\frac{^\circ}{dec}$. The crossover frequency is $f_{\mathrm{c}} = 181\,Hz$. For the position of the poles and zeros, Bode plots of the calculated transfer function of the output current to the output voltage $G_{\mathrm{vi}}(s)$ in figure 7.9 on p.119 are helpful.

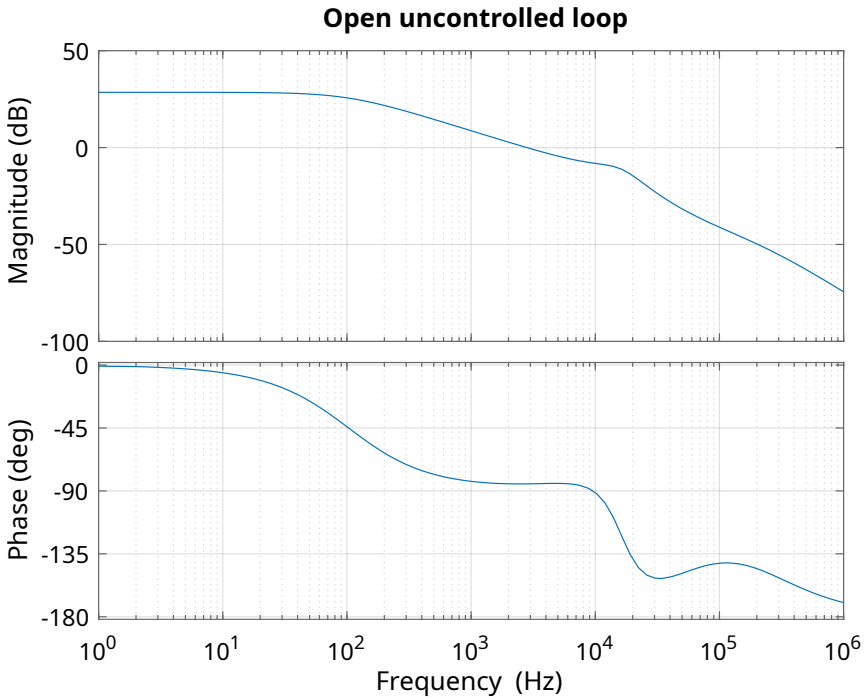


Figure A.4: Open uncontrolled control loop in buck mode and CCM with a load resistance of $R_l = 2\,\Omega$.

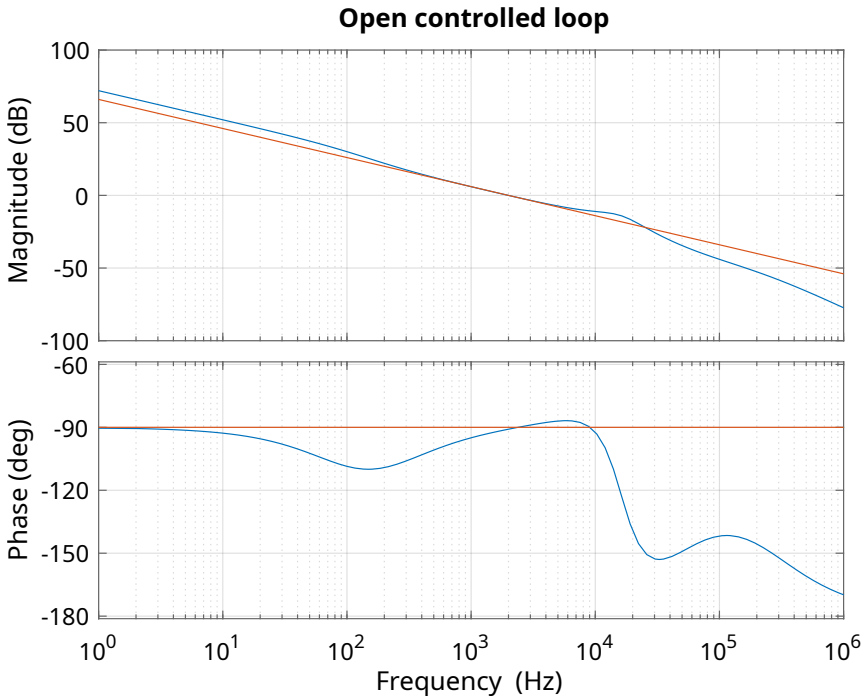


Figure A.5: The open controlled control loop in buck mode and CCM with a load resistance of $R_l = 2\,\Omega$ approximately exhibits the behavior of an I-compensator. The crossover frequency is $f_c = 2\,kHz$.

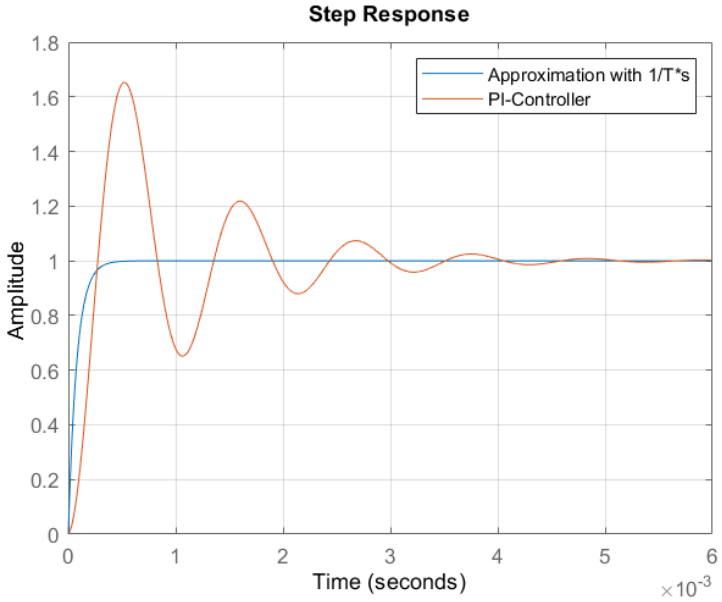


Figure A.6: Step response in buck mode and DCM with a load resistance of $R_\mathrm{l} = 1\,k\Omega$.

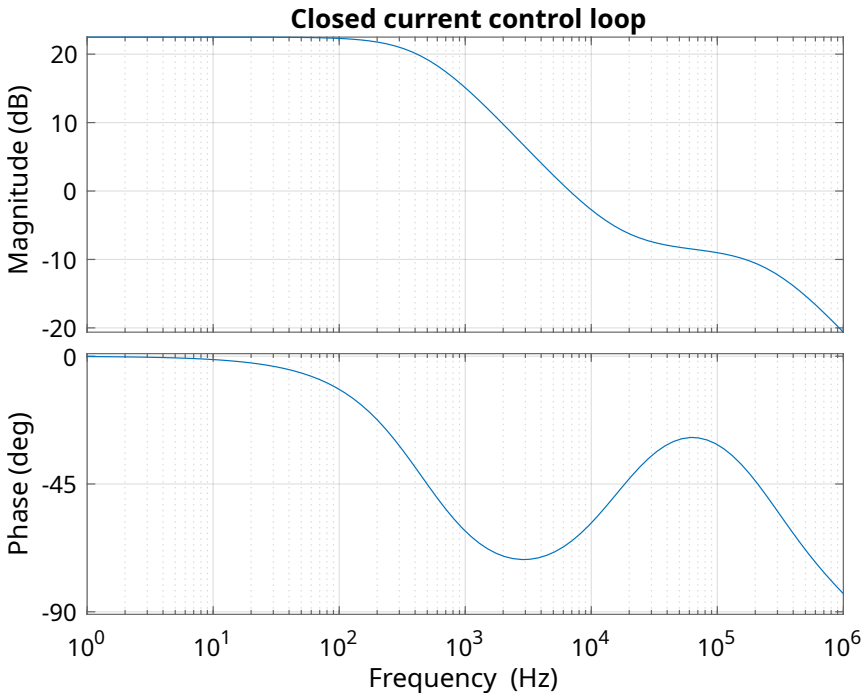


Figure A.7: Closed current control loop in buck mode and DCM with a load resistance of $R_\mathrm{l} = 1\,k\Omega$. Up to a frequency of $200\,Hz$ the gain is approximately constant and equals $G_0 = 22.4\,dB$. At a frequency $f_p = 100\,Hz$ a pole position occurs followed by a magnitude decrease of $-20\frac{dB}{dec}$ of and a phase change of $-90\frac{^\circ}{dec}$. Two zeros occur at a frequency of $f_z = 2\,kHz$ and $f_z = 5\,kHz$ respectively causing a magnitude change of $+20\frac{dB}{dec}$ and a phase change of $+90\frac{^\circ}{dec}$. Consequently, two pole positions occur in the frequency range between $f_p = 50\,kHz$ and $f_p = 100\,kHz$. The crossover frequency is $f_\mathrm{c} = 6.75\,kHz$. For the position of the poles and zeros, Bode plots of the calculated duty cycle to current $G_\mathrm{id}(s)$ in figure 7.12 on p.121 are helpful.

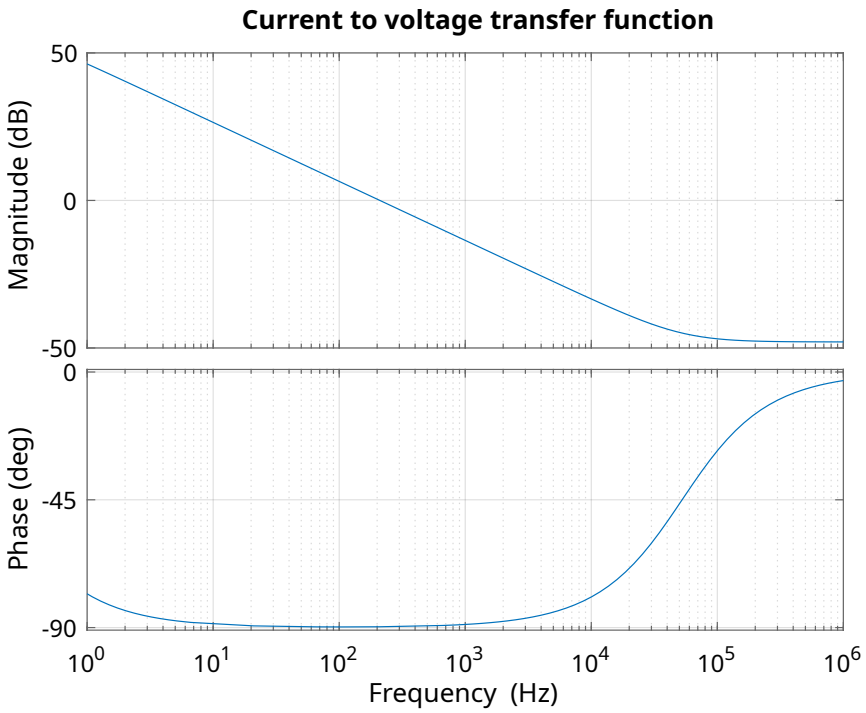


Figure A.8: Output current to output voltage transfer function $G_{\mathrm{vi}}(s)$ in buck mode and DCM with a load resistance of $R_{\mathrm{l}} = 1\,k\Omega$. Up to a frequency of $1\,kHz$, the gain decreases with $-20\frac{dB}{dec}$. The phase is approximately constant at $-90\circ$. The pole responsible for this occurs at very low frequencies and is not recognizable within the bode plot. At a frequency of $f_z = 2\,kHz$ a zero occurs and causes a magnitude change of $+20\frac{dB}{dec}$ and a phase change of $+90\frac{^\circ}{dec}$. The crossover frequency is $f_{\mathrm{c}} = 210\,Hz$. For the position of the poles and zeros, Bode plots of the calculated transfer function of the output current to the output voltage $G_{\mathrm{vi}}(s)$ in figure 7.9 on p.119 are helpful.

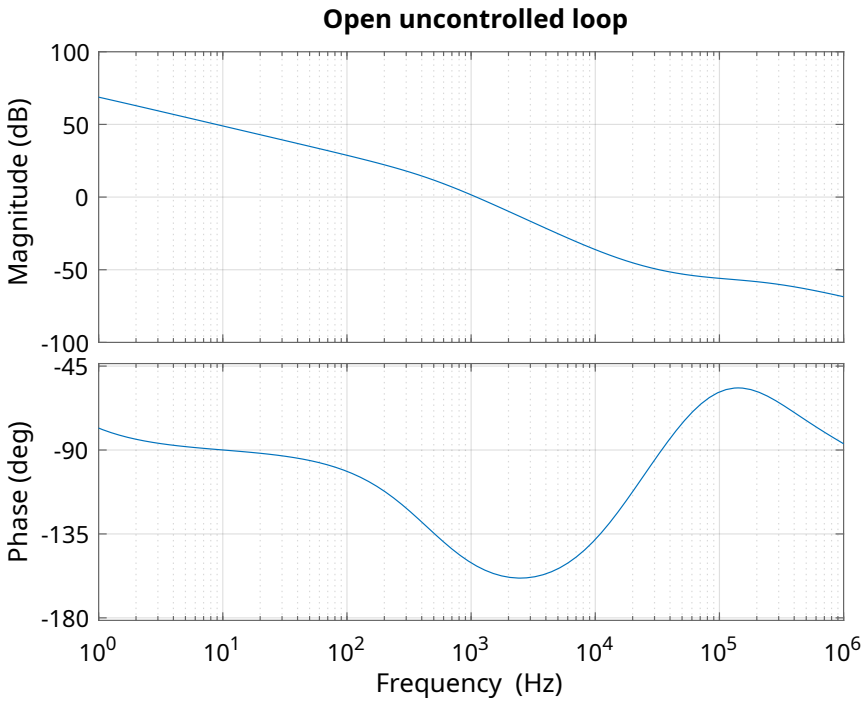


Figure A.9: Open uncontrolled control loop in buck mode and DCM with a load resistance of $R_{\mathrm{l}} = 1\,k\Omega$.

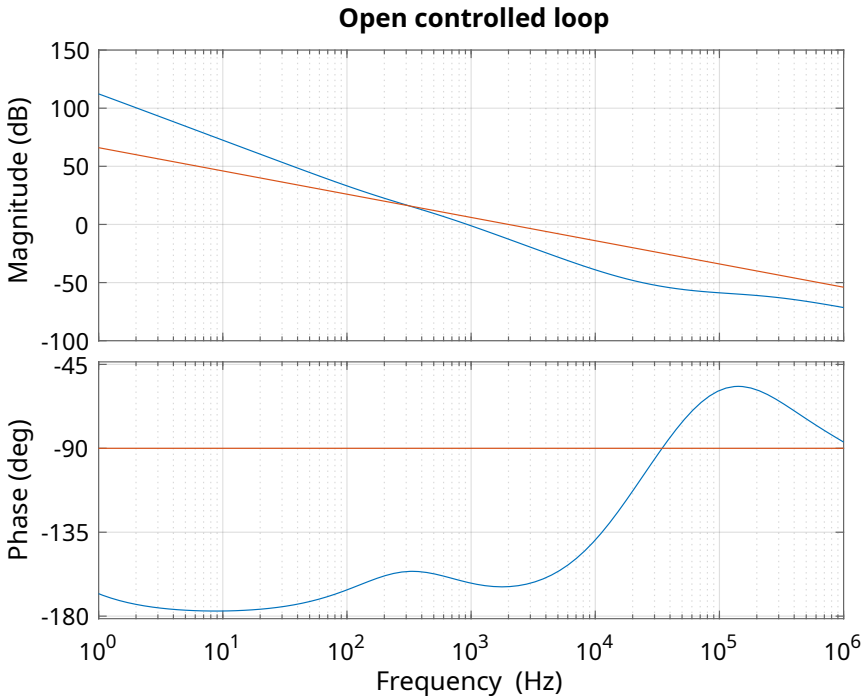


Figure A.10: Open uncontrolled control loop in buck mode and DCM with a load resistance of $R_l = 1\,k\Omega$. The orange line shows the approximation. It shows approximately the behavior of an I-compensator. The crossover frequency is $f_c \approx 1\,kHz$.

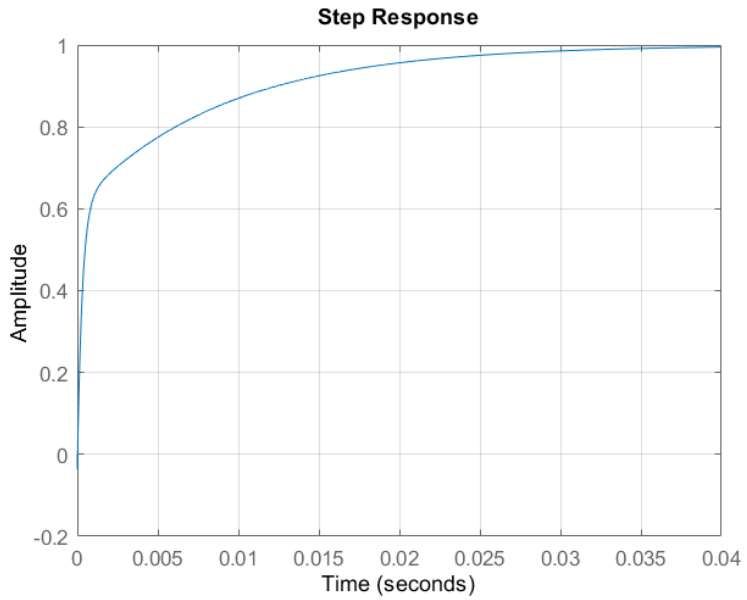


Figure A.11: Step response in boost mode and CCM with a load resistance of $R_l = 2\,\Omega$.

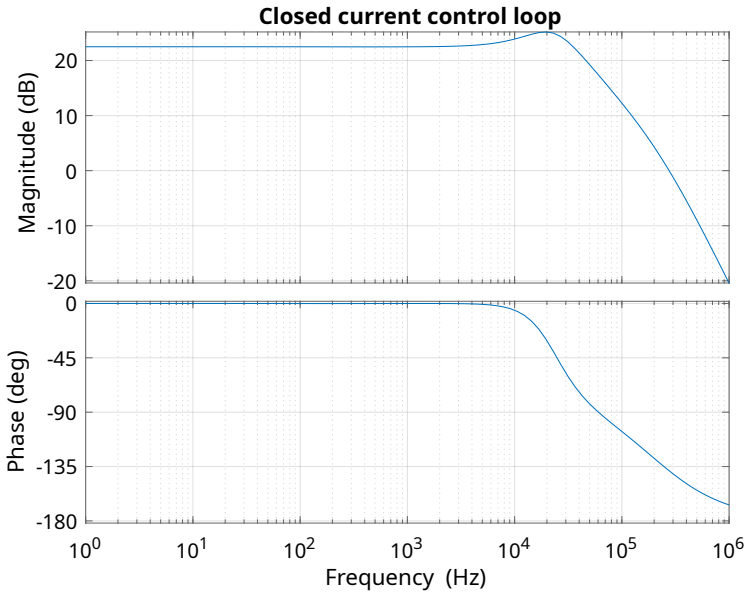


Figure A.12: Closed current control loop in boost mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. Up to a frequency of $5\,kHz$ the gain is approximately constant and equal to $G_0 = 22.5\,dB$. The phase is constantly $0°$ within that frequency range. At a frequency of approximately $f_\mathrm{p} = 20\,kHz$ a pole occurs and leads to a change in the magnitude and phase response. The magnitude decreases with $-20\frac{dB}{dec}$ and the phase with $-90\frac{°}{dec}$. The crossover frequency is $f_\mathrm{c} = 278\,kHz$. For the position of the poles and zeros, Bode plots of the calculated duty cycle to current transfer functions $G_\mathrm{id}(s)$ in figure 7.16 on p.126 are helpful.

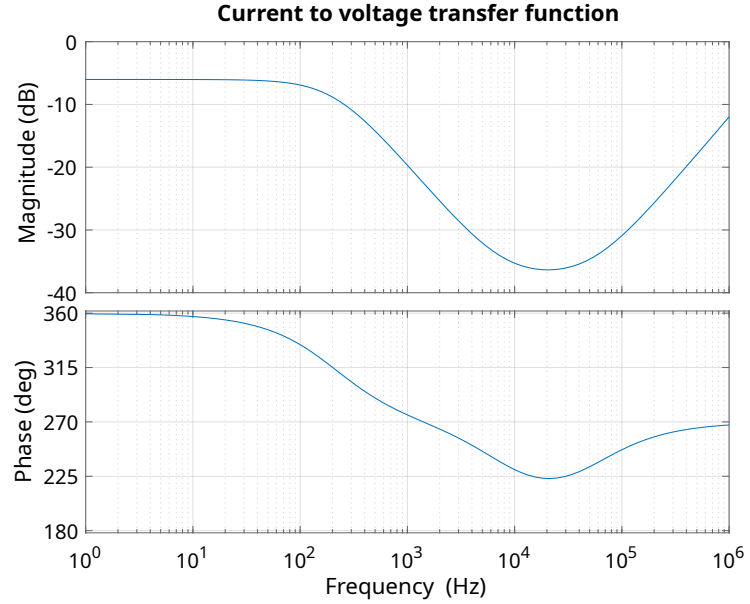


Figure A.13: Output current to output voltage transfer function $G_\mathrm{vi}(s)$ in boost mode and CCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$. For the position of the pole and zeros, Bode plots of the calculated transfer function of the output current to the output voltage $G_\mathrm{vi}(s)$ in figure 7.17 on p.128 are helpful.

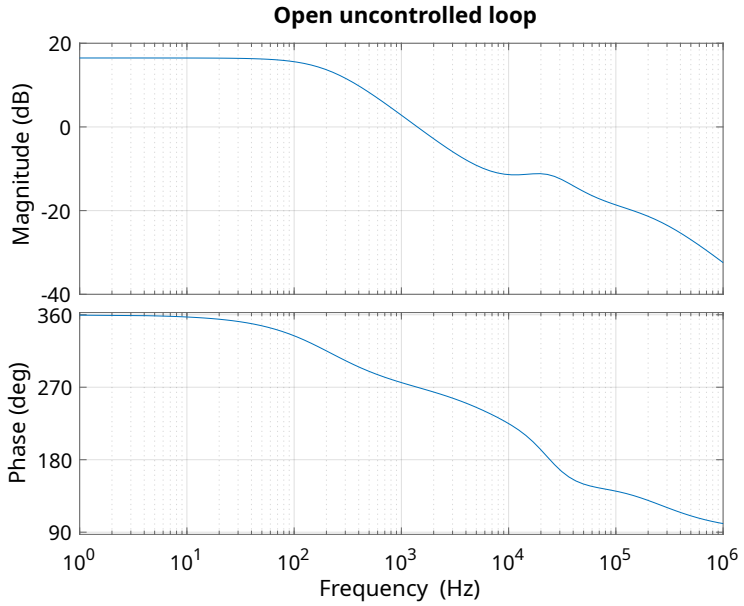


Figure A.14: Open uncontrolled control loop in boost mode and DCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$.

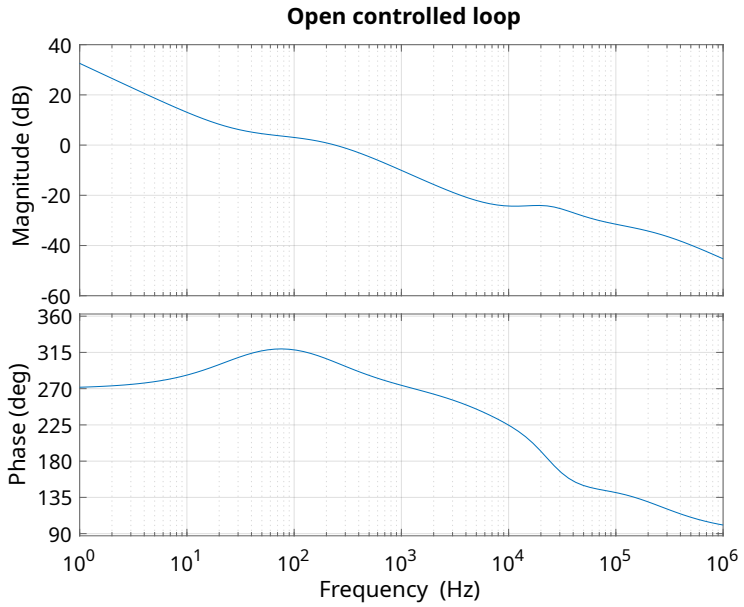


Figure A.15: Open controlled control loop in boost mode and DCM with a load resistance of $R_\mathrm{l} = 2\,\Omega$.

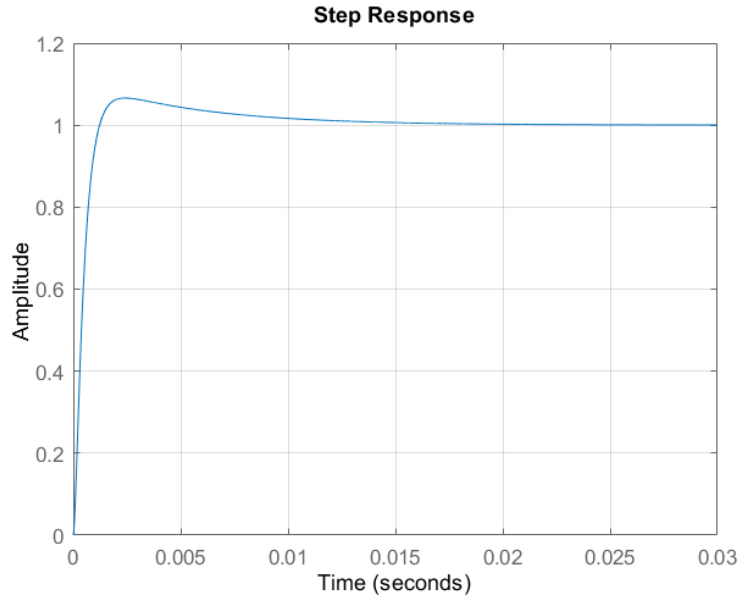


Figure A.16: Step response in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$.

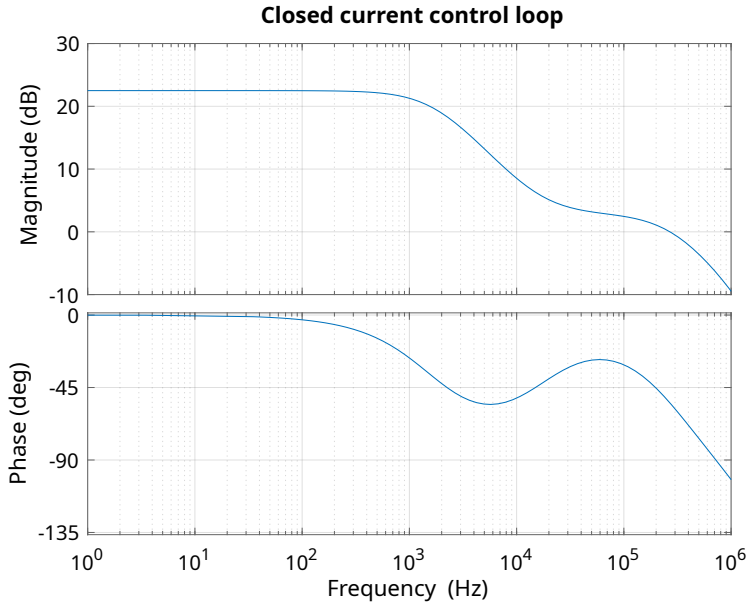


Figure A.17: Closed current control loop in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$. For the position of the poles and zeros, Bode plots of the calculated duty cycle to current transfer functions $G_{id}(s)$ in figure 7.20 on p.130 are helpful.

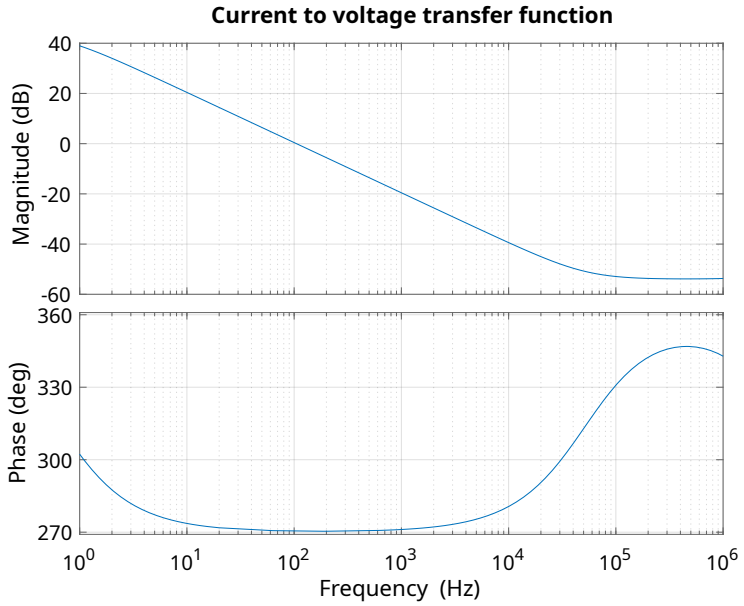


Figure A.18: Output current to output voltage transfer function $G_{\mathrm{vi}}(s)$ in boost mode and DCM with a load resistance of $R_{\mathrm{l}} = 1\,k\Omega$.

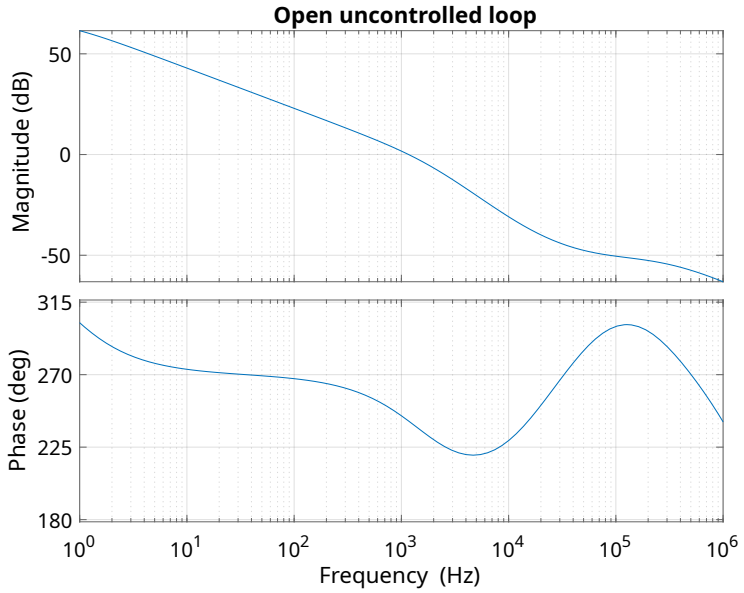


Figure A.19: Open uncontrolled control loop in boost mode and DCM with a load resistance of $R_{\mathrm{l}} = 1\,k\Omega$.

,

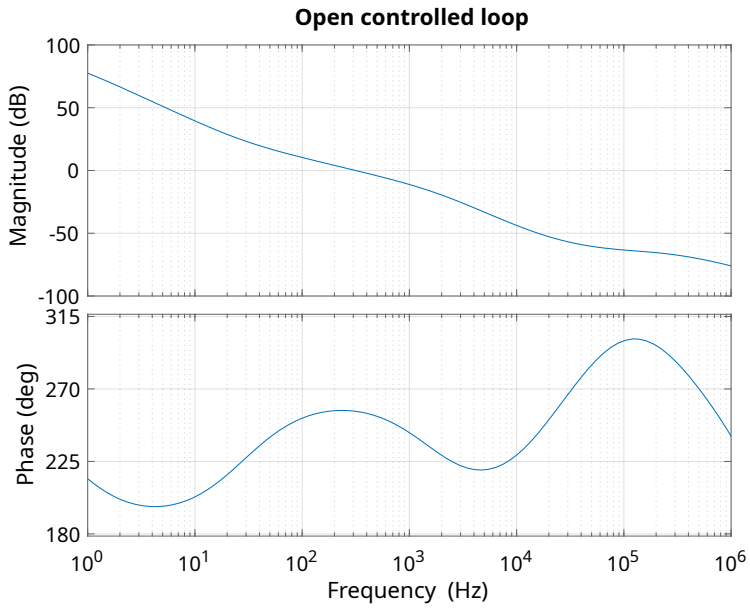


Figure A.20: Open controlled control loop in boost mode and DCM with a load resistance of $R_l = 1\,k\Omega$.