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Abschlussarbeit zum Thema

Design and Test of High Speed, Low Noise, High Resolution Frontend Electronics for a Microbolometer Array

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Abstract

In this thesis, frontend electronics for operating a microbolometer sensor are developed. This sensor consists of resistive microbolometers that act as a radiation camera and are sensitive to the wavelength range of $8 - 14\ \mu m$. The sensor's requirements for supply voltages, bias voltages, and clock signals are identified and met through suitable circuits. For the video signals, a signal path is designed to convert the signals into balanced, differential signals that can be interpreted by an analog-to-digital converter. Subsequently, two printed circuit boards are developed and manufactured for the design. The boards are assembled and commissioned. Tests conducted afterward reveal that the designs are functional. The resulting interferences are very low; however, there are influences whose origin cannot be localized. The sensor's supply voltage is low-noise, except for a disturbance at 94 kHz. A functional LVDS path has been developed, capable of transmitting clock signals.

Zusammenfassung

In dieser Abschlussarbeit wird eine Frontend Elektronik zur Betreibung eines Mikrobolometer Sensors entwickelt. Dieser Sensor besteht aus resistiven Mikrobolometern, welche als Strahlungskamera agieren und für den Wellenlängenbereich von $8 - 14\ \mu m$ empfindlich sind. Die Anforderungen des Sensors an Versorgungs- und Biasspannungen sowie an Clock-Signale werden heraus gearbeitet und durch geeignete Schaltungen erfüllt. Für die Video Signale wird eine Signalstrecke entworfen, welche die Signale in balancierte, differentielle Signale umwandelt, die von einem Analog-zu-Digital Konverter ausgewertet werden können. Für das elektronische Design werden im Anschluss zwei Platinen entwickelt und gefertigt. Die Platinen werden bestückt und in Betrieb genommen. Aus den anschließend durchgeführten Tests geht hervor, dass die Designs funktional sind. Die sich ergebenden Störungen sind sehr gering, es bleiben jedoch Einflüsse, deren Ursprung nicht lokalisiert werden konnte. Die Versorgungsspannung des Sensors ist rauscharm, mit der Ausnahme einer Störung bei 94 kHz. Es wurde eine funktionierende LVDS-Strecke entwickelt, die die getakteten Clock-Signale übertragen kann.

Danksagung

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Abschließend bedanke ich mich bei Alexander Fitzner für die motivierenden und beruhigenden Worte.

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Acronyms

ADC Analog-to-Digital Converter. 7

DAC Digital-to-Analog Converter. 5

DLR Deutsches Zentrum für Luft- und Raumfahrt. 1

EMI Electromagnetic Interference. 28

FDA Fully Differential Amplifier. 18

FPA Focal Plane Assembly. 1

FPGA Field Programmable Gate Array. 3

IC Integrated Circuit. 4

JTAG Joint Test Action Group. 26

LDO Low-Dropout-Regulator. 13

LVDS Low-Voltage Differential Signaling. 10

NASA National Aeronautics and Space Administration. 1

op amp Operational Amplifier. 10

PCB Printed Circuit Board. 1

PEU Proximity Electronics Unit. 1

PSD Power Spectral Density. 64

PSRR Power Supply Rejection Ratio. 13

SPI Serial Peripheral Interface. 15

1 Introduction

A bolometer is a sensor that uses infrared radiation to generate a signal. This radiation changes the temperature of a sensitive area and therefore provides a signal that can be converted to a video signal. An array of smaller bolometers can be constructed as a camera with a single microbolometer per pixel. As microbolometers are only sensitive in the long wavelength infrared region of $8 - 14\mu m$ and not in the visible spectrum of light, they generate information on the temperature. They are ideally suited to pick up small temperature differences and have therefore wide ranges of applications such as in firefighting, security, and surveillance [13]. Microbolometer cameras are not a new concept in space applications. First tests with microbolometers were made by NASA as early as 1997 [18]. Since then, microbolometers have gained in significance, as production possibilities improved and better detectors could be developed [21].

For future missions engineers at the German Aerospace Centre (DLR) are evaluating different sensors for their functionality and practical applicability. One of these detectors is the PICO1024™ by Lynred. This is an integrated system that provides analog output signals. [2] Frontend electronics are needed to supply the detector with clock signals, power supplies, and other configuration data.

Throughout this thesis, a design for these frontend electronics will be created that will comply with the detector's requirements. This design will then be tested for its compatibility with the detector. Most instruments at DLR are divided into two main assemblies. The Sensor itself is positioned on a Focal Plane Assembly or short FPA. This is a smaller building block that can easily be mounted in a housing or positioned for best use with additional optics. The main electronics are situated in the Proximity Electronics Unit or short PEU. This means, that two printed circuit boards (PCB) will be designed, manufactured, and tested.

1.1 Theory

The basic principle for a bolometer infrared sensor is shown in figure 1.1. The incoming radiation is collected by an absorber which heats up. The absorber's temperature is measured and a corresponding signal is generated by the read-out circuit. Thermal insulation protects the read-out circuit from experiencing signal deviations due to its increase in temperature [2][13].

There are different versions of microbolometers, but most are resistive bolometers. The temperature difference changes a resistor value. These resistors can be placed in a tight array. Typically those have pitches between $12\mu m$ and $25\mu m$ with pitch meaning the distance between two pixel centers. Figure 1.2 shows the basic structure of a microbolometer pixel. It consists of an absorbing membrane with a temperature-sensitive resistor and the readout circuit in the substrate

below. Insulation is further enhanced by using narrow bridges to connect the different parts [2][13][8].

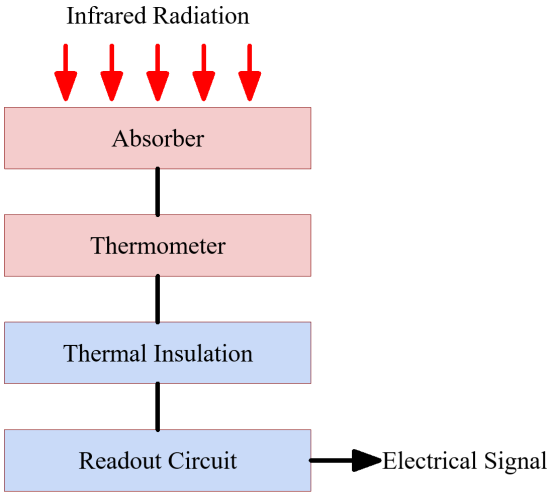


Figure 1.1: Bolometer Sensor Principle - *The incoming radiation heats an insulated absorber. In the detector's readout integrated circuit (ROIC) its temperature change is then converted into an electrical signal.*

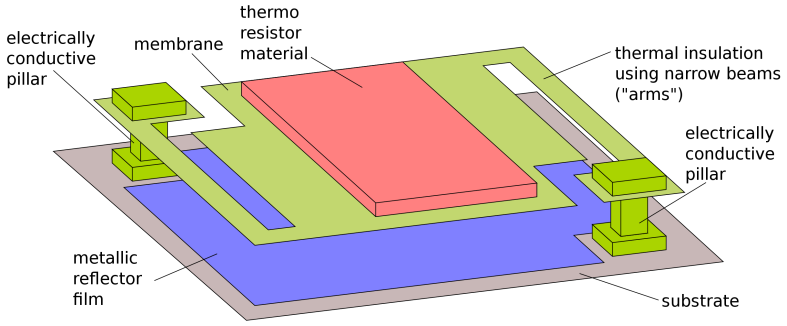


Figure 1.2: Microbolometer Pixel [9] - *Most microbolometer arrays consist of multiple pixels of monolithic silicium structures.*

1.2 Scope of this Thesis

The goal of this thesis is to create an electronics design for the frontend electronics of this specific microbolometer sensor. The requirements for these circuits are therefore directly derived from the specifications of the PICO1024™. The design consists of a schematic and the corresponding layout. This design is to be manufactured and the components fitted for further testing. The main goal of these tests is to evaluate the applicability of the sensor and to determine, whether this design can accommodate this microbolometer sensor. Testing will include:

- the noise of the supply voltages generated for the sensor
- the transfer behavior for the signal voltages
- the performance of filtering and converting
- the power-up sequencing
- evaluation of high-speed control signals

This design will include a field programmable gate array (FPGA) to generate the required clock and control sequences. Synthesizing the FPGA is not in the scope of this thesis. Therefore, tests are conducted without the main functionality of the FPGA. The results will still be relevant as a lot of the detector's performance will be reliant on the overall PCB design and the FPGA's system clock will still be operational.

This design is only intended for use on Earth. Therefore the used components will not be space grade. Wherever possible, commercial of the shelf components will be used.

2 Design

The PICO1024™ is the microbolometer detector that is to be implemented. Before its performance can be evaluated, frontend electronics need to be designed. These should provide the sensor with all of the required bias, supply, clock, and control signals while also interpreting its video signals.

2.1 Detector Description

The PICO1024™ is a microbolometer sensor with 1024×768 pixels. These pixels are arranged with a pitch of $17\mu m$ and are sensitive to radiation with wavelengths of $8\mu m - 14\mu m$. The pixels are read out with a rolling shutter. The output signal can be configured to two or four data lines. Four outputs are needed to achieve frame rates of up to $120Hz$ with full resolution. The output signals are analog signals with a dynamic range from $0.5V$ to $2.9V$. The frequencies depend on the configuration. Three clock signals are used: the masterclock MC, the integration clock INT, and a RESET signal for frame synchronization. The maximum usable frequency is $25MHz$ [2].

The main supply voltage is $3.6V$ but the integrated circuit (IC) needs several additional voltages during operation. All these voltages must be low noise to ensure proper operation. The PICO1024™ provides its temperature at an additional output. This analog signal is to be used for error and offset correction of the video signal.

2.1.1 Requirements

To achieve the best possible performance, precise requirements need to be formulated. These all derive from the microbolometer datasheet, although some decisions also have to be made [2].

General Structure It is good practice to place the sensor itself on a dedicated PCB. This enables better positioning in a housing and simplifies the application of optics, which improves the system itself. Although this is not in the scope of this thesis, the general structure shall be such, that further development is possible and not unnecessarily complicated. Therefore, the project will be divided as follows:

- The sensor will be placed on the FPA.
- The other electronics will be placed on the PEU.

Supply Voltages The datasheet of the PICO1024™ states, that a $3.6V$ supply voltage is needed. Its noise density has to be less than $20nV/\sqrt{Hz}$ from $1kHz$ to $10Mhz$.

Bias Voltages The documentation for the PICO1024™ lists a total of six pins, that need to be supplied with a bias or reference voltage. See table 2.1 for an overview.

Name	Function	Value
VDET	Active Bolometer Bias Voltage	$0V$
GFID	Active Bolometers Gate Voltage	$1V - 3.2V$
VSK	Compensation and coarse bolometers bias voltage	3.6V
GSK	Compensation Bolometers - Gate Voltage	$1V - 3.2V$
VBUS	CTIA reference voltage	$2.3V$
GOC	Coarse Bolometers - Gate Voltage	Adjustable

Table 2.1: Reference Voltages for the PICO1024™

The signal GOC is special in this case, as it refers to a feature that the current version of the PICO1024™ does not provide. It shall be left adjustable. The signals GOC and GFID will also be adjustable so that the optimal operating point can be evaluated during testing. A digital-to-analog converter (DAC) will be used to generate a voltage that is given by the FPGA.

Clocks and Control Signals A total of 4 serial signals are needed for the operation of the PICO1024™. They are listed in table 2.2. To ensure signal integrity, the datasheet lists a requirement of a maximum rise time of $5ns$.

Name	Function	Maximum Frequency
SERDAT	Serial Data	Synchronized on MC
MC	Masterclock	26 MHz
INT	Integration Time	92 kHz with 4 outputs.
RESET	Frame Synchronisation	Depends on frame rate

Table 2.2: Clock and control signals for the PICO1024™

The SERDAT signal is needed to initialize the PICO1024™. In it, the mode of operation and other parameters are set. These signals are further explored in chapter 2.1.2.
Figure 2.1 shows an example of the clock signal sequence as it is required in the detector datasheet. The RESET and INT signals change their states only on the rising edge of the masterclock signal. The on-time of the signals will also depend on the masterclock's period length (1 TMC equals one period of the masterclock).

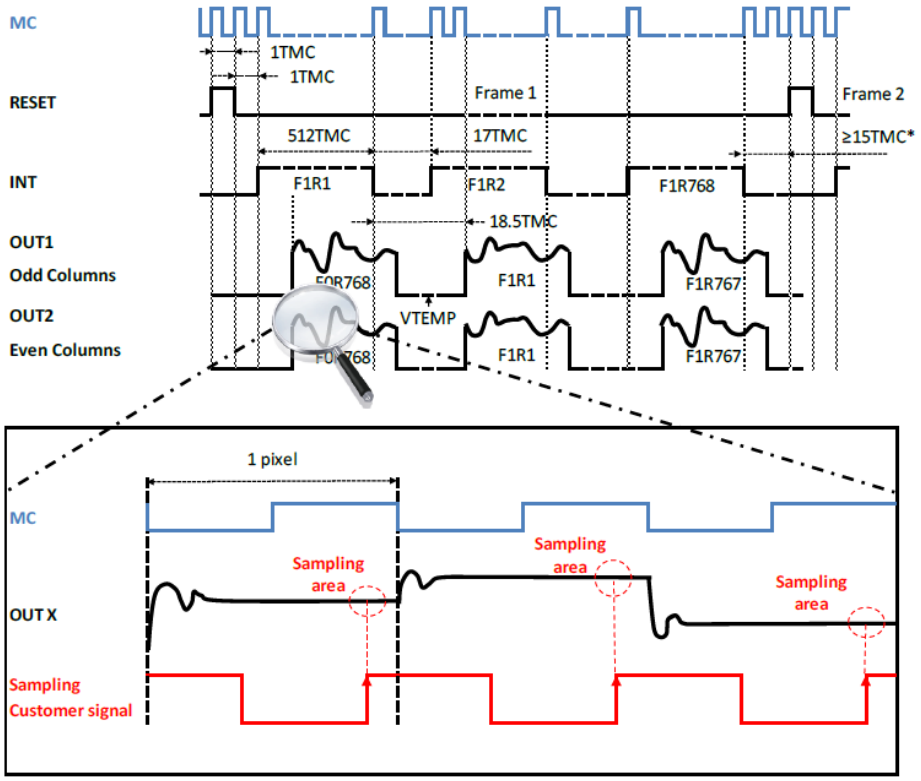


Figure 2.1: Clock Signal Sequence [2] - *One TMC corresponds to one cycle of the masterclock. In each cycle of the masterclock, one pixel is read out. The signal is sampled near the falling edge of the masterclock so that the signal has enough time to settle. "F1R1" correlates to the first row of the first frame. This example uses the full frame with two outputs. During the high time of the INT signal, each output generates 512 pixels for a total of 1024 pixels - the full frame possible. A row is read out, while the next row is integrated.*

Power-On Sequence To ensure optimal starting behavior, the bias and supply voltages need to be applied in a strict sequence. The required sequence is detailed in table 2.3. The clock signals from chapter 2.1.1 must also be applied in the correct sequence.

First Step	Apply 3.6V supply voltage.
Second Step	Enable the masterclock signal.
Third Step	All other supply and bias voltages are supplied.
Fourth Step	The serial configuration data are sent with the SERDAT signal.
Fifth Step	Reset and INT can be applied to start operation.

Table 2.3: Starting Procedure as in the Detectors Datasheet [2]

Output Signals The PICO1024™ supports a 2-output and a 4-output mode. These are analog signals with an amplitude of $0.5V - 2.9V$. The higher the intensity of incoming infrared radiation, the higher the output voltage. Additionally, the sensor provides the sensor temperature on an analog output. The load impedance of these analog outputs has to be more than 1 $M\Omega$. To interpret these analog signals, an analog-to-digital converter (ADC) is needed.

The requirements as derived from the datasheet or the configuration of the PICO1024™ are consolidated here:

- The frontend electronics will be split into FPA and PEU.
- FPA and PEU will be connected with a 31-pin micro-D connector.
- The PEU will be supplied with an external power supply of 6V and derive all needed voltages from that.
- The PEU will include an FPGA that generates the 3 clock signals as well as the serial link.
- The FPGA will control ADCs to interpret the detector's analog output signals.
- The FPGA will control the adjustable bias voltages of the detectors.

2.1.2 Modes of Operation

The detector is capable of different modes of operation. Those are configured by the SERDAT signal and the chosen frequencies for the clock signals. The first choice to be made is the number of output channels. Using four outputs instead of two allows for double the amount of data to be transmitted in an amount of time. This enables higher frame rates and is required for frame rates of more the 60Hz. For this application, the frame rate is of lesser significance. Therefore the two output mode is chosen. Only using two outputs is easier for signal routing and allows for lower clock frequencies.
Choosing the masterclock frequency defines the achievable frame rate as of equation 1. By using a full frame of 1024x768 pixels and a masterclock frequency of 8 MHz a frame rate of nearly 20 Hz can be achieved. This frequency is arbitrarily chosen for its ease of implementation [2].

$$MC\ (Hz) = Frame\ Rate\ \cdot\ number\ of\ lines\ \cdot\ INT\ period\ (TMC)_{min} \quad (1)$$

Further configuration is done with the SERDAT signal. This signal is a serial link that is used to configure the detector's control registers. This serial signal can be 53 bits long for compatibility with previous projects of the manufacturer. The PICO1024™ commands additional features that are accessed by using a longer 73-bit sequence. These features include gain adjustments, windowing, and flipping the image. Four output mode is also activated in the longer sequence as well as features that are not yet implemented in this version of the sensor. Whether the 53 bits or the 73 bits are used, the detector requires an additional start bit.

This control signal is essential for the optimal configuration and operation of the detector. It is also synchronized to the masterclock signal.

2.2 Conceptual Design

With the detector in mind, a design concept needs to be formulated. For use in a device, it is beneficial to have a dedicated sensor head. This way the actual detector can be placed at the best possible position while the main electronics are positioned for ease of use. The electronics will therefore be split into the Focal Plane Assembly (FPA) and the Proximity Electronics Unit (PEU). Figure 2.2 shows the overall concept. The FPA will house the detector and little electronics besides that. The biggest share of the components will be on the PEU. This includes an FPGA and the components needed to digitize the signals of the detector. An external power supply unit will provide a single supply voltage. The PEU will generate all other needed voltages from this external supply. The electronics on the PEU are also responsible for all configuration signals, supply, and bias voltages that the detector needs for operation.

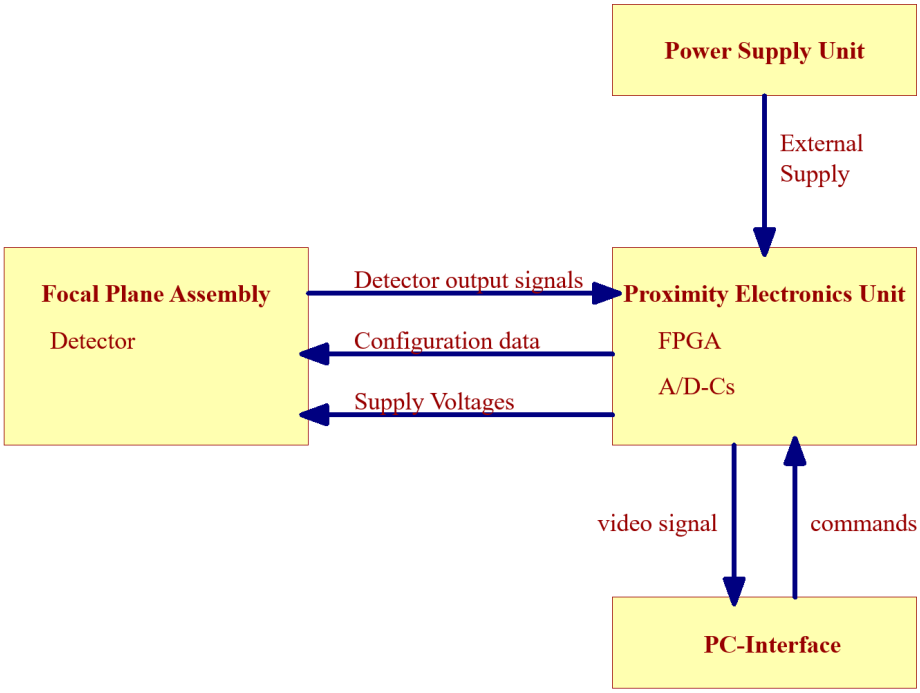


Figure 2.2: Design concept - *Two boards will provide flexibility in positioning the detector while still housing the electronics for digitizing the analog detector output signals.*

2.2.1 Focal Plane Assembly - FPA

The FPA will house the PICO1024™ and its further design is specified by this detector. The detector's analog outputs have to adhere to the specifications outlined in the previous chapter. At the FPA, the load impedance at the analog outputs is the most relevant part. An operational amplifier (op amp) in a simple buffer configuration will be able to drive the signal across the wired connection without issues. Figure 2.3 details the FPA in a block diagram.

The bias voltages needed by the detector are generated on the PEU and can be directly connected to the detector. Since the 2.3V bias voltage is fixed, it will be generated on the FPA. A very simple circuit can be used and the space usage so minimized. By placing this circuit on the FPA, its accuracy is improved greatly.

The serial clocks and the serial configuration data will be transmitted via low voltage differential signaling (LVDS). A receiver is needed, to transform the differential signal back to a single-ended signal. LVDS is further explored in chapter 2.6.3.

2.2.2 Proximity Electronics Unit - PEU

The PEU holds the major share of the electronic components (see Figure 2.4). With the FPGA chosen, the need for a total of seven different power domains becomes apparent. They supply the FPGA, the ADCs, and all other components. The ADCs are needed to make the analog output signals of the detector readable by the FPGA.

The FPGA is at the heart of the PEU. It will interpret the video signal and transfer it to the connected computer. The FPGA is also responsible for supplying the detector with the serial configuration data and the required clocks. Some of the bias voltages are left variable according to the datasheet. Those will be generated by a DAC that is controlled by the FPGA.

The specific sub-circuits are explored in the following chapters. Table 2.4 provides an overview of the used supply voltages.

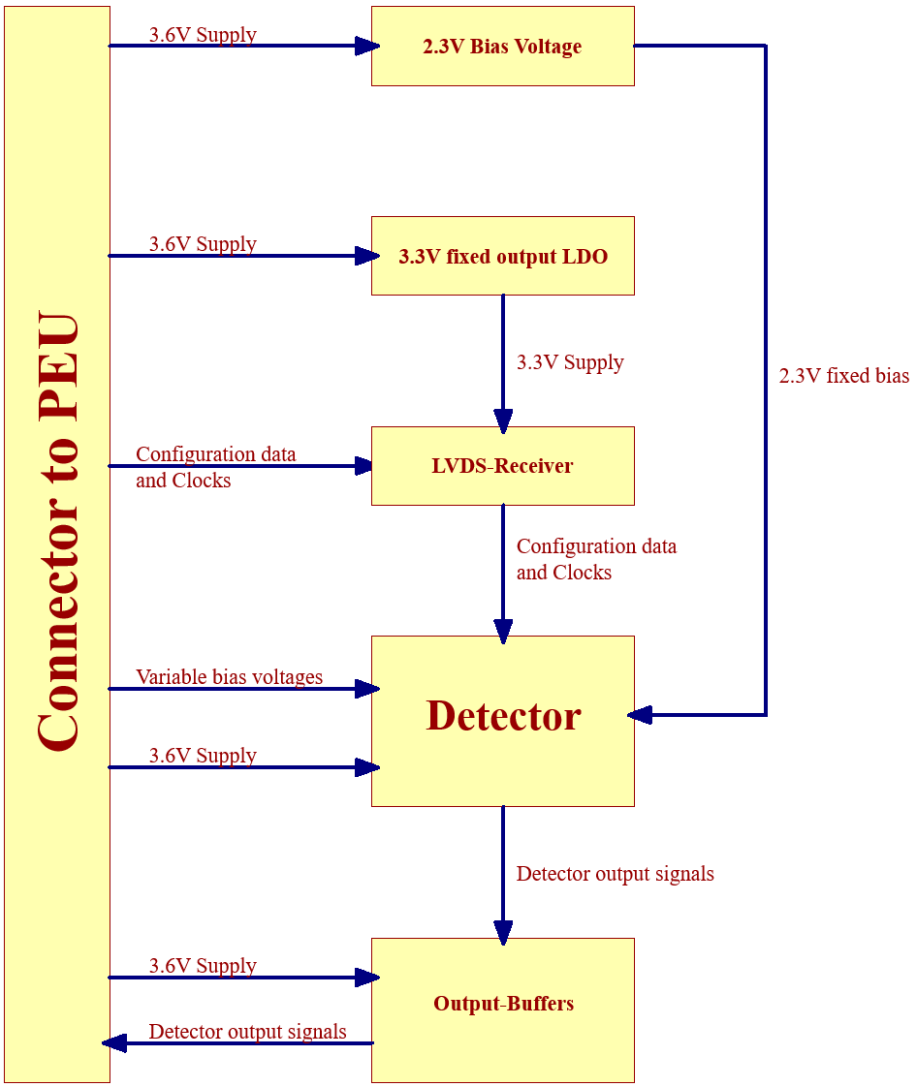


Figure 2.3: FPA concept - *The FPA houses the detector itself and minimal components beyond that. The detector requires a defined output impedance and is not capable of reliably driving the signals across the wire connection. Buffers are used to ensure better signal propagation. An LVDS receiver will convert the differential signals for the detector to use.*

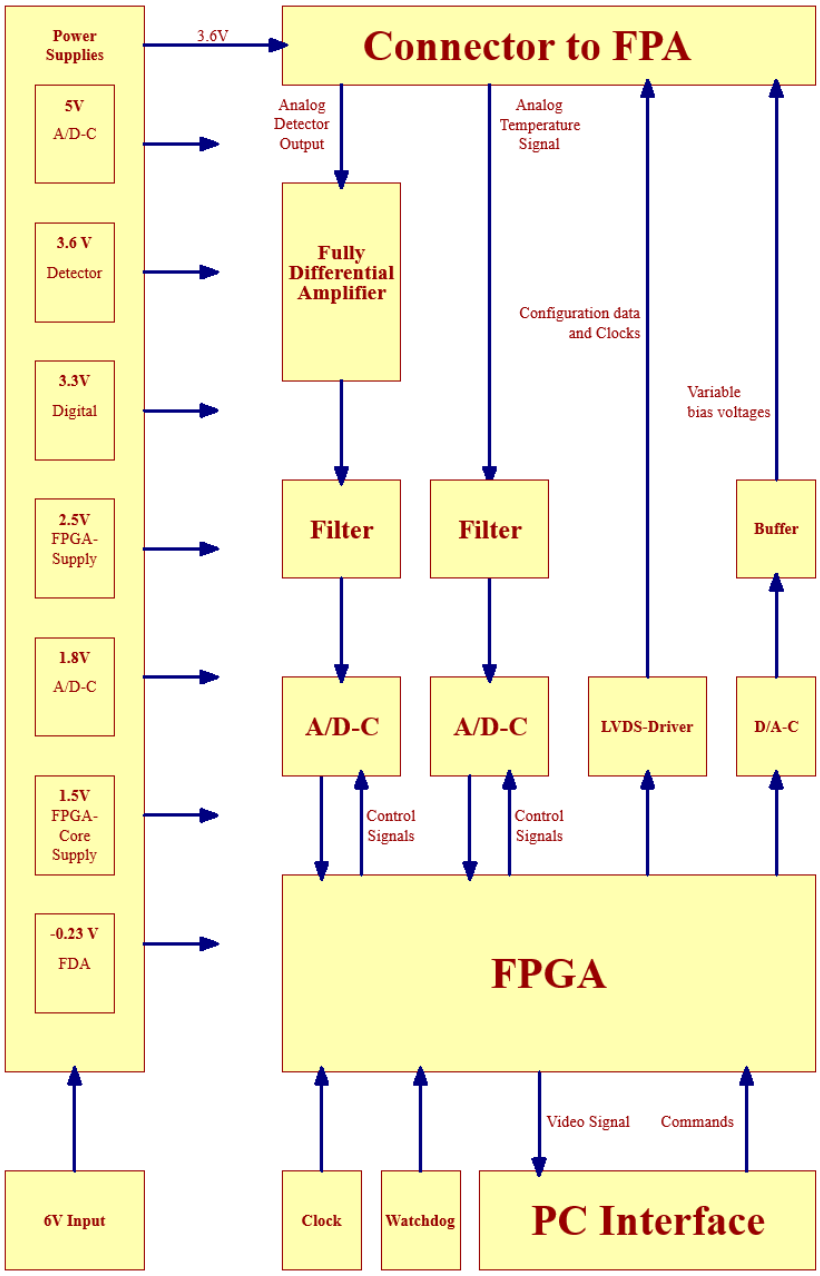


Figure 2.4: PEU concept - *The PEU is mainly responsible for interpreting the analog output signals and generating the required supply voltages.*

2.3 Power Supply

The design will need power supplies with several values. An important factor with supply voltages is their noise level. Noise or ripple voltages on those will propagate through ICs and affect signals and other ICs. Because of that, the supply voltages should be generated with great care. Using a linear dropout regulator is favorable compared to the classic approach of switching voltage regulators.
The PICO1024™ needs to be supplied with a very accurate $3.6V$ supply. The main ADC for the output signals must be supplied with $1.8V$ and $-0.23V$, while the ADC for the temperature measurement signal is powered by $5V$. They are further explored in chapter 2.5.
A single $3.3V$ supply is used for other digital circuits. In addition to that, a $2.5V$ supply is needed to power the FPGAs LVDS module. The FPGA itself is powered by a core voltage of $1.5V$. See table 2.4 for an overview.

5V	ADC supply voltage
3.6V	Detector supply voltage
3.3V	Digital supply voltage
2.5V	FPGA-LVDS supply voltage
1.8V	ADC supply voltage
1.5V	FPGA core voltage
-0.23V	Negative supply for the amplifers

Table 2.4: Supply Voltages Overview

To generate these voltages, the external supply needs to be higher than the highest supply voltage. Therefore a $6V$ input voltage is chosen to supply the power supply circuits. Using low-dropout regulators (LDO) is a suitable solution for most of these supplies. The currents are low enough, for the power loss to remain manageable. The exception to this is the $1.5V$ FPGA-core voltage.
The ADM7151 is chosen to achieve the needed supplies. This IC is an ultralow noise, high power supply rejection ratio (PSRR) linear regulator [6]. The PSSR suppresses errors and noise that would propagate from the IC's input voltage. Its noise spectral density of $1.7nV/\sqrt{Hz}$ conforms to the detector's specifications. This specific IC is available in multiple versions, that optimize the noise behavior according to the relation between input and output voltage. The ADM7151 has an adjustable output voltage and will therefore be used for the 5V, 3.6V, 2.5V, and 1.8V supplies. Its nominal output voltage lies between 1.5V and 4.0V. Therefore, the "-02" version is applied for the 5V supply, since its output range lies between 1.5V and 5.1V.
The 3.3V supply will be realized by the ADM7150 from the same component family. This IC has a fixed 3.3V output voltage and is therefore better designed for low noise and overall performance.

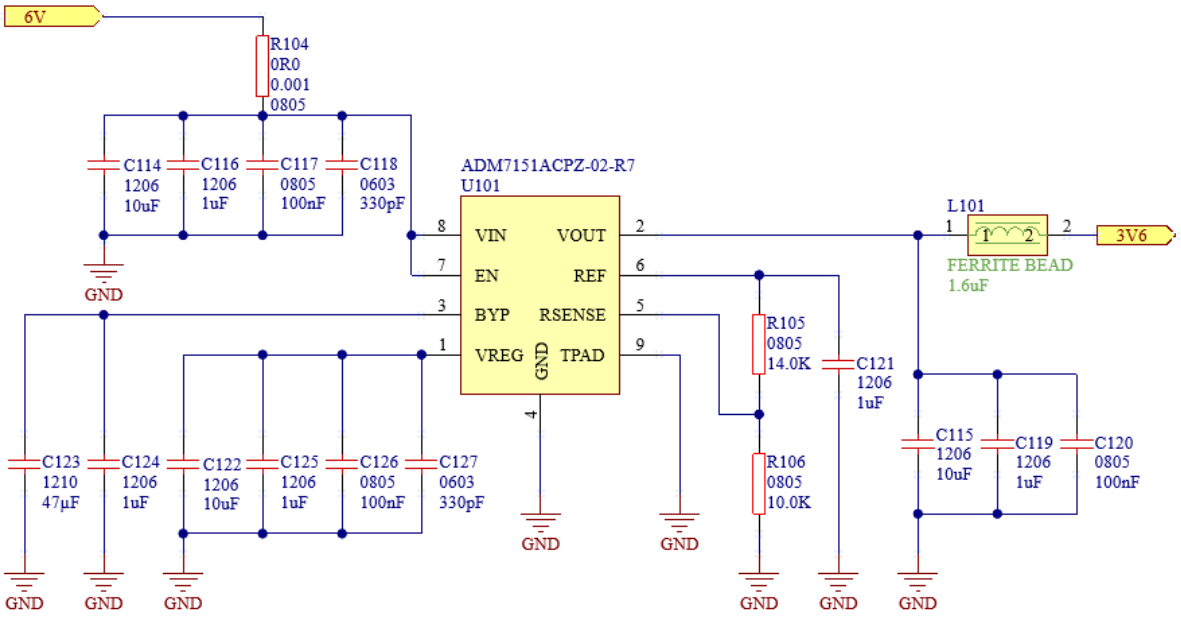


Figure 2.5: 3.6V Power Supply - *The output voltage of this linear regulator is defined by the voltage divider in R105 and R106. The other supply voltages are generated by a similar circuit, where these resistors realize a different ratio.*

2.4 Bias- and Reference Voltages

The detector requires a considerable amount of bias voltages for operation [2]. One of these is a $2.3V$ bias. It is fixed and used as the reference voltage for the bolometer currents integration. Due to its fixed and relatively simple nature, it will be positioned on the FPA. As can be seen in figure 2.6 the resistors R202 and R204 form a voltage divider that is the input for the OPA837 in buffer configuration. This provides a stable output which is suitable for this application [14].

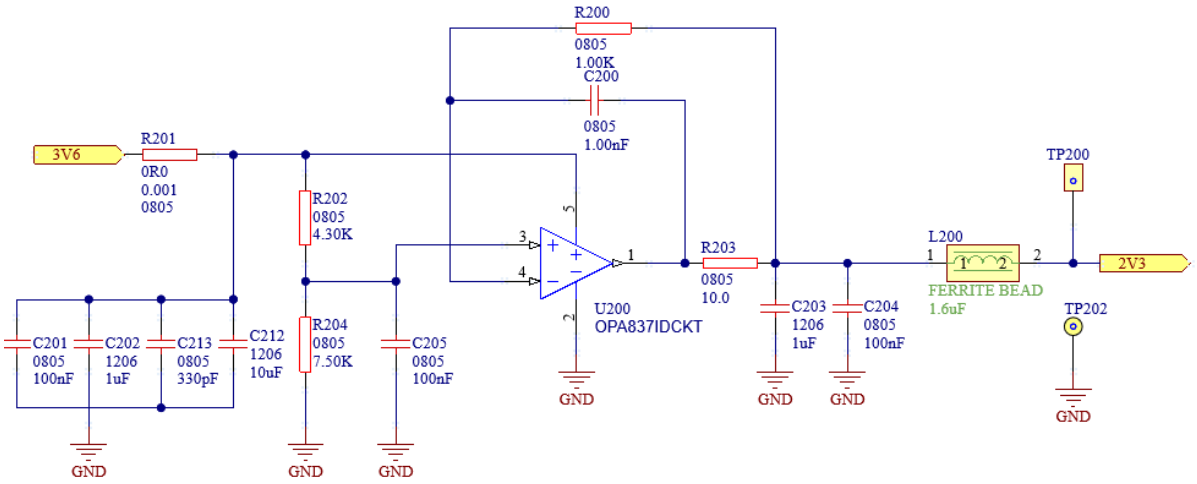


Figure 2.6: 2.3V Bias - *The 2.3V bias generation is placed on the FPA. The voltage divider of R202 and R204 is used to produce the 2.3V which is then driven by the operational amplifier.*

Additionally, the detector requires 3 variable output voltages. These will be realized by using a digital-to-analog converter that is controlled by the central FPGA. The chosen component will require an external reference voltage of $3.3V$. It will be generated by using the REF3433-EP. This component is a low-power low-noise voltage reference. It reliably provides the needed reference voltage without further components [16].

2.4.1 DACs

Up to three variable bias voltages can be used for operating the detector. The voltage range for those lies between $1V$ and $3.2V$. The AD5684 is chosen to be used. Its outputs are configurable through the serial peripheral interface (SPI) or provide a defined level at startup. Since the FPGA will not be available immediately after power-on, this feature is important. Depending on the potential at Pin 9 ($\overline{LDAC}$) on the IC, the output is defined during start-up. If it is at $0V$ or below a logic threshold, the outputs will power up at mid-scale. With a 3.3V supply, the output is therefore to be expected at $1.65V$. If the DAC is faster

than the other voltages, the detector's power on sequencing might be violated. This can be rectified by defining the Pins value with the FPGA. Besides the SPI, three additional configuration signals are controlled by the FPGA. One of these is the $\overline{LDAC}$ signal. By defining the FPGA's output during reset here, the DAC's output can be defined while the FPGA is still in reset mode [15].

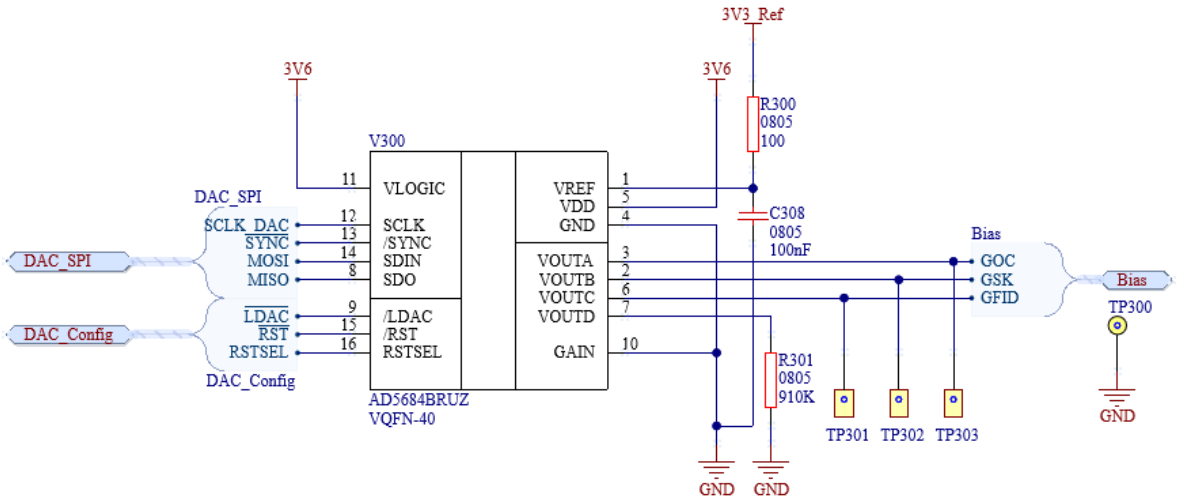


Figure 2.7: Digital-to-Analog Converter - *The control signal $\overline{LDAC}$ provides the option of adjusting the DAC's output and so the bias voltages while the FPGA is in reset mode.*

Usually, an additional buffer circuit would be needed to drive the signal over the wired connection. The AD5684 has the additional advantage of an integrated output buffer. This way an additional IC and the necessary passive components can be omitted.

2.5 Output Signals

The PICO1024™ generates an analog output between $0.5V$ and $2.9V$. This signal should be transferred to the PEU with as little disturbance as possible. Due to the wire connection from FPA to PEU and the detector requirements a buffer is needed. These buffers need to be selected for fast response and low noise. Low power consumption is also beneficial, to keep the overall power needed on the FPA down. Rail-to-rail behavior is not necessarily needed due to the expected voltage range of the signal. A simple buffer circuit is used. Most of the passive components will be adjusted or omitted completely during testing. The circuit is detailed in figure 2.8. The operational amplifier is placed in the most basic buffer configuration. The capacitors and resistors at its output side are placed to facilitate adjustments if necessary.
The chosen operational amplifier is the ADA4897 by analog devices. According to its datasheet, it provides a low-noise solution with very low power consumption [1].

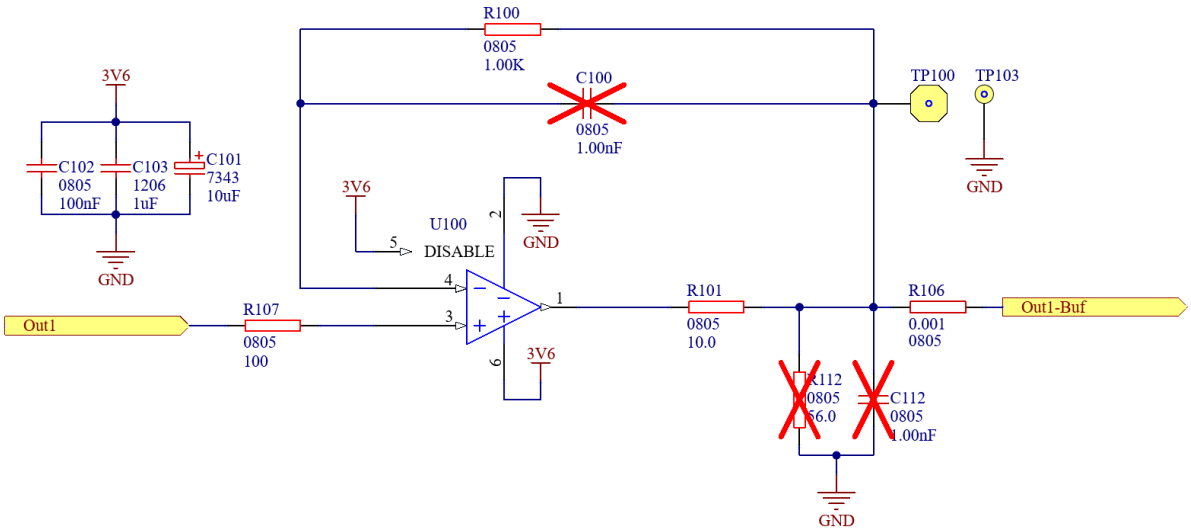


Figure 2.8: Output Buffer - *The output buffer on the FPA. The crossed-out components are not fitted during assembly and are available for adjustments during testing.*

2.5.1 Fully Differential Amplifier

The signal on the PEU will then have to be processed by an ADC. High-performance ADCs usually use differential input signals. Differential signals have the advantage of better noise performance. Therefore the single-ended output signal needs to be converted. In this case, a fully differential amplifier (FDA) will be used. The FDA converts a single-ended signal into a full differential balanced output signal [19]. An argument could be made, to place the FDA on the FPA to utilize the differential signal for the wire connection. It is decided against this, to keep the electronics on the FPA as simple as possible. A further reason is the common mode voltage. This is a precision reference voltage that is generated by the ADC. It and its precision are very important for the accuracy of the converted differential signal. Therefore it is good practice, to place the FDA as close as possible to the ADC. The FDA is in essence still an amplifier. So additional passive components were placed in the proximity to enable adjustments during testing.

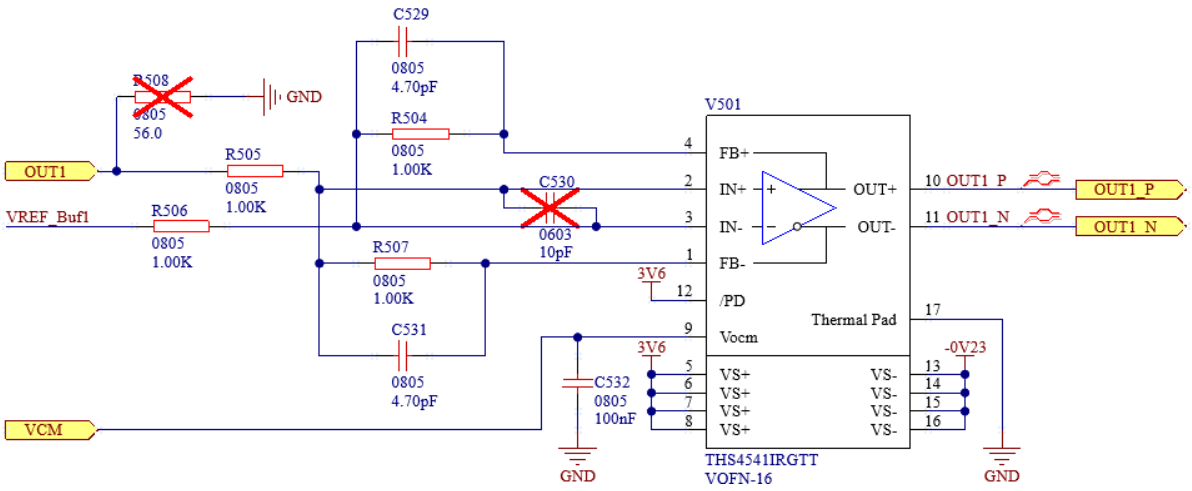


Figure 2.9: Fully Differential Amplifier - *The inverting input V_{REF} is buffered before it reaches this circuit. This way its behavior will be very similar to the detector's analog output signal, as it uses the same components and experiences similar noise influences.*

The chosen FDA is the THS4541 [17]. Its function and provided features match the chosen ADC as it is the component that is used in available evaluation boards [20]. It will therefore be ideal for ensuring the ADC's functionality.

2.5.2 ADCs

The ADC and its resolution are crucial for the entire system and the precision of the measured output signals. Therefore the choice, of which component to use, was made early in the design process and the other components matched to this IC. The choice fell on the ADC3661 by Texas Instruments. This ADC has a resolution of 16 bits and is designed for low-noise applications. Its dual channel inputs match the two outputs of the chosen mode of operation. The analog bandwidth of 900 MHz is more than sufficient for the chosen speeds and steep edges. The output signal is transmitted via a low-voltage-differential-signal which can easily be processed by the FPGA with the added benefit of better noise resilience. For configuration, a standard SPI is available [20][7].

As mentioned in the previous section, the ADC generates the common mode voltage for its differential input. In this case, it is a DC signal with an amplitude of $0.95V$.
ADCs use a reference voltage to convert the analog signal. The ADC3661 uses an integrated voltage reference. Using internal circuitry is usually more precise than adding external resistors and traces. Each trace and additional component would be subject to tolerances and deviations that influence the reference voltage, the common mode voltage, and therefore the overall signal quality. The internal reference voltage is also used for the FDA.

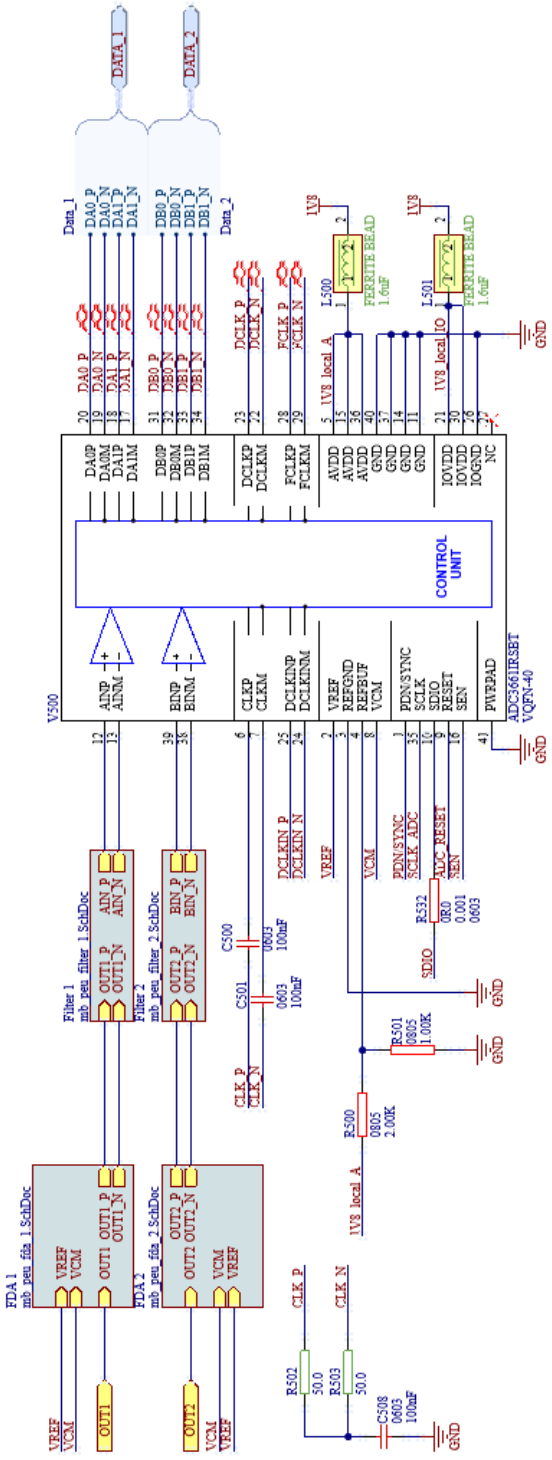


Figure 2.10: Analog-to-Digital Converter - *The ADC-modules input signals are on the top left, labeled as "OUT1" and "OUT2". This designation stems from the detector's perspective, as these signals are the detector's analog video outputs. The signals VREF and VCM are generated by the ADC IC and used by the FDAs. All other signals originate at or are routed to the FPGA.*

2.5.3 Filter

Due to the limited rise time and general bandwidth of every operational amplifier, the signal will have an overshoot and additional swinging after each edge. Filters have to be carefully adjusted to reach an ideal waveform. Several resistors in the signal path can be used for this. They form RC-lowpass filters together with parasitical capacitances and inductors. An anti-aliasing-filter (R520 and C568 for example) will allow further adjustments.

ADCs sample the incoming signal with high frequencies. This often feeds back to the incoming signal. Therefore a glitchfilter has to be placed in front of the differential input. The exact values of the capacitors must also be adjusted during testing. The anti-aliasing filter and the glitch filter are represented in figure 2.11. This filter network is placed once for the two detector output paths [20].

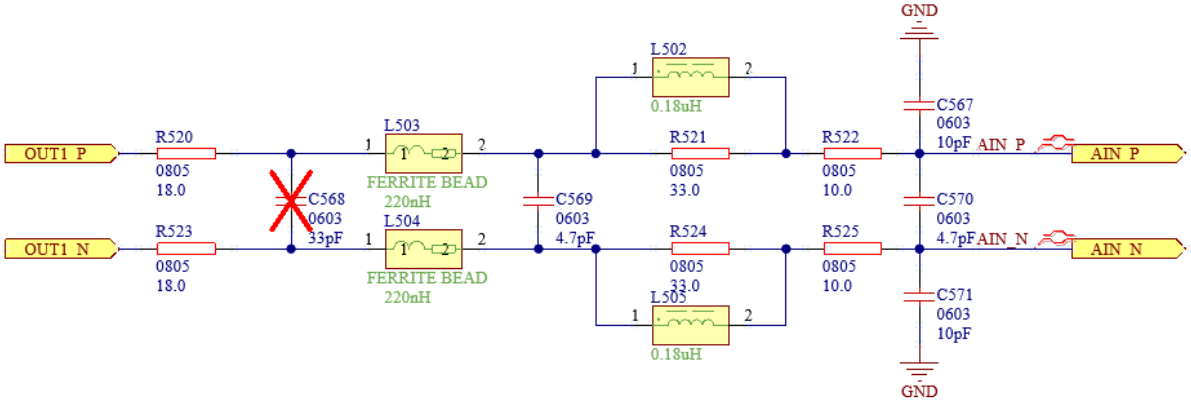


Figure 2.11: Filter circuit - *During testing it was determined, that the signal integrity is best when omitting the capacitor C568. During further testing, its value should still be adjusted to yield the best results for the given situation.*

2.5.4 Simulation

Simulating a circuit provides additional insight into its functionality and dimensioning of the passive components. Figure 2.12 shows the result of simulating the small signal behavior of the buffer circuit on the FPA (see figure 2.8).

The circuit is stimulated by an 8 MHz rectangular signal. It and its steep edges represent the output signal of the detector, which will be similar to that. An amplitude of 200mV is also a reasonable assumption. The output seems to be usable although a pretty large overshoot is observable. This is adjustable by changing the values for R100 and R107. If needed, this can be compensated during testing to conform to real conditions. Since sampling will be done close to the falling edge (see chapter 2.1.1) the overshoot is even less relevant.

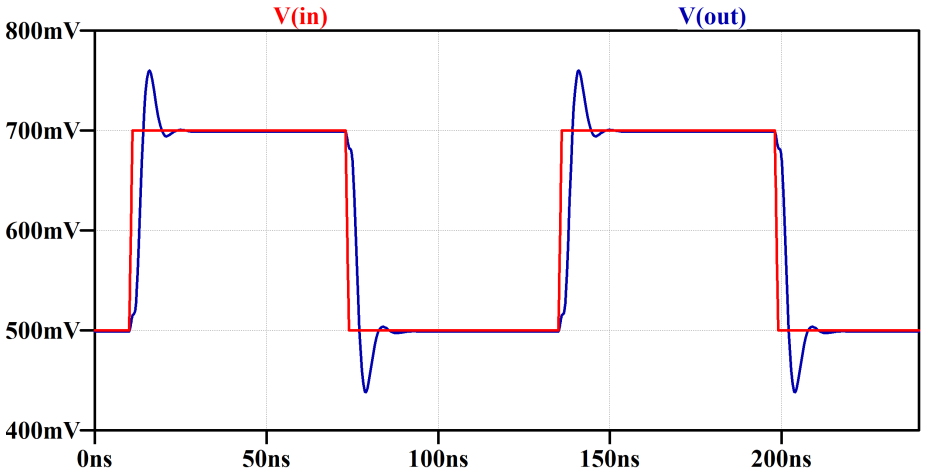


Figure 2.12: Small Signal Buffer Simulation - *Since sampling will be close to the falling edge, the overshoot influence is small.*

In real conditions, the maximum output swing that is expected from the detector is the difference from 0.5V to 2.9V. Figure 2.13 shows the results for this large signal behavior. The ADA4897 has a limited rise time which is much more prominent for larger output swings like this.

Figure 2.14 shows a section of the simulated bode diagram. With the 3dB cut-off frequency equivalent to an output of around 0.707V at an input voltage of 1V, an estimation can be made. The -3dB threshold is broken at around 171 MHz. This leaves enough room for high-frequency contingents.

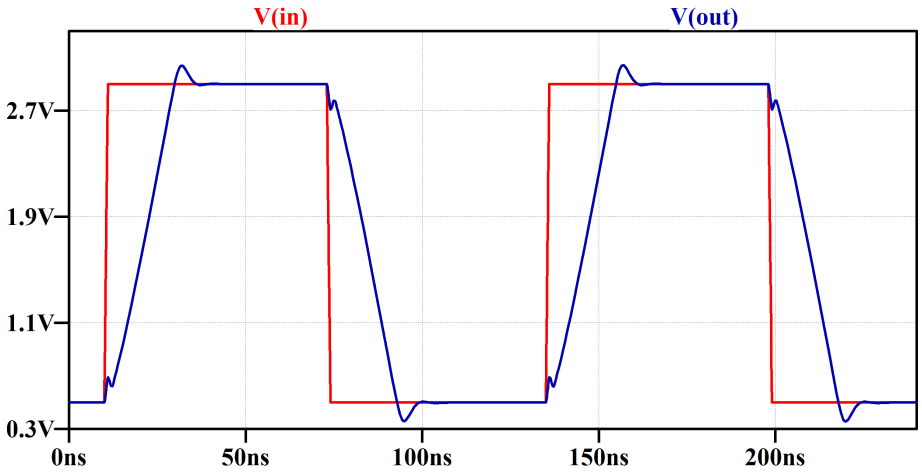


Figure 2.13: Large Signal Buffer Simulation - *With larger amplitudes, the limited rise time becomes more prominent.*

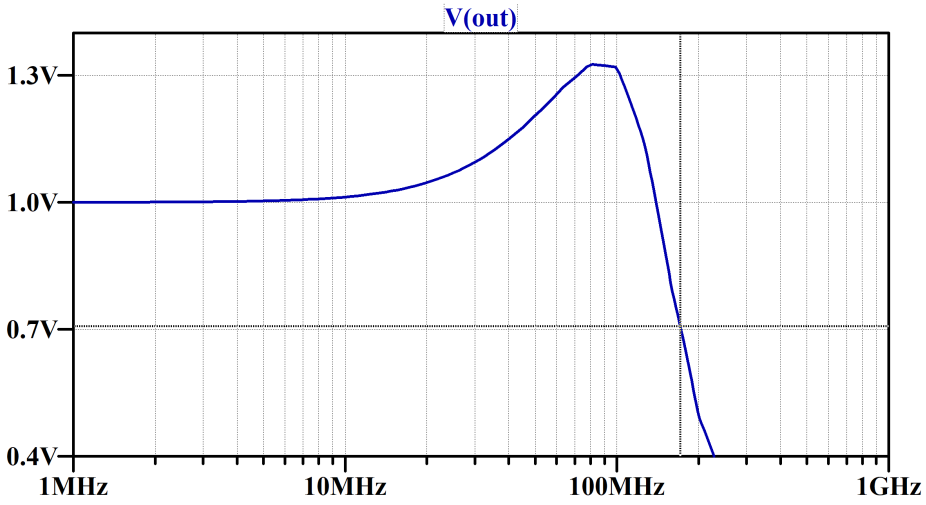


Figure 2.14: Buffer Cut-Off-Frequency - *By using the AC-analysis available in LTSpice, the cut-off frequency can be estimated at around* 170 MHz.

2.5.5 Temperature signal

The detector provides an additional analog output for a temperature signal. This information can be used to calibrate the sensor and optimize the imaging. Temperature changes much slower, so the ADC for this signal does not adhere to the same requirements as the other one. The LTC2312 is chosen for its precise integrated reference voltage. Depending on the IC's supply voltage, a different reference voltage is generated. By applying a 5V supply, a reference voltage of $4.096V$ is generated. This is ideal, as it optimizes the signal amplitude range with the ADCs resolution of 14 bits. Figure 2.15 shows the circuit for the temperature signal. Since the expected signal is only changing with very low frequencies, a simple RC element suffices as filter topology. Also, this ADCs input signal is not differential but only single-ended. At these speeds, this is an advantage as a lot of additional components can be omitted [3].

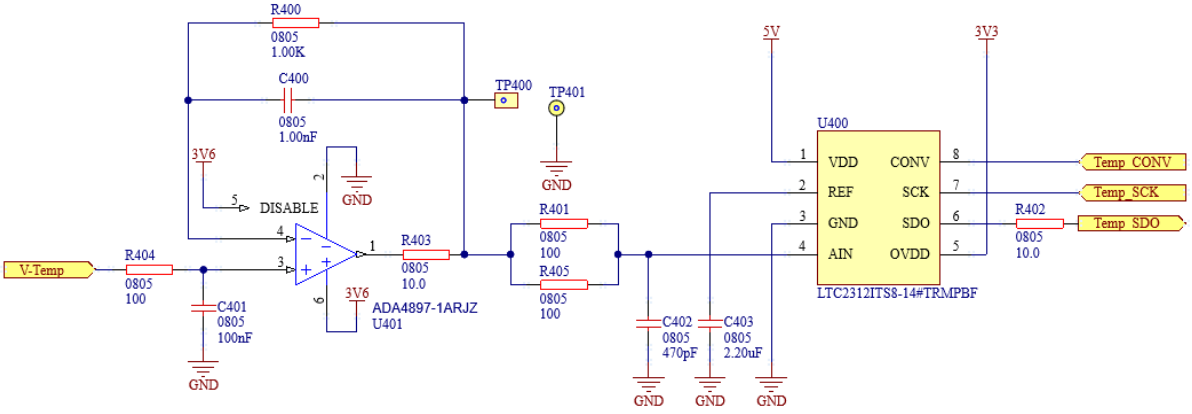


Figure 2.15: Analog-to-Digital Converter for Temperature Signal - *The temperature signal can be handled with much fewer components. The ADC input is a single-ended signal and a simple RC-element suffices for filtering. An operational amplifier in buffer configuration ensures defined input impedances.*

2.6 Interfaces

The core concept defines the use of two PCBs. These two have to be connected. For ease of use and also due to cost constraints, the decision is made to use a wired connection. The connector-specific component is chosen to suit the applications at DLR. A Micro-D-Sub connector has been used in different projects, so it is still in stock. For this connection, a 31-pin variant is chosen. The corresponding pin assignment is shown in figure 2.16. The assignment is done with the signals in mind. Signals that are faster or require precision and noise resistance are surrounded by ground connections to shield the signal from noisy influences. The wires can then also be twisted together with a ground connection to enhance this shielding effect. The differential signals are instead twisted pairs with their partner.

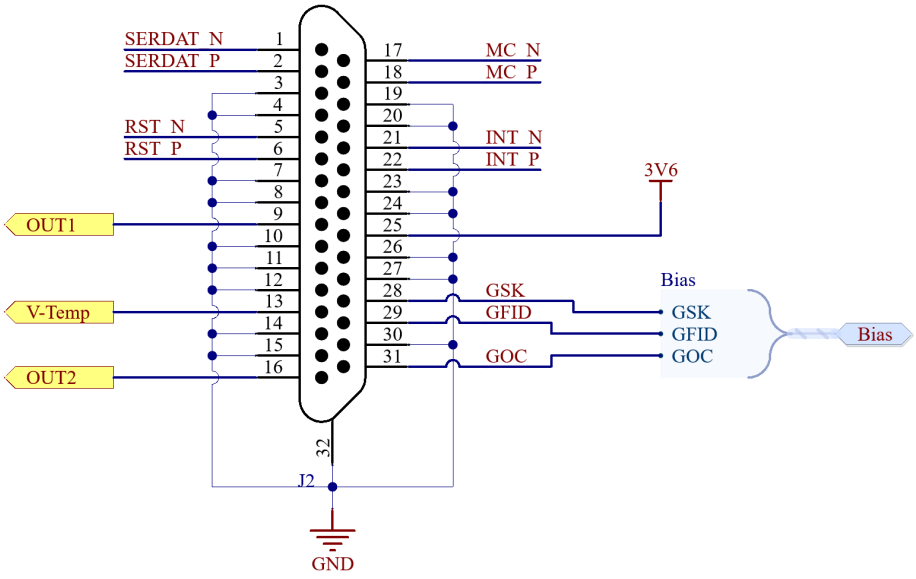


Figure 2.16: FPA-Connector - *Differential signals are placed closely together to enable twisted pair connections. The other signals are interspersed with ground connections to help in the shielding effort.*

The second connector will be the power connector. This interface will supply the board with a 6V supply and its corresponding return path, the ground connection. The cable for this connection will be reused from a previous project. Therefore the Pin assignment is specified by this cable as is visible in figure 2.17. Other projects utilized an additional complimentary power supply. Since the PEU will only be supplied by a single supply voltage, these connections are grounded with an adjustable resistor.

An interface to a computer is needed to visualize the signals, that the FPGA reads. As with the power connection, a module is reused from previous projects.

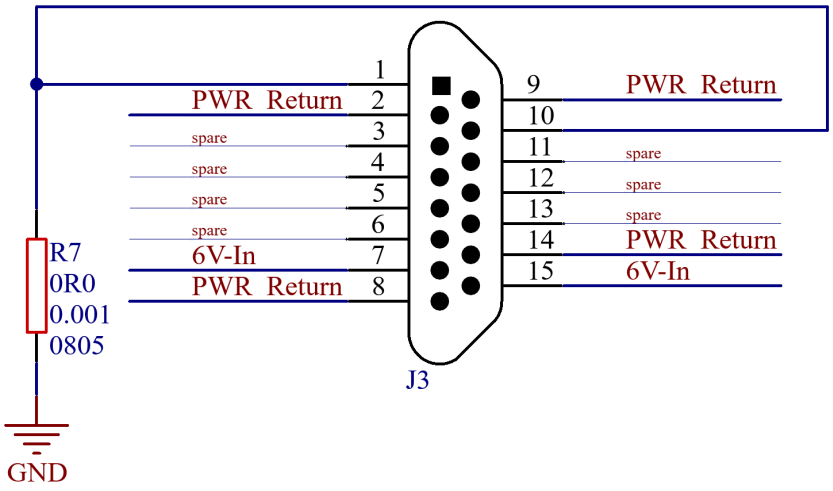


Figure 2.17: Power Connector - *The power connector is reused from a different project and utilizes a fixed pin assignment. The other projects used dual supply inputs, so the additional pins are grounded. These prevent floating potentials with undefined states.*

This allows easy adaptation of existing programs and test assemblies in the DLR for this new detector and its electronics.

Lastly, a JTAG connector (see figure 2.18) is needed to access the FPGA. Its assignment is given by the programmer and is implemented without any adjustments. JTAG is a popular standard for testing and debugging ICs. Its use is not in the scope of this thesis.

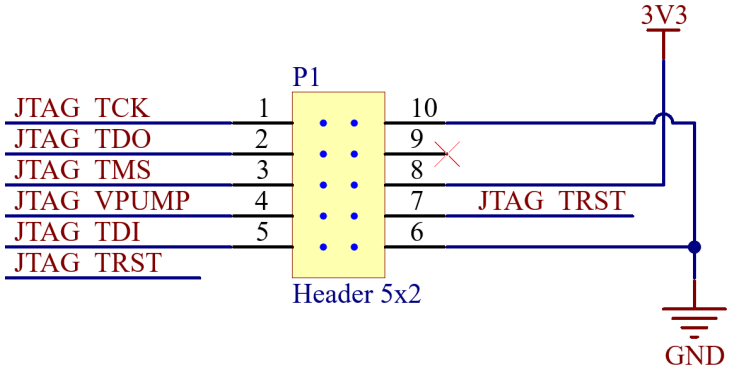


Figure 2.18: JTAG Connector - *The pin assignment is defined by the JTAG-programmer, that will be used.*

2.6.1 FPGA Interface

An FPGA on the PEU will serve as the central control unit for the detector and its data. The detector and the ADC require precise clock signals, which an FPGA will be able to generate. The A3PE3000 by Microchip Technology in the FG484 package was chosen since it was used in different DLR projects already. It uses up to 484 I/O pins and 8 banks [12]. Each bank can use a different logic supply voltage to match the connected circuits. To ensure shorter signal paths within the chip, it is advisable to limit the used pins to a single quadrant. This would mean only using two banks, as they are positioned in star form around the center. Due to the different supplies needed for the banks, this is not possible. In total, four banks are used to distribute the signals. The exact positioning for each signal is directly linked to the positioning on the PCB and the corresponding signal routing. See chapter 2.7 for details on the component placement and the signal routing.

The FPGA must meet several requirements to operate the detector. These are consolidated in table 2.5.

Requirement	Description
REQ-FPGA-01	The FPGA shall function with an active HIGH reset signal.
REQ-FPGA-02	The FPGA shall be configured to have its I/O-Pin A20 held at logic low level during reset.
REQ-FPGA-03	The FPGA shall generate the clock signals needed for the detector according to its datasheet.
REQ-FPGA-04	The FPGA shall operate the two ADCs that are used by the detector's output signals.

Table 2.5: Requirements for the FPGA

2.6.2 FPGA Periphery

The FPGA itself requires some components to function as desired. This is very obvious in the power supplies that are generated (see table 2.4). A 1.5V core supply voltage is managed just for this IC. To be able to process LVDS signals, an additional 2.5V supply is needed. For the FPGA to function, it needs a system clock. All other clocks are generated by dividing the system clock of the FPGA. To have enough room for adjustments in programming the chip, a 128MHz clock is used. This is achieved by implementing an external crystal oscillator. Ideally, the clock signal would be transmitted with a differential signal. This would be better to ensure noise resistance on the system clock. Due to component availability, an oscillator with a single-ended output is used. Future testing can be done with the differential clock signal because a different fitting option enables switching the component.

FPGAs use a power-on-reset function to initialize correctly. During the first few milliseconds, a voltage supervisor circuit asserts the FPGAs reset. This way, the FPGA initializes only as the supply voltages are already settled.

The FPGA datasheet suggests the use of multiple capacitors to stabilize the supply voltages. This applies to all different voltage domains that are used by the chip. For the core voltages, a very small package of 0402 is chosen. These packages can be placed very close to the connected pins. This is done for optimal response times.

2.6.3 LVDS Interface

LVDS, short for *low-voltage differential signaling*, is a technical standard for signal transmission. A constant current of typically 3.5mA is driven to the receiver where it meets a termination resistor of 100 Ω. The constant current results in a voltage drop across the resistor and then flows back to the current's origin over the second wire. By changing the current direction, the voltage drop across the resistor is inverted. The receiver reads this voltage drop and can receive the digital signal [10][11].

The advantage of LVDS is its low power consumption. Due to its low current and constant current consumption, the signal interference on the PEU's ground and supply potential is lower. The signal's differential nature helps against noise susceptibility and also against electromagnetic interference (EMI) caused by the signal transmission. Since the current flows in opposite directions, the induced electromagnetic fields offset to a certain degree, as long as the traces and wires are closely placed. The differential nature of the signal provides immunity to common mode noise. Any EMI from other circuits around the transmission lines will affect both lines but since the receiver only interprets the difference between the signals, the transmitted signal is unaffected.

As with many modern ADCs, its output signal is transmitted with a differential signal. The FPGA can handle this signal type, as long as the corresponding bank is supplied with 2.5V. The detector's clock signals will also profit from an LVDS transmission. They are the fastest signals on the PCBs and their accurate transmission is vital for the detector's operation. The ADN4668 is chosen as the LVDS receiver. It provides 4 channels that match the four signals that are to be transmitted: MC, Int, RESET, and SERDAT [5]. Check chapter 2.1.1 for details on these signals. A matching LVDS driver is produced by Texas Instruments. The FPGA is capable of generating LVDS signals. But since a fitting component exists and a buffer circuit would be needed anyway, the ADN4667 is used for driving the LVDS signal [4].

2.7 Detailed Design

With the overall concept and detailed modules clear, the design can be implemented. For this, the software Altium Designer is used. This is a CAD tool used to design high-complexity electronic circuits and projects. FPA and PEU will be designed in individual projects. Each will include schematics and the PCB layout. An export bill of material will be used for procurement of the electronic parts.

2.7.1 Schematics

The schematics for the FPA are relatively simple. Building upon the conceptual design in figure 2.3 a block diagram for use in Altium Designer is created. This allows for the hierarchical design structure and is the first step towards the complete schematic design.
Analog to the approach for the FPA, another block diagram is created for the PEU. Due to its increased complexity, the PEU consists of a more complex hierarchical structure.

The circuits and components are then added as discussed in the previous sections. In several instances are 0 Ω resistors included to facilitate isolating the circuit. This way, it can be tested without influencing the following components, if an error occurs. Sometimes, different components like chip beads are also used for this application.

Every active component uses some kind of supply voltage. To ensure optimal operation, capacitors are placed towards the corresponding pins. They improve the supply's behavior as they intercept ripple or peak currents. Different capacitor types and packages influence different disturbances. By placing four different capacitors, all disturbances are taken into account. This is especially important for the FPGA. It uses a lot of different voltages each with multiple pin connections. To facilitate the optimal placement of these decoupling capacitors, very small packages are used. The "0402-type" has outer dimensions of $1mm \times 0.5mm$ and is therefore ideal for dense positioning. Placing these decoupling capacitors directly under the FPGA on the other side of the PCB enables connecting them with a via directly to the corresponding pin.

Figures 2.19 and 2.20 show the hierarchical top sheet for each of the two projects. This sheet connects the other schematic sheets.

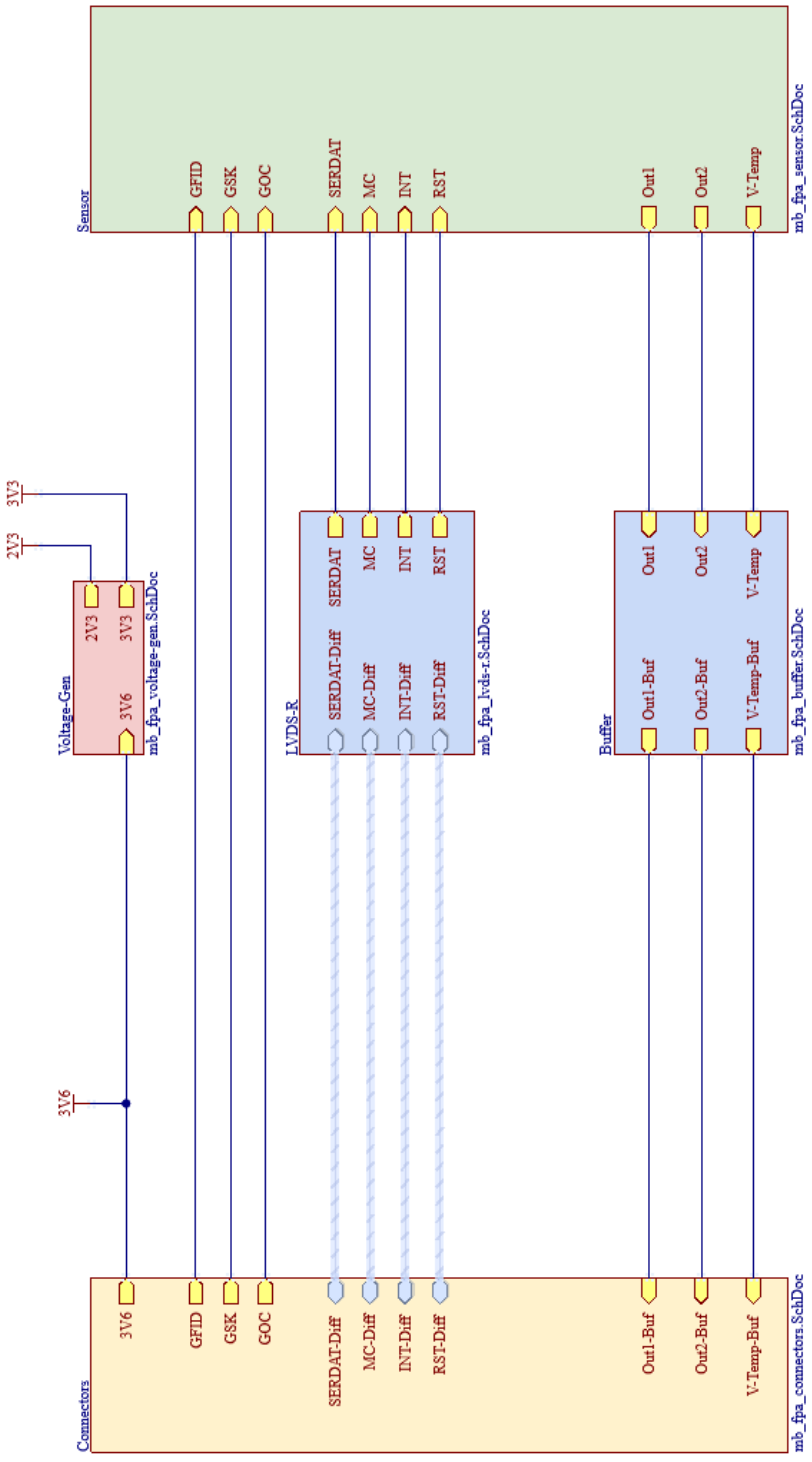


Figure 2.19: Hierarchical Top Sheet for the FPA - *Signals between different sheets are connected here while power objects such as ground or the 3.6V power supply are global signifiers. The slightly larger, light blue connections are so-called "harness" connections. They consist of multiple signals that are grouped.*

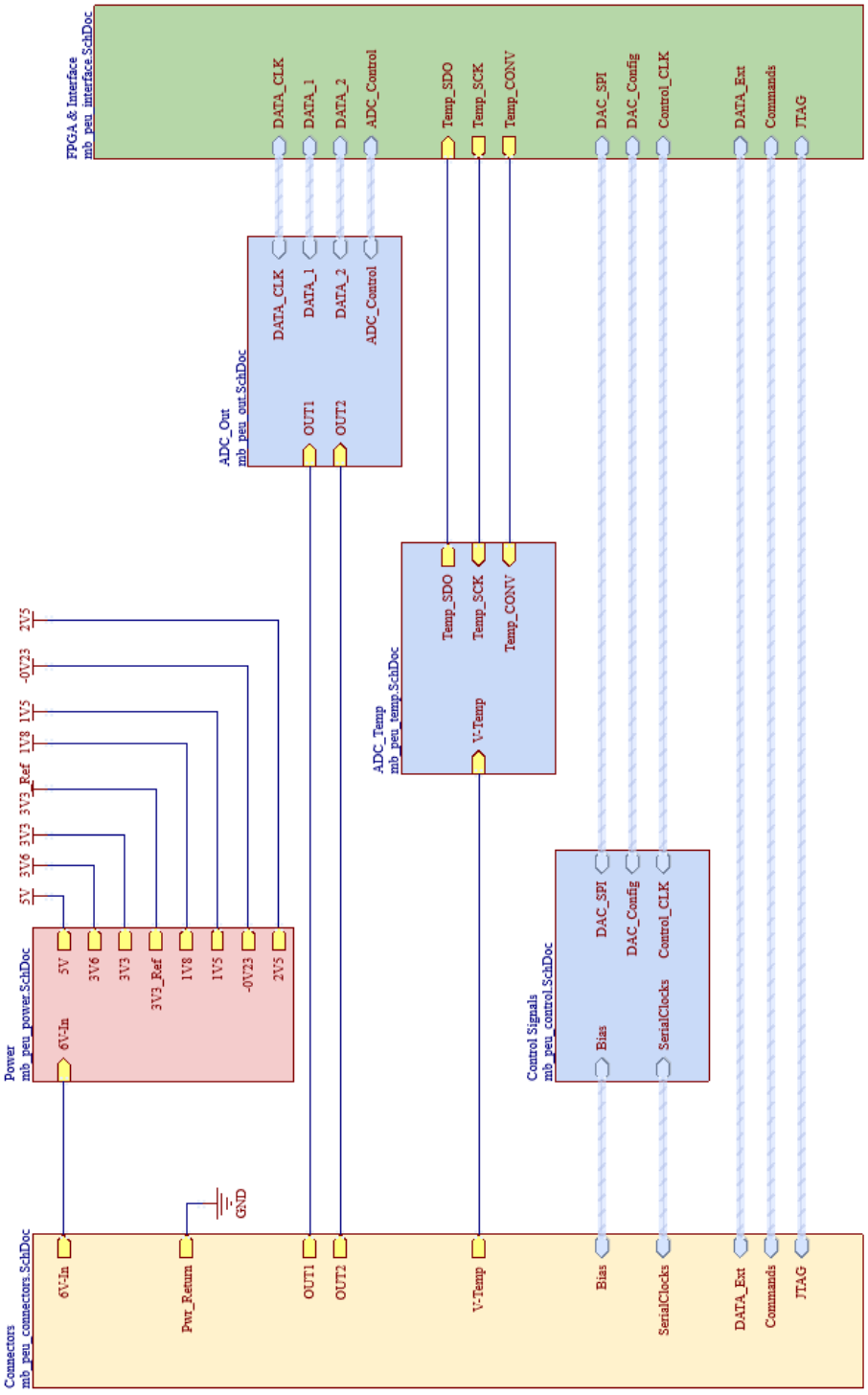


Figure 2.20: Hierarchical Top Sheet for the PEU - *The displayed signals and harnesses are to be read as in figure 2.19. Additionally, the sheets that are presented here consist them self of multiple sheets, as the schematic becomes more complex in depth. For example, each supply voltage is designed on its own sheet, which is then combined in the power sheet which is displayed here in red color.*

2.7.2 Layout Requirements

Several factors should be taken into account when layouting the PCBs for this project. As with all signal paths, the trace width is important to reduce the connection's impedance. There are no signals that are expected to carry more than a few miliampèrs of current. Trace width therefore loses its significance but using trace widths as large as possible will nonetheless improve signal integrity. Trace width will be much more important for the power supplies. Large planes on inner layers will be able to distribute the supply voltages to all needed components. To make this feasible without using a single layer for every voltage domain, the components are grouped on the PCBs according to the needed supply voltages.
Large ground planes are also important to improve the return paths, for supply voltages as well as for faster signals. Ensuring that there is little to no potential difference on the ground potential at different points on the PCB prevents errors and disturbances. This is also the reason for the large share of ground connections across the FPA connector (see figure 2.16).

Multiple differential signals will be read out and need to be routed across the PCB. They are of speeds up to 8 MHz or even 128 MHz in the case of the FPGAs system clock. These traces need to be of a calculated impedance. If the traces are of different impedances, one of the two traces might suffer delay which would render the resulting differential signal unusable. As discussed in chapter 2.6.3 keeping the traces close to each other also helps in mitigating disturbances. To route the signals most optimally, two layers will be reserved entirely only for these differential signals. Having a suitable ground connection is also important, as the ground planes above and below the signal further enhance the noise resistance as a whole.
This leads to the layer stack which is formed with these considerations in mind. Figure 2.21 shows the layer stack that was decided upon. Ground planes are placed with the differential signals on layers 4 and 7 in mind. On the other side of the differential signals are the power planes placed. These are large copper areas that are connected to a lot of capacitors. This will absorb most of the disturbances, that can be expected.
By choosing a PCB stack with 10 layers, the signal routing becomes much more manageable. Especially components like the FPGA that use a ball grid array instead of other landing patterns would be far more complicated to fan out. This is further reinforced by using microvias. Microvias are a technology that uses laser etching processes to connect outer layers with the layers directly below the surface without connecting the other inner layers. In combination with the buried vias that connect only the inner layers but not the outer layers it is possible to connect components and signals without infringing on the landing patterns of adjacent components.

#	Name	Type	Thickness
	Top Overlay	Overlay	
	Top Solder	Solder Mask	0.015mm
1	Top Layer	Signal	0.03mm
	Dielectric 4	Prepreg	0.064mm
	Dielectric 10	Prepreg	0.064mm
2	Signal 1	Signal	0.03mm
	Dielectric 2	Prepreg	0.064mm
	Dielectric 12	Prepreg	0.062mm
3	GND 1	Signal	0.018mm
	Dielectric 6	Core	0.2mm
4	Signal 2	Signal	0.018mm
	Dielectric 8	Prepreg	0.055mm
	Dielectric 14	Prepreg	0.055mm
5	Power 1	Signal	0.018mm
	Dielectric 1	Core	0.2mm
6	Power 2	Signal	0.018mm
	Dielectric 15	Prepreg	0.055mm
	Dielectric 9	Prepreg	0.055mm
7	Signal 3	Signal	0.018mm
	Dielectric 7	Core	0.2mm
8	GND 2	Signal	0.018mm
	Dielectric 13	Prepreg	0.062mm
	Dielectric 3	Prepreg	0.064mm
9	Signal 4	Signal	0.03mm
	Dielectric 11	Prepreg	0.064mm
	Dielectric 5	Prepreg	0.064mm
10	Bottom Layer	Signal	0.03mm
	Bottom Solder	Solder Mask	0.015mm
	Bottom Overlay	Overlay	

Figure 2.21: PEU Layerstack - *The ten layers and their designations are visible in orange on the left side. The exact layer stack and its dimensions are coordinated with the external manufacturer. The right side details the used via types. Besides the classic through-hole via, which connects all layers, microvias and also buried vias are used.*

The FPA is a lot simpler in its circuits and will therefore not require ten layers. Its layerstack is detailed in figure 2.22. Although the circuit is relatively simple, 6 layers were chosen for this application. This allows for two very good ground layers which are beneficial for the general signal integrity and especially for the differential signals. Since a lot of the components should be placed as close as possible to the detector and signal paths should be as short as possible in general, additional layers to route across the PCB are beneficial.

Figure 2.22: FPA Layerstack - *The six layers and their designations are visible in orange on the left side. The exact layer stack and its dimensions are coordinated with the external manufacturer. The right side details the used via types. Besides the classic through-hole via, that connects all layers, microvias help in routing the shortest distances.*

2.7.3 PCB Design

Firstly the FPA layout is created. It shall house the detector and might therefore be placed in a housing during later projects. To accommodate these plans an outline for the PCB is given. The detector will be placed in the centre while the backside should ideally house no components. This would allow an ideal placement for Peltier elements or other cooling mechanisms. Due to the detector's pin assignment, this will not be possible, as most components require to be placed as close as possible to the detector's pin. By placing only the buffers on the bottom side, more than half of the area can be kept clear for a potential cooling mechanism. The finished layout can be seen in figures 2.23 and 2.24.

The PEU layout is more complex as it incorporates more components and more complicated components with small footprints or complicated landing patterns. It also distributes a total of 7 supply voltages. The power planes that are chosen for them are shown in figures 2.25 and 2.26. The power domains provide insight into the component placement. All components that are powered by 3.6V are placed close to the FPA connector, as this voltage is also needed on the FPA. The 6V input voltage is distributed across the edge strip of the PCB. This way, the generated voltages can access their respective planes where needed.

The finished layout can then be seen in figures 2.27 and 2.28.

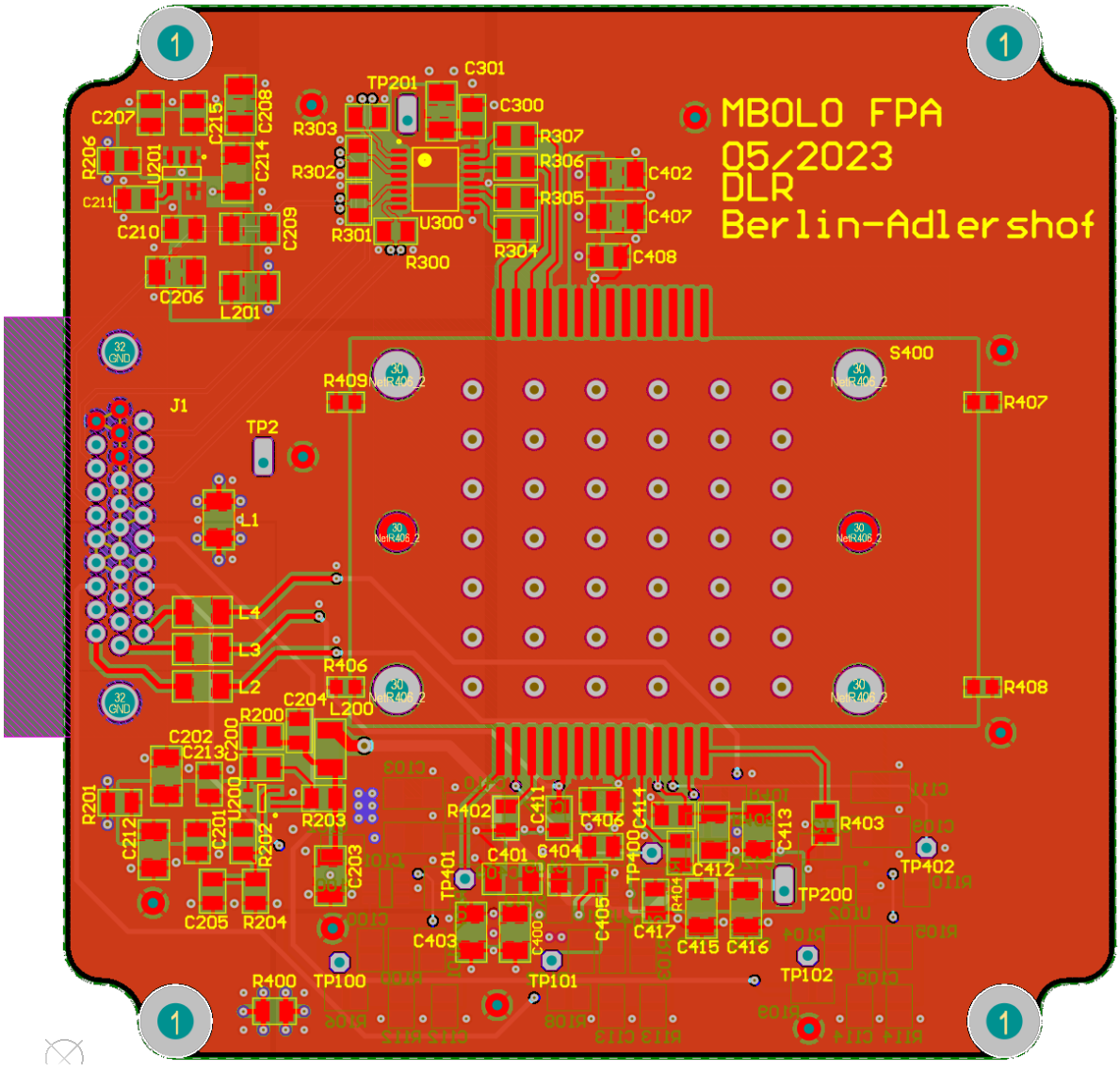


Figure 2.23: FPA Layout Topview - *The detector is placed in the center of the board a solid copper plane with several vias will provide a thermal connection for the detector. It is grounded with* 0Ω *resistors that can be adjusted.*

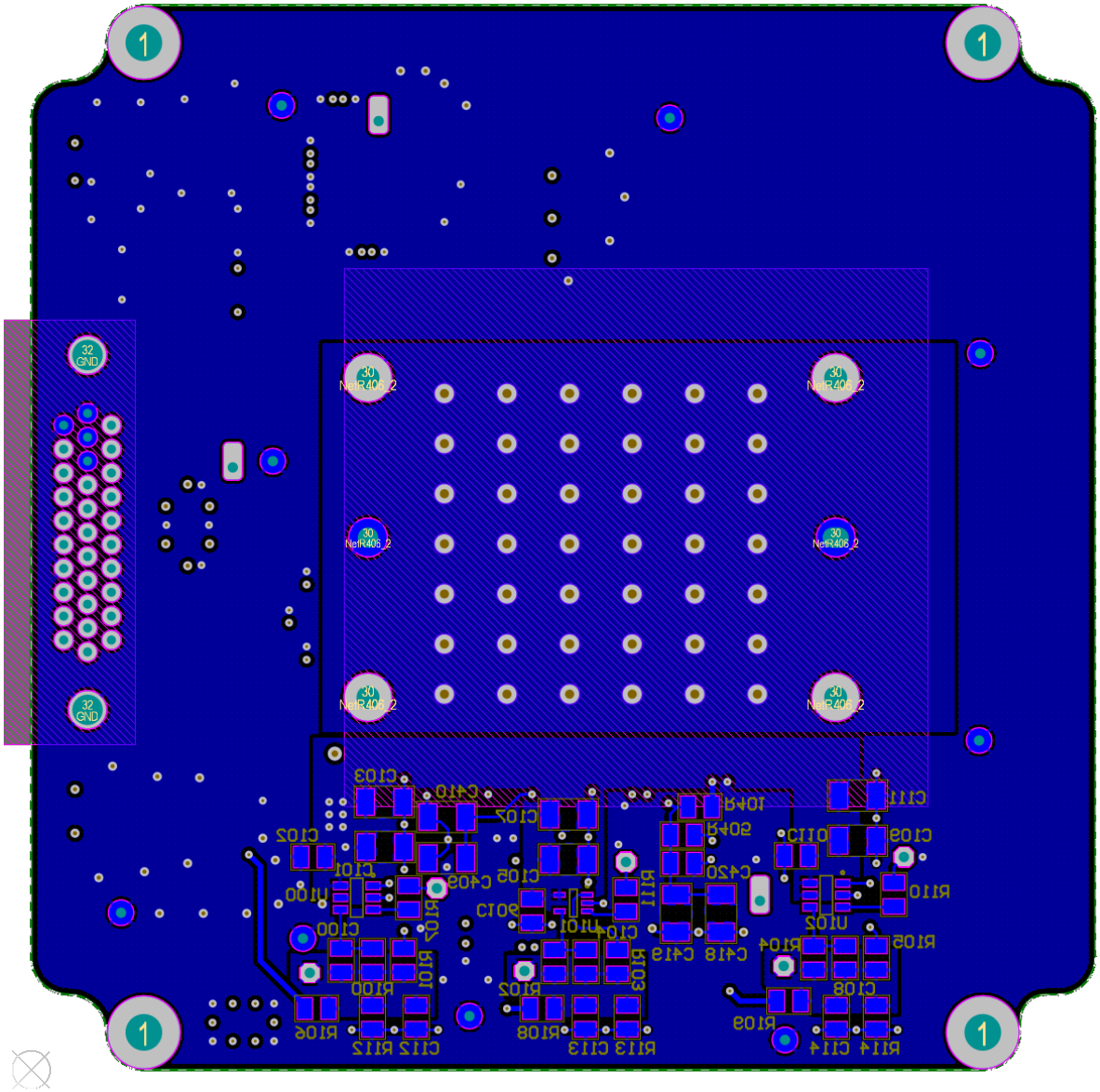


Figure 2.24: FPA Layout Bottom View - *Most of the area is kept open to allow the placement of cooling mechanisms if needed.*

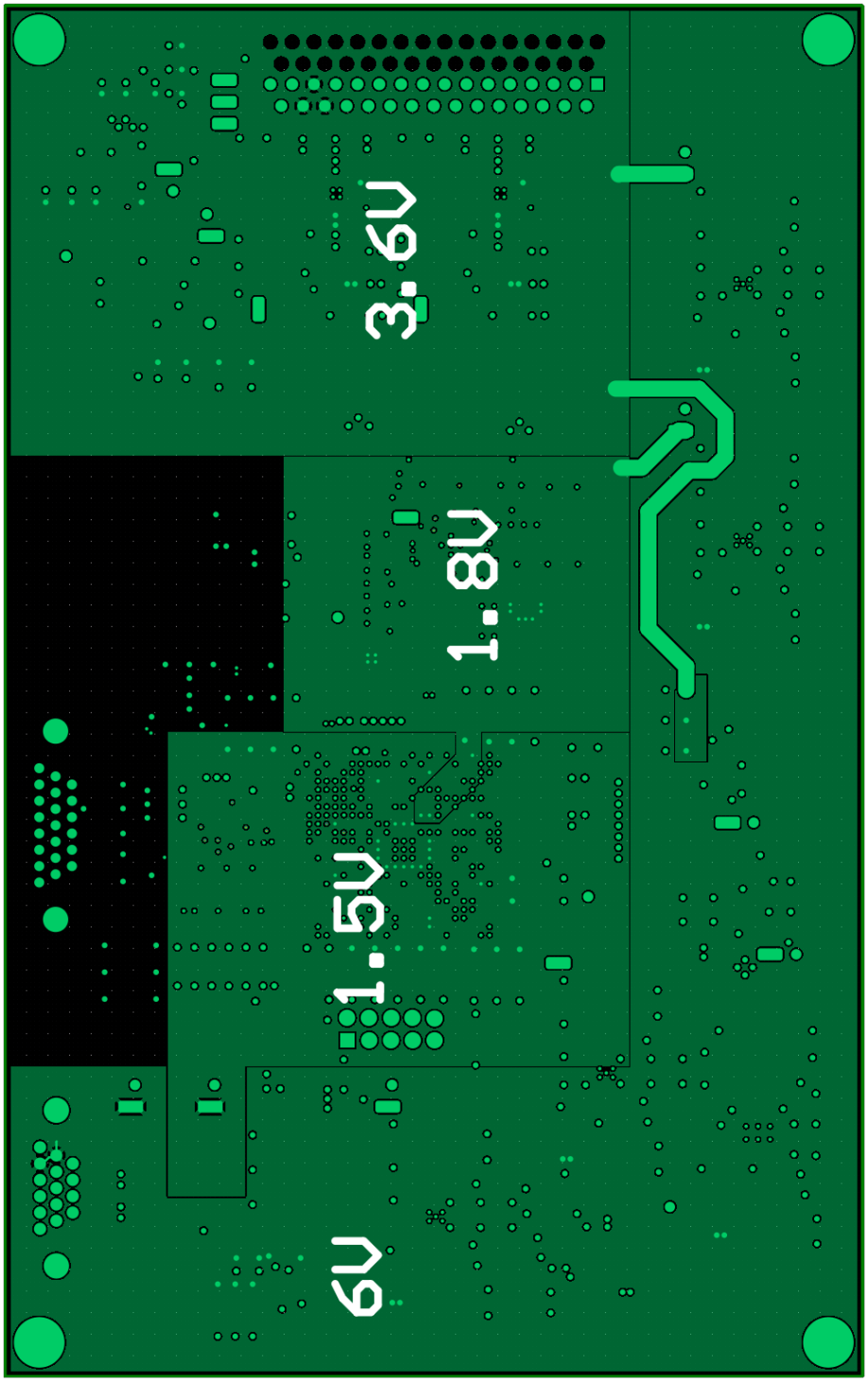


Figure 2.25: PEU first Powerplane - *The Power supply circuits are placed along the board's edge within their supply area of 6V.*

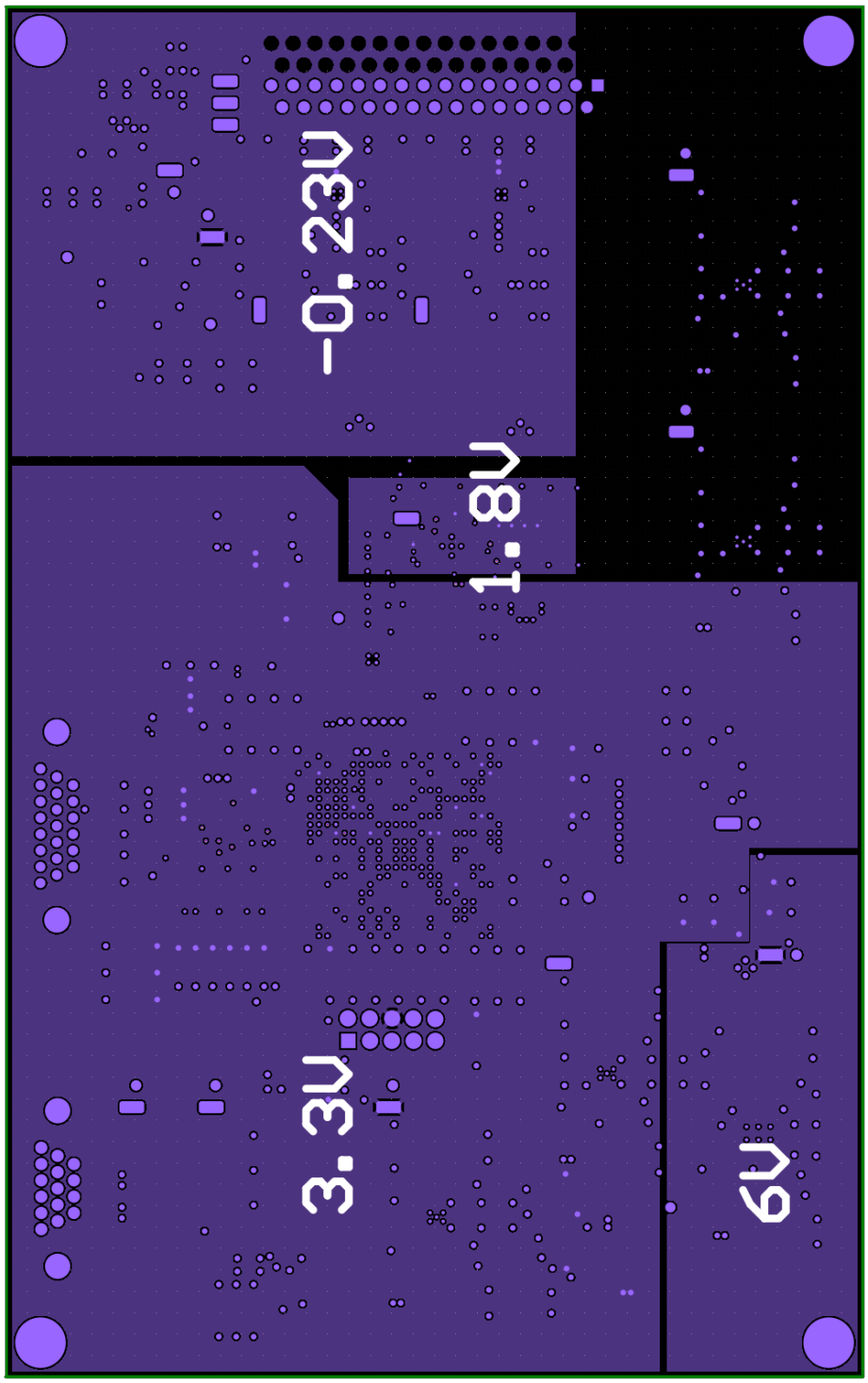


Figure 2.26: PEU second Powerplane - *The 3.3V supply voltage is mainly used for the FPGA and other digital circuits. It is kept as far away from the analog output signals as possible, to prevent any noise propagation.*

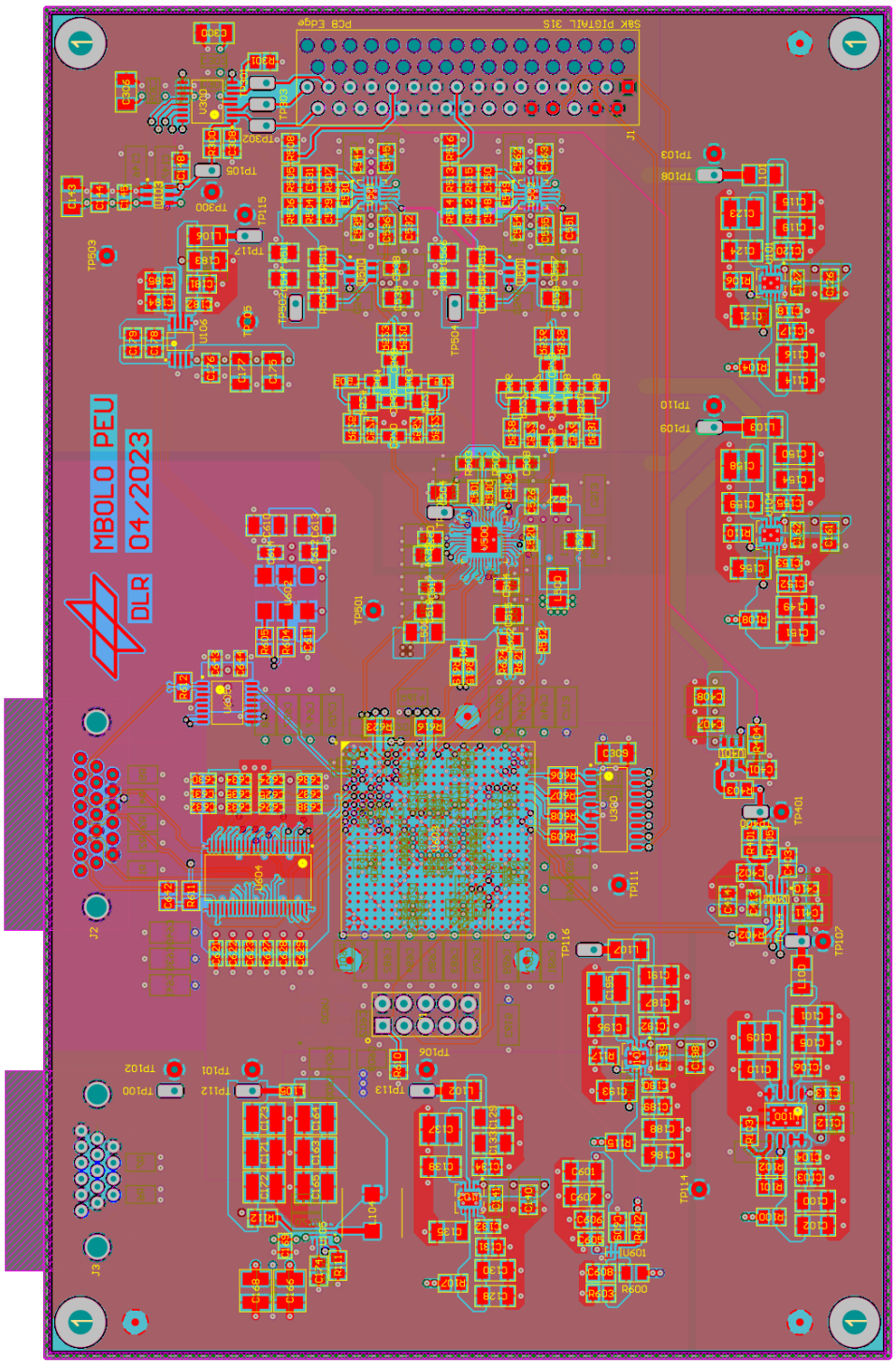


Figure 2.27: PEU Layout Topside View - *The FPA-connector is positioned on the right side. directly in front of it are the FDAs, followed by the filters and the ADC.*

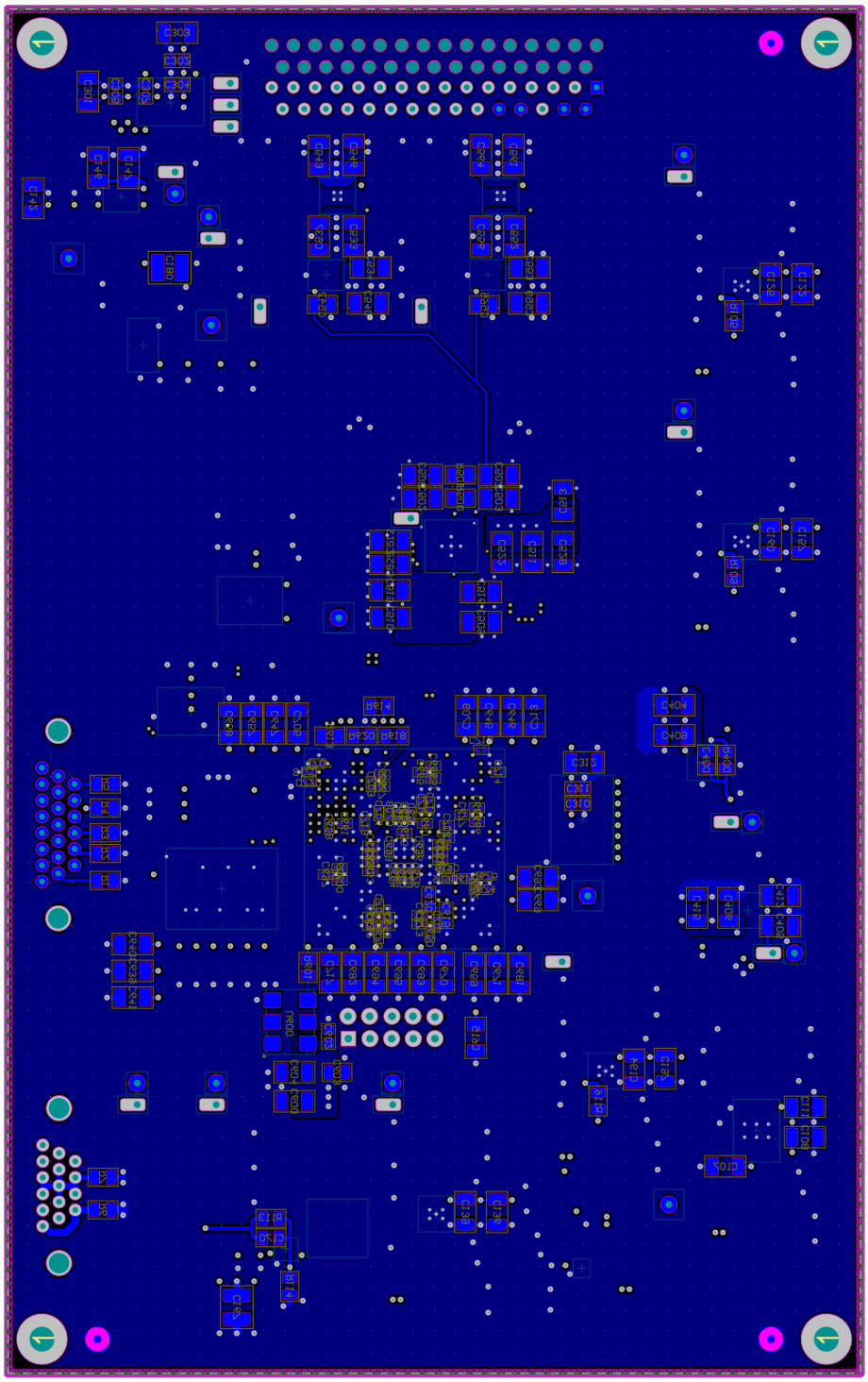


Figure 2.28: PEU Layout Bottom View - *The Bottom side is mainly used to place larger capacitors, which would use a significant area on the top side and prevent shorter signal paths.*

3 Test

After designing and manufacturing the PCBs, testing is needed to ensure performance and functionality. The first step in testing is to ensure basic functionality and prevent damage due to errors in the design or fabrication. After this, the main components are characterized to evaluate the performance of the design.

3.1 Testplan

Testing will be split into three phases. Both boards will first be tested for general functionality. It is important to ensure no mistakes have been made during design or assembly, that could harm other components. These two testing phases will be called FPA-Commissioning and PEU-Commissioning. Afterward, both boards will be tested with all components fitted during the Integrated Tests. These tests are the main tool to evaluate the design's performance and its suitability for operating the detector.

Table 3.1 shows the testplan for the FPAs commissioning. As intended, there are not a lot of components placed on the FPA. But the buffers are the first components on the video signals signal path. They provide a first insight into the design's overall performance.

Test	Description
Supply Voltage	The FPA generates a 3.3V supply voltage out of its 3.6V input voltage. With all other components disconnected by not fitted 0 Ω resistors, the FPA is powered and the generated voltage measured.
Reference Voltage	The detector uses a fixed 2.3V bias voltage that is generated from the FPA's input supply voltage of 3.6V. With all other components disconnected by not fitted 0 Ω resistors, the FPA is powered and the generated voltage measured.
Buffer Functionality	The FPA houses buffer circuits that will drive the detector's analog output signal over the connecting cable. With the supply voltages enabled, a signal is imprinted into the buffer input. By comparing it to the measured output, the buffer's functionality can be verified. This measurement also serves as a first evaluation of the signal quality.

Table 3.1: Testplan for FPA-Commisioning

Table 3.2 shows the planned tests for the PEUs commissioning. A large proportion of the PEU area is taken up by the different supply voltages. These will be tested individually, although they have been grouped in the table. Here it is much more important to properly isolate the circuits under test and monitor the current consumption at the PEUs input.

Test	Description
Supply Voltages	The PEU generates several supply voltages. All of them must be tested individually. Isolating the different modules is again achieved with fitting options. Chip beads or 0 Ω resistors at the modules out- and inputs are fitted only when functionality has been accounted for.
Reference Voltage	The DAC uses an external 3.3V reference voltage that is generated from the generated supply voltage of 3.6V. With all other components disconnected by not fitted 0 Ω resistors, the PEU is powered and the generated voltage is measured.
Watchdog	The voltage supervisor or watchdog is used to apply the power-on-reset signal needed by the FPGA. With all supply voltages working, its values are measured over time.
System Clock	The FPGA will be clocked by an external 128 MHz crystal oscillator. With all supplies in working condition, a rectangular signal with this frequency should be measurable at the oscillator output.

Table 3.2: Testplan for PEU-Commisioning

With both PCBs tested for general functionality, the main performance analysis can be done. The evaluation focuses on the detector and its output signals (see table 3.3). The detector's clock and configuration signals are transmitted with LVDS. The Power-On sequencing will also ensure, that the adjustable bias voltages can be applied according to design. Through thorough testing, the signal path for the analog video signals will be evaluated and adjusted. Filters need to be adjusted according to the surrounding circuit and the signal disturbances. Since the FPGA is not available for testing, the ADC cannot receive its required clock signals. These would be a major disturbance for the video signal, as the sampling frequency typically can be seen on the ADCs input signal. The design compensates for these disturbances with a glitch filter. This filter has to be adjusted during testing which will not be possible without the FPGA.

Test	Description
LVDS Signals	The detector's clock signals are transmitted with the LVDS driver and receiver. By imprinting a signal into the LVDS driver's input, the output of the receiver can be verified.
Power-On Sequencing	The detector requires specific sequencing at its supply and bias voltages. These timings will be verified when powering up the PEU-Board.
Analog Output Signals	The design's performance is evaluated at the detector's output signals. By imprinting a signal on the FPA, the circuit can be evaluated on the PEU. As the tests need to be done without using the FPGA, the ADC can also not be used. It requires the FPGAs control and clock signals for operation. The signal will therefore be evaluated directly at the ADCs Input.
Temperature Signal	The temperature signal is transmitted very similar to the analog video outputs. Since temperature changes very slowly, a very slow signal can be imprinted on the FPA to evaluate the performance of this module.

Table 3.3: Testplan for Integrated Tests

Testing will be done with the equipment that is available in the DLR Berlin-Adlershof laboratories. For the sake of completeness, they are summarized in table 3.4.

Device Designation	Description
Agilent E3631A	Power Supply Unit
Tektronix AFG31252	Function Generator
Keithley DMM6500	Bench Multimeter
Tektronix MSO64	Digital Oscilloscope
Tektronix RSA5103B	Real-Time Signal Analyser

Table 3.4: Testequipment

3.2 FPA-Commissioning

The first PCB to test is the FPA. To power the FPA on its own, an adapter cable was assembled. Only the GND and the input supply voltage connection are needed to power the FPA from an external power supply unit. With an input voltage of $3.6V$ only the output buffers will be powered initially. To check for short circuits or mistakes in the manufacturing process, it is suitable to monitor the input current with a multimeter. Visual inspection shows no signs of problems during fabrication or assembly. The finished board can be seen in figure 3.1 and 3.2.

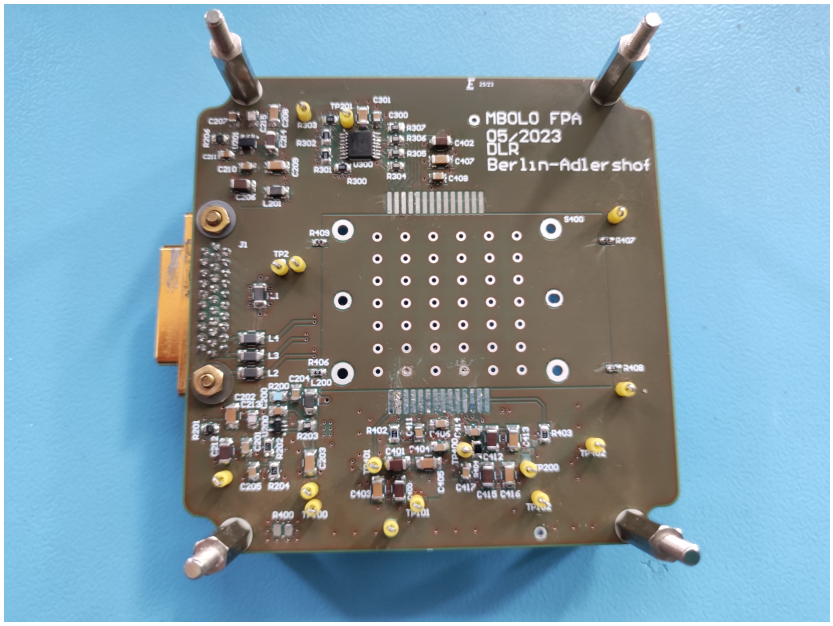


Figure 3.1: FPA Board Topside View - *The finished FPA board ready for testing. An adapter cable was put together, to enable supplying the FPA without using the PEU. View of the top side.*

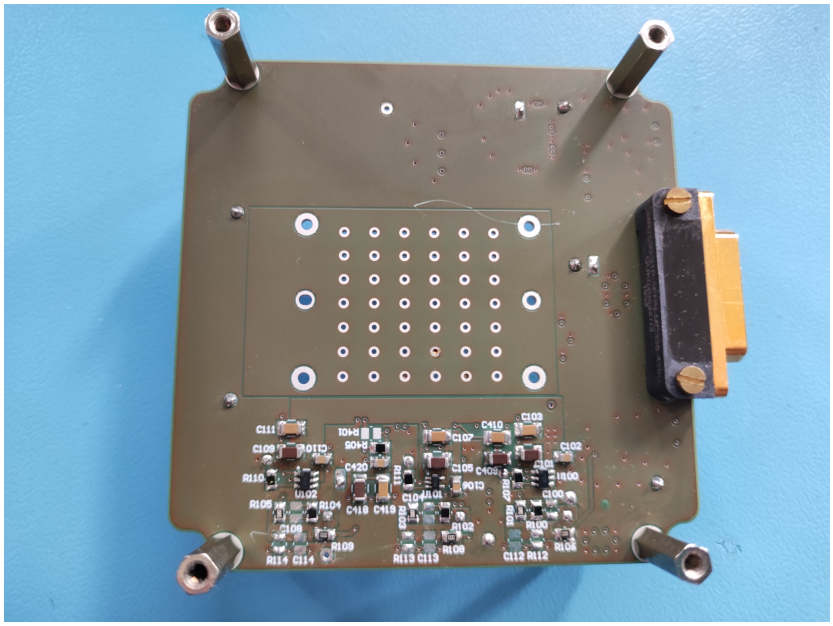


Figure 3.2: FPA Board Bottom View - *Only the buffer circuits are placed on the bottom side.*

3.2.1 Supply and Reference Voltage on the FPA

Only two voltages are generated on the FPA. Their required accuracy depends solely on the powered circuit: the sensor itself, and the control signals and clocks LVDS-receiver.

The sensor needs a simple $2.3V$ reference voltage to function. It is generated with a simple voltage divider and a buffer circuit. With the preceding $0\ \Omega$ resistor fitted, its output can be measured. Figures 3.3 and 3.4 show the results of a measurement with the bench multimeter. The histogram shows the expected Gaussian distribution. The mean value is automatically calculated at $2.331V$ which is within the expected range of deviations due to resistor tolerances. The PICO1024™ expects a value of $2.2V - 2.4V$ with root-mean-square noise of less than $100\mu V$. The standard deviation directly corresponds to the root-mean-square voltage of the noise signal. Therefore the $2.3V$ signal is within acceptable accuracy.

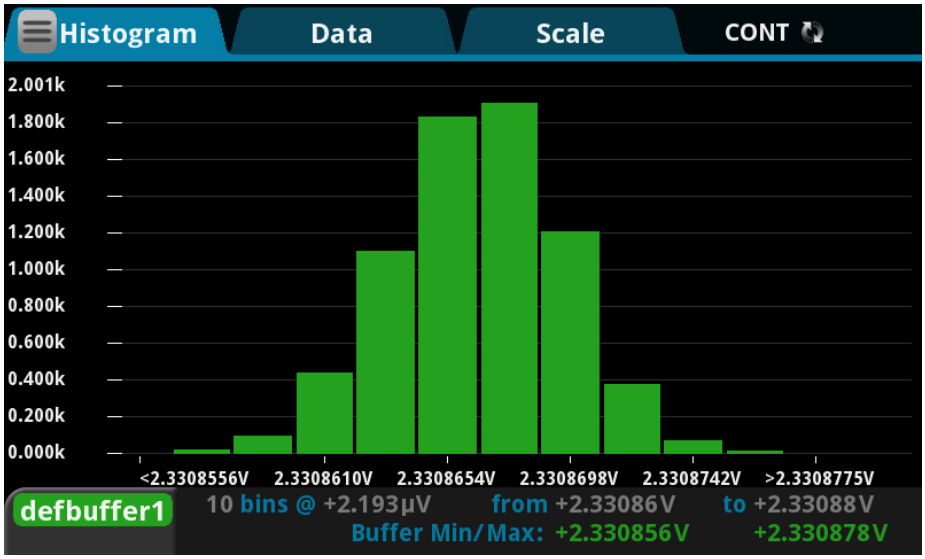


Figure 3.3: 2.3V Histogramm - *Histogram of the* $2.3V$ *voltage on a bench multimeter. The expected Gaussian distribution can be seen.*

The 3.3V supply voltage will be enabled with the fitting of another $0\ \Omega$ resistor. It will power the LVDS receiver. Figures 3.5 and 3.6 show the results of this measurement. The powered IC leaves more tolerances to its power supply so the 3.3V is suitable for operation.

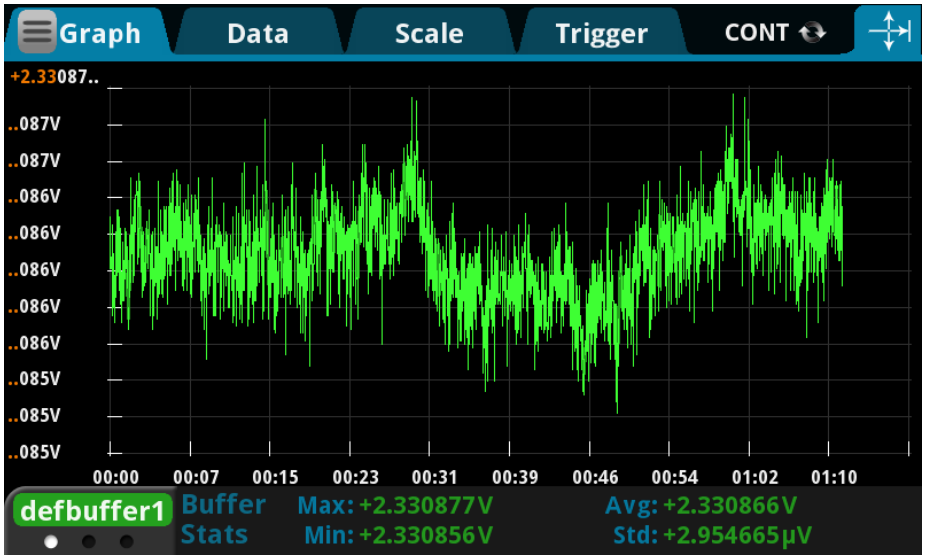


Figure 3.4: 2.3V supply over time - *Graph of the 2.3V voltage over time on a bench multimeter. The instrument also provides statistics on the bottom side of the screen.*

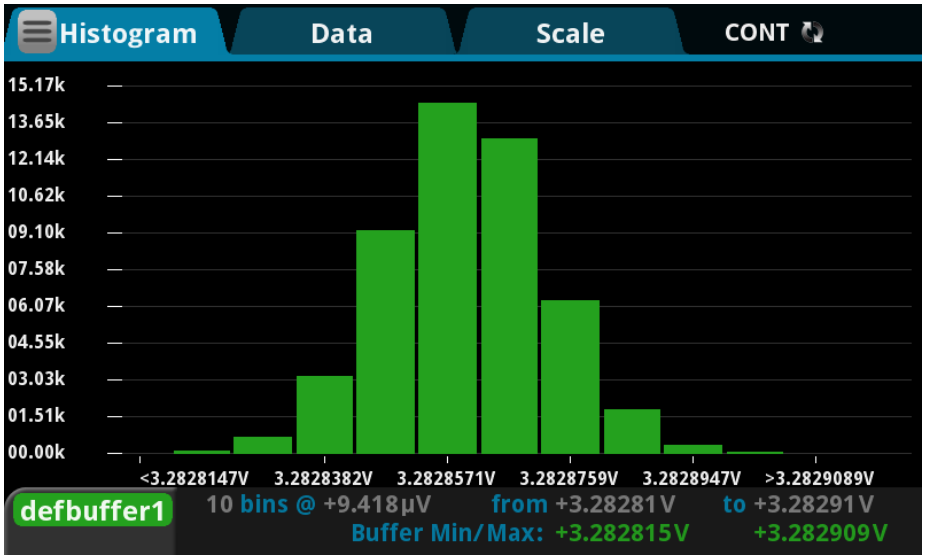


Figure 3.5: 3.3V Histogram - *Histogram of the 3.3V voltage on a bench multimeter. The expected Gaussian distribution can be seen.*

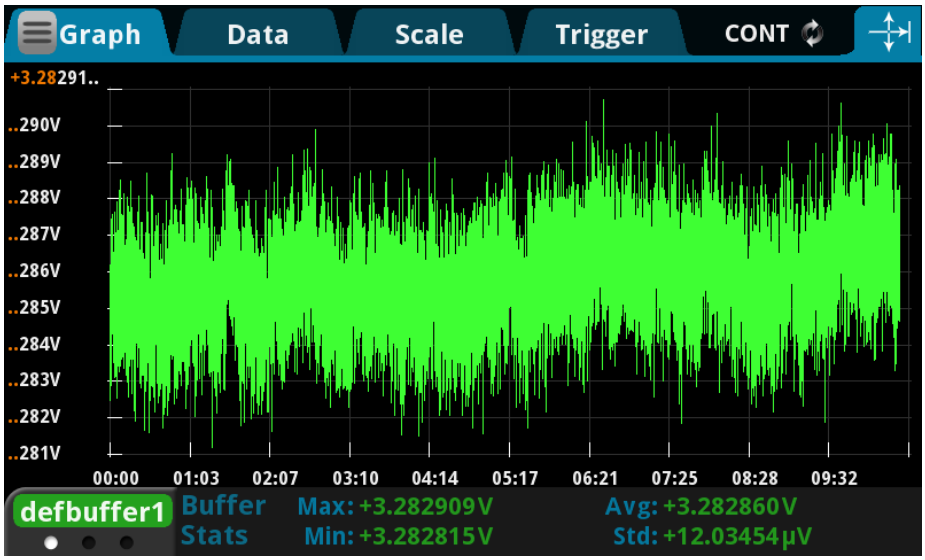


Figure 3.6: 3.3V supply over time - *Graph of the* 3.3*V voltage over time on a bench multimeter. The instrument also provides statistics on the bottom side of the screen.*

3.2.2 General Buffer functionality

The general function of the output buffers is tested next. Imprinting a fast signal with a function generator is difficult due to the connection. A coaxial cable is used and terminated with a 50 Ω resistor. This assembly provides the most accurate signal at the input of the operational amplifiers. Figure 3.7 details the signal integrity that can be reached with this method. As can be seen even with this optimized configuration, a difference in the signals is visible.

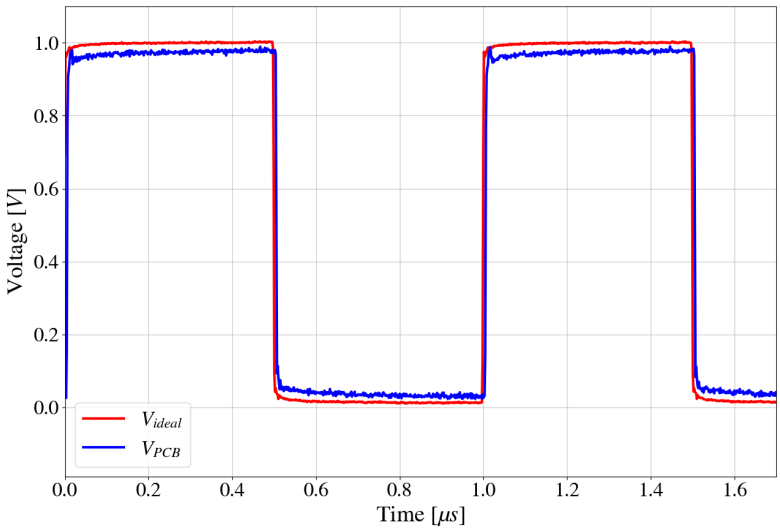


Figure 3.7: Ideal Signal - *Comparing the ideal output at the function generator and the measurable signal on the PCB shows differences that are caused by the cable and its connection.*

For testing the operational amplifiers and their transfer behavior, the resistor R106 at the buffer output is to be removed. It connects this circuit with the connector to the PEU and the traces that would follow this resistor are prone to reflection for signals within the desired bandwidth. These reflections distort the signal massively. The amplifier output is visible in figure 3.8. The input signal chosen was a 8 MHz square signal. A square wave was chosen because its steep edges are similar to the edges that are to be expected from the PICO1024™. With the masterclock at 8 MHz, the output will also change at the same frequency.

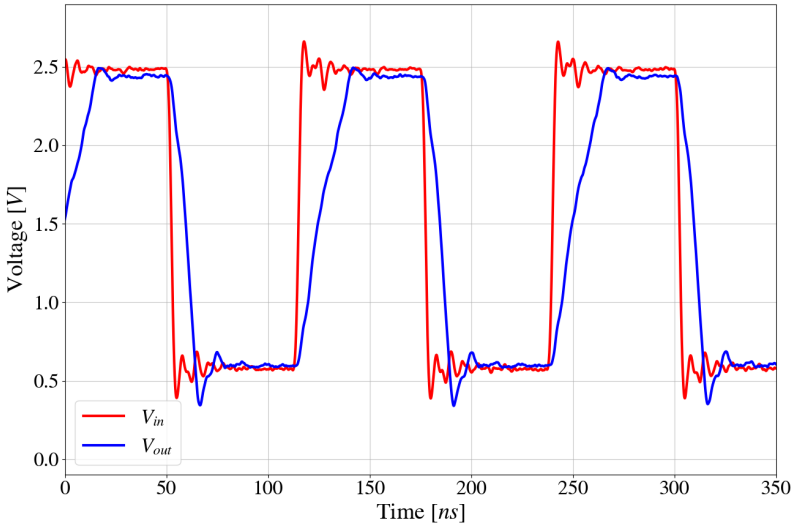


Figure 3.8: Buffer Large Signal Behaviour - *An 8 MHz signal is chosen as the stimulus. This is representative of the detector's output signal, which will be read out with the same frequency. But as the output signals will only change their amplitude at the end of the cycle (see figure 2.1), the actual frequency during operation will be half of that. The amplifiers limiting rise time is evident and a delay is fabricated in the output signal.*

A distortion of the input signal is visible. The chosen operational amplifier is defined with a very low noise behavior. Its dynamic behavior is not ideal for this application though as is evident in the rise time. The small signal behavior is much better than the large signal behavior. The first signal utilizes the entire available range of the frequency generator. Figure 3.9 shows the operational amplifiers behaviour for a small signal of $200mV$ peak-to-peak.

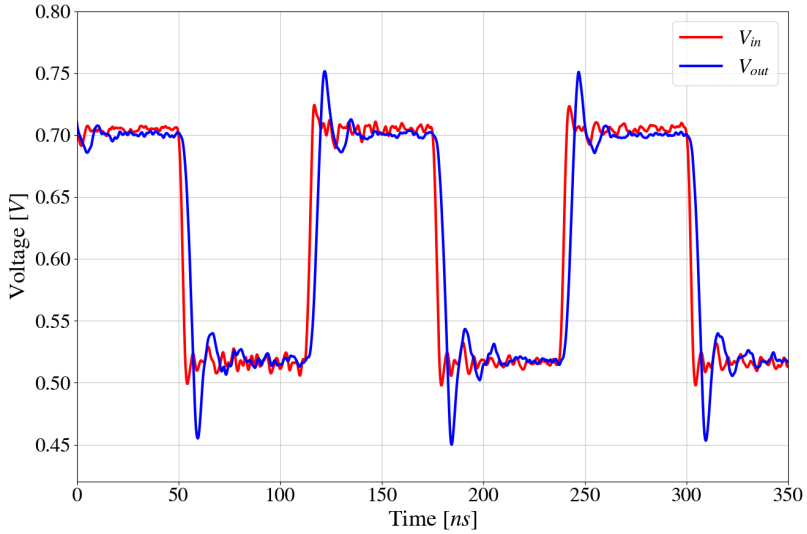


Figure 3.9: Buffer Small Signal Behaviour - *A 200mV peak-to-peak signal with the same frequencies as in figure 3.8 shows much better results. The overshoot is more prominent but the delay is mostly compensated.*

In comparison with the simulated signals in figures 2.13 and 2.12, the signal is noisier. The connection to the PCB is one reason for that. The signals behave very similarly to the simulated results which shows the design's successful implementation.
It should be noted, that the video output signal only changes at the end of the masterclock's cycle. Its real frequency is therefore half of the masterclock frequency. So the results show acceptable results above the required specifications.

3.3 PEU-Commissioning

As with the FPA, the commissioning tests shall ensure the design's general function and prevent damage to the components due to mistakes during assembly or manufacturing. Figures 3.10 and 3.11 show the assembled PCB.

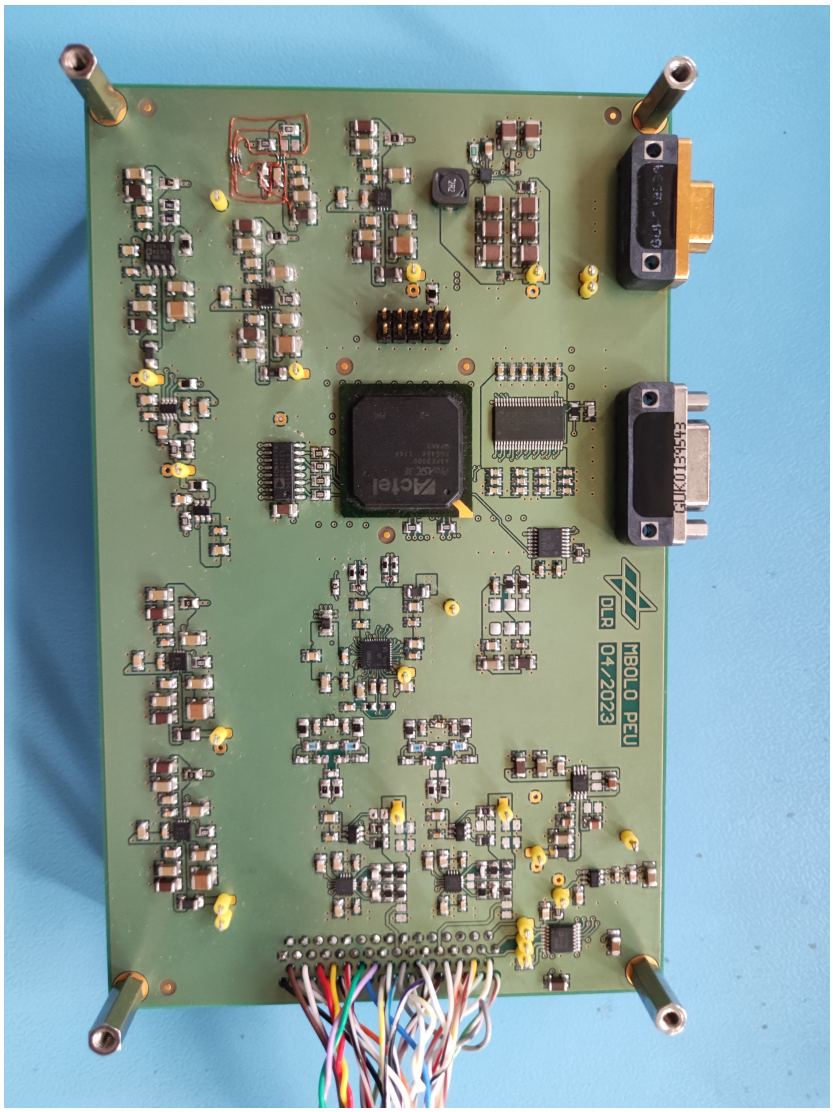


Figure 3.10: PEU board Topside View - *The FPA connector on the bottom of the figure uses a so-called pig-tail connection. This provides a lot of flexibility during testing or when handling the PCB.*

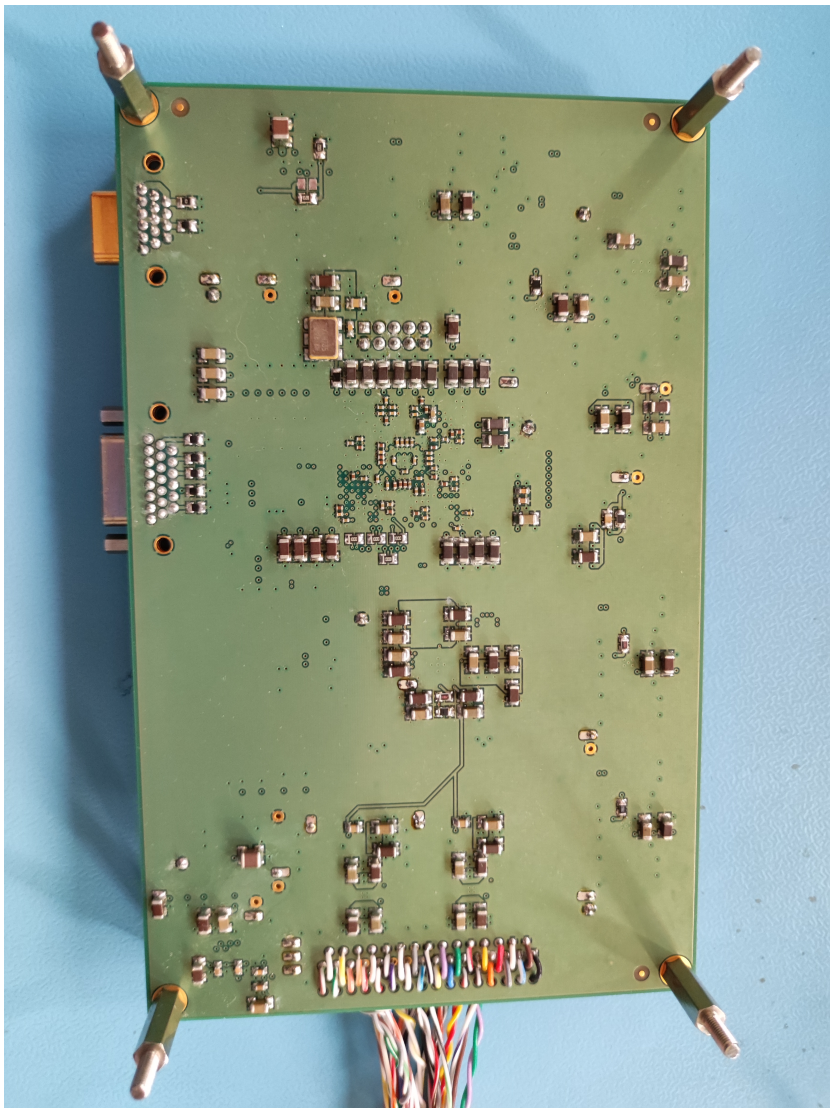
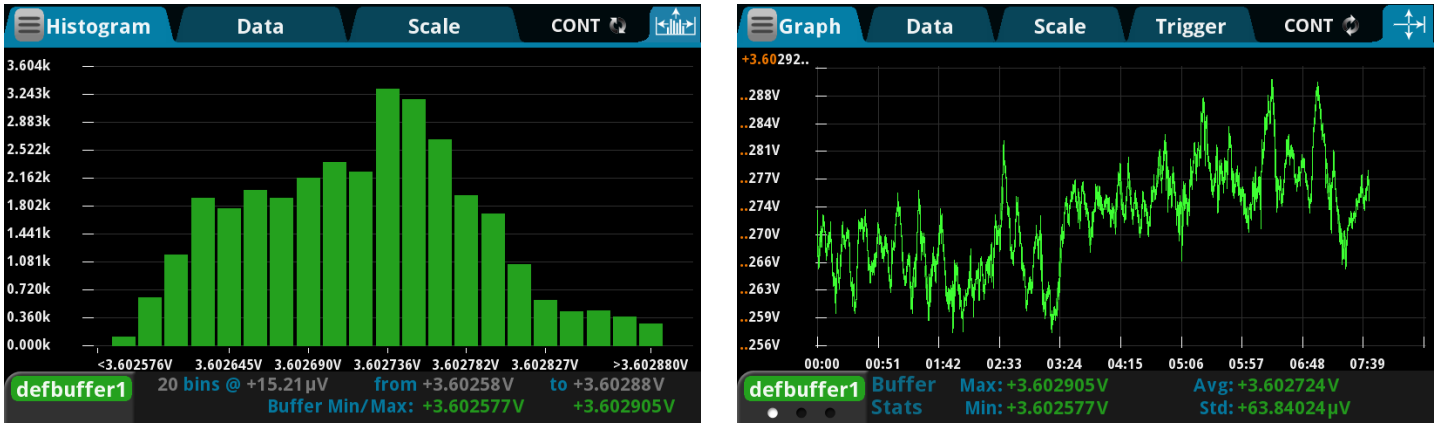


Figure 3.11: PEU board Bottom View - *The components that need to be tested are placed mostly on the top side.*

3.3.1 Supply Voltages

There are quite a few different supply voltages in use on the PEU. They are one by one checked in isolation.
Figure 3.12 shows the measurements for the 3.6V supply voltage. The measured voltage is within the expected values. The other supply voltages are also tested and the results are displayed in table 3.5 or can be seen in the appendix. The negative power supply stands out as deviating from the expected values. This is due to the larger current that two fully differential amplifiers draw compared to the single component that should be supplied by the generating circuit. This component will work out of its specified region of operation for the following tests, which will not affect further results, as its purpose is to enable the rail-to-rail operation of the FDAs.



(a) Histogram (b) Time signal

Figure 3.12: 3.6V Supply Voltage - *These images from the bench multimeter show the results from the 3.6V power supply. A standard deviation of* 63.84μV *suggests a stable supply voltage.*

Supply Voltage	Average	Standard deviation
5V Supply	4.99V	37.81µV
3.6V Supply	3.60V	63.84µV
3.3V Supply	3.30V	21.74µV
2.5V Supply	2.52V	19.04µV
1.8V Supply	1.79V	14.62µV
1.5V Supply	1.45V	17.73µV
-0.23V Supply	-152.10mV	1.46mV
3.3V Reference	3.30V	4.93µV

Table 3.5: PEU Supply Voltages during Commissioning

3.3.2 FPGA periphery

The FPGA is fitted with components that are needed for its operation. Before start-up, a single power-on reset is needed. The voltage supervisor will provide this signal. Figure 3.13 shows the resulting signal of this circuit. By varying the value of the capacitor at the components *"CT"*-pin the delay time can be adjusted. With the current assembly, the reset is asserted for approximately 520ms.

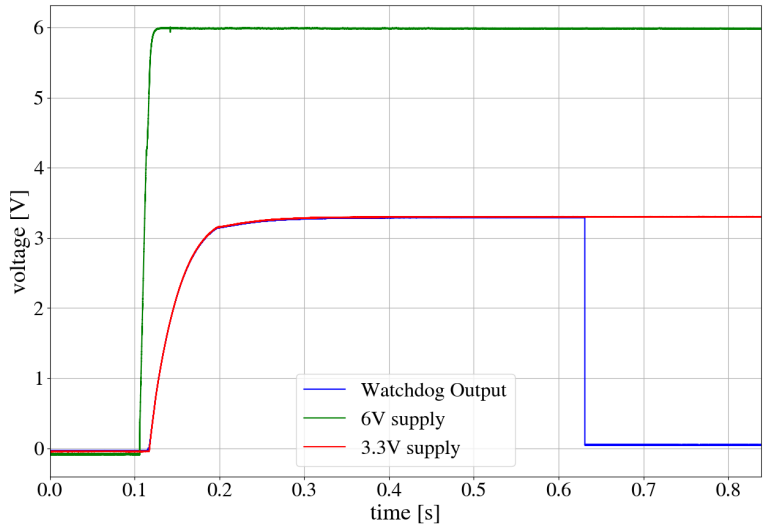


Figure 3.13: Watchdog - *The voltage supervisor asserts the FPGAs reset for an adjustable time. With a* $100nF$ *capacitor fitted, the resulting delay is roughly 520ms.*

The oscillator should generate the system clock of the FPGA, a 128MHz rectangular signal, immediately upon start-up. Figure 3.14 shows this signal. With the oscilloscope's resolution bandwidth of 1 GHz perfect edges cannot be expected. The resulting measurement shows a very good signal with the expected frequency. The rise time can be estimated at approximately 1.5 ns. This is in accordance with the ICs datasheet.

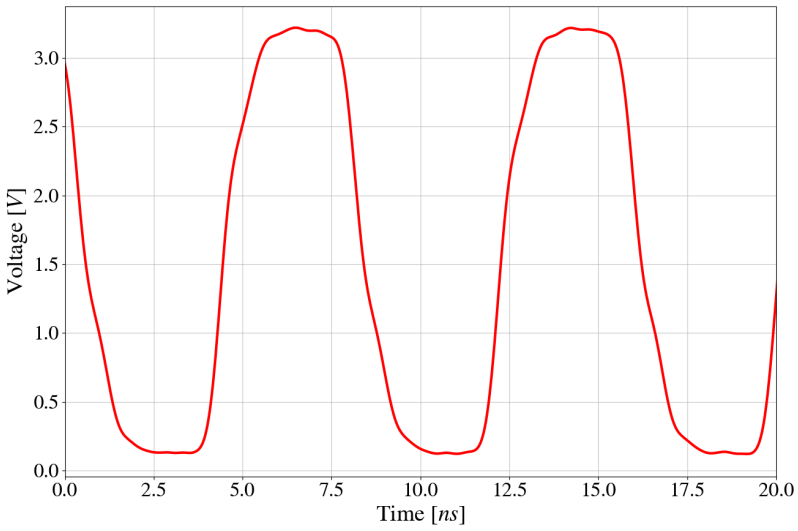


Figure 3.14: System Clock - *The oscillator provides the 128MHz system clock. The observable rise time of approximately 1.5ns complies with the datasheet's specifications.*

3.4 Integrated Tests

After general functionality is assured, the main performance analysis can be done. Its goal is to evaluate the suitability of the design for the PICO1024™. Synthesizing the FPGA is not within the scope of this thesis. So testing is done without the FPGA.

3.4.1 LVDS Driver and Receiver

Since testing is done without using the FPGA, a signal needs to be generated by a frequency generator. Contrary to the later-used FPGA, the device used has a maximum output voltage of 2.5V. The LVDS receiver will still use its supply voltage of 3.3V to generate the correct amplitude at the output. The signal is fed into the system with a coaxial cable and a 50Ω termination resistor. This leads to the least amount of interference as was tested during the FPA's commissioning.

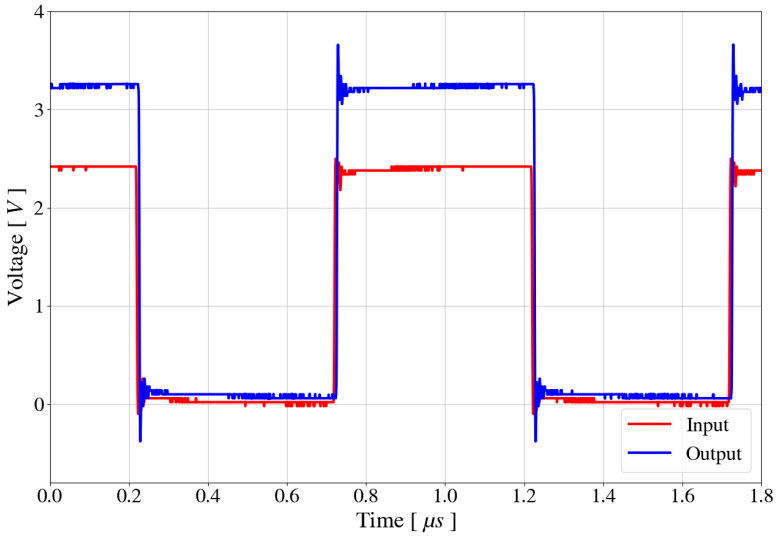


Figure 3.15: LVDS at 1MHz - A signal with a frequency of 1 MHz is fed into the LVDS driver. The function generator has a maximum output voltage of $2.5V$. The LVDS driver and receiver are powered by $3.3V$, so the output signal is as well.

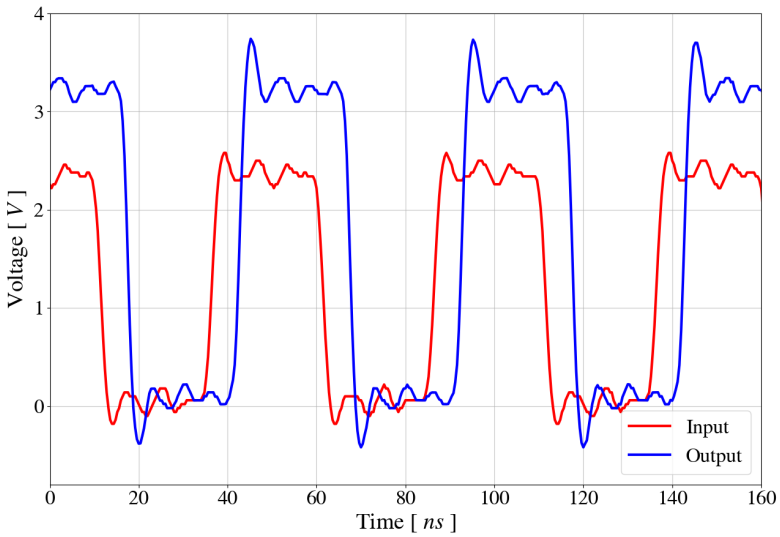


Figure 3.16: LVDS at 20 MHz - At higher frequencies, the signal suffers observable delay.

3.4.2 Power-On sequencing

The PICO1024™ needs to follow a specific power-on sequence to prevent damaging the IC. This pertains mainly to the supply and bias voltages but also the clock signals. The needed order is displayed in table 2.3. As is evident, the bias voltages "GFID" and "GSK" need to be applied after the main supply voltage but before everything else. The chosen DAC powers the outputs up to mid-scale instead of keeping them at an undefined or unwanted voltage level. When switching on the main supply voltage, they need to be applied after the PICO1024™s main supply voltage has reached a stable $3.6V$. The starting behavior of these signals can be seen in figure 3.17. As is shown, the $3.6V$ rises very slowly. This is due to the large amount of capacitors that are needed to ensure low ripple and noise on the supply. The bias voltages are asserted before they should be, according to the detector datasheet.

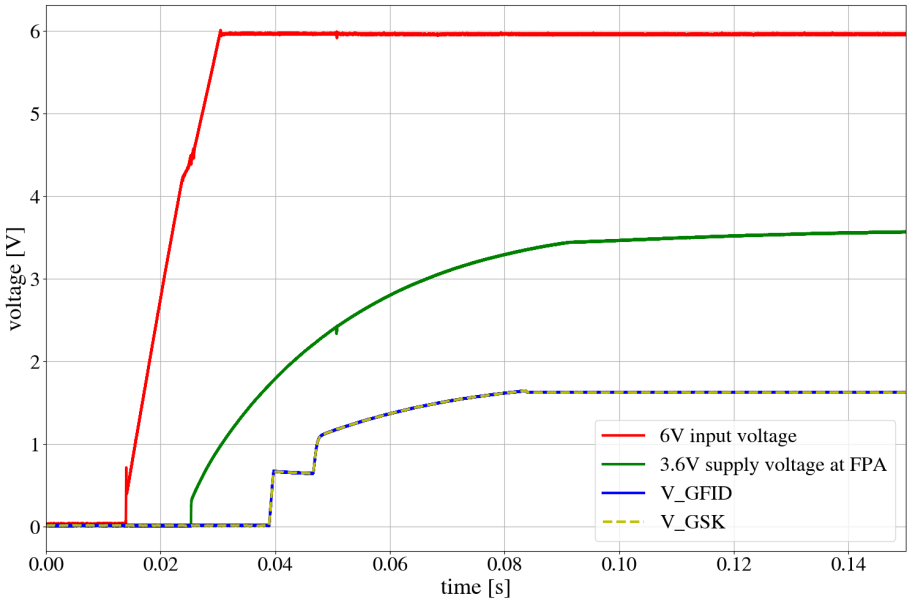


Figure 3.17: Bias Voltage at Power-On - *GFID and GSK are bias voltages that the PICO1024™ needs, after its* $3.6V$ *supply is initialised. As this figure shows, the current configuration of the DAC does not fulfill this requirement.*

This problem will be rectified when the FPGA is correctly configured. The voltage supervisor (see chapter 2.6.2) asserts the FPGAs reset signal. With the current components fitted, the FPGA will wait for $520ms$ before initializing. The corresponding DAC pins are connected to I/O pins. Their potential during the reset state can and must be adjusted. This way the FPGA can completely control the bias voltages and their timing.

3.4.3 Analog Output Signals

The analog detector output signals are essential for evaluating the performance. As was detailed in chapter 3.2.2 the buffer on the FPA is already imprinting an error on the signal. No matter how good the PEU performs, this error will still be visible. Figure 3.18 shows the result of measuring directly at the ADC inputs. An 8 MHz square wave simulates the detector's real analog output. The signal is measured with a differential probe. To even see the signal correctly, the oscilloscope's dynamic range had to be reduced dramatically. The signal still shows large inaccuracies and is not suitable for this application.
The signal amplitude is partially below zero. This is only because the differential probe subtracts two amplitudes from one another. The actual voltage is still positive. It is not centered around $0V$ because the input signal has an offset of $500mV$.

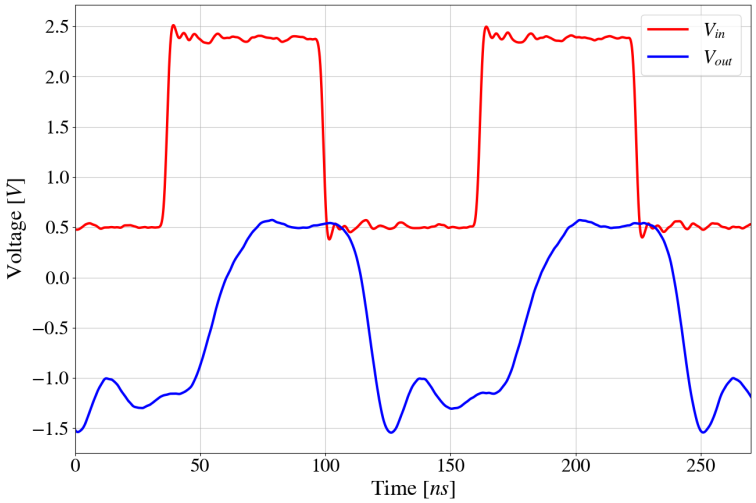


Figure 3.18: Uncorrected Signal Path - *The initial measurements show significant ringing and inaccuracies. A differential probe was used to measure* V_{out}

The filter circuit from chapter 2.5.3 is especially needed for filtering glitches and errors originating during the ADCs sampling. Without the ADC in operation, it cannot be dimensioned. Measuring without the filter connected and with the capacitor and resistors adjusted results in figure 3.19. As can be seen, the signal is much smoother, even with the oscilloscope's higher dynamic range. The slow-rising edge is the result of the buffer on the FPA and can be seen in figure 2.8. So it can be concluded, that the FDA generates a very good signal for further processing.

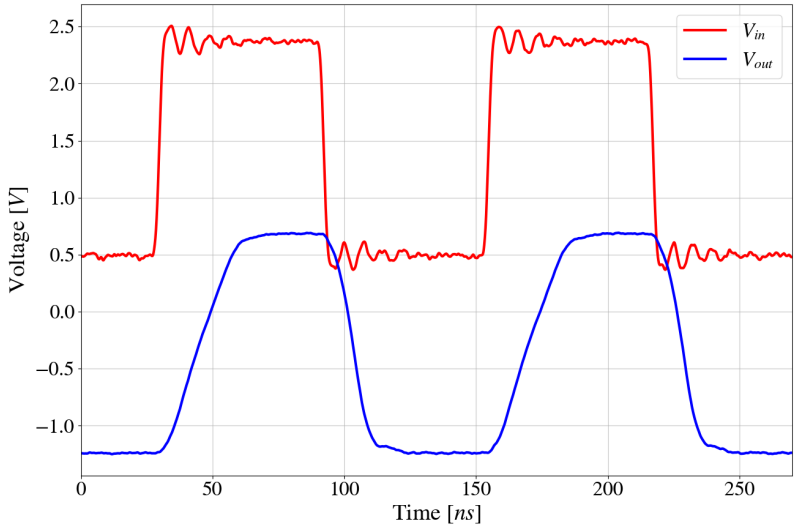


Figure 3.19: Detector Signal Path - *General reduction of capacitances results in better accuracy. The input signal is an 8 MHz square wave, that is representative of the detector's analog output signal.*

Figure 3.18 and 3.19 show the signalpaths behavior for a large amplitude of $2V$. Figure 3.20 examines the behavior for small signals with an amplitude of $200mV$. Due to the nature of the differential signal, the resulting output is calculated to a negative voltage.

3.4.4 Temperature Signal

The temperature signal will be much slower than the other output signals. Imprinting a 1 Hz sine wave simulates a slow temperature drift. Figure 3.21 shows the resulting waveform at the ADCs input. A maximum difference of $17.7mV$ between in- and output is an acceptable result.

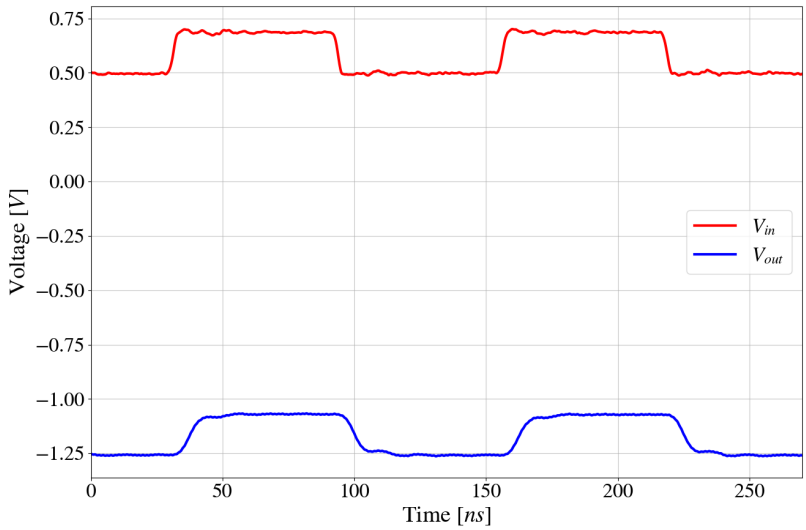


Figure 3.20: Detector Signal Path for smaller Signals - *Small signals with an amplitude of* $200mV$ *result in a differential signal below* $0V$.

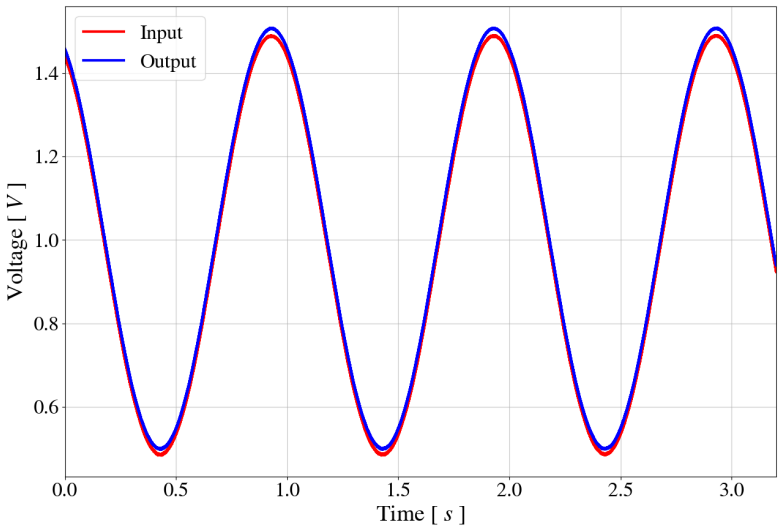


Figure 3.21: Temperature Signal - *As temperature changes are very slow, testing is done with a* $1\ Hz$ *input signal. The maximum difference between both signals is* $17.7mV$.

3.5 Noise Analysis

Even with no signal generated by the detector, the PEU, its components, and its design may influence the ADC's input. This noise can be detrimental to the signal integrity during operation. To evaluate this noise, a frequency analyzer is used. with no signal imprinted at the FPA's input, only the noise generated by the boards is measured. The supply voltages are switched on. This way, the surrounding noise sources are active. For this measurement, the frequency analyzer is used with a differential probe. The data is then transformed into the power spectral density. This is achieved with *numpy's periodogram*-function. The power spectral density (PSD) provides insight into the noise power at specific frequencies. The results can be seen in figure 3.22 and 3.23.

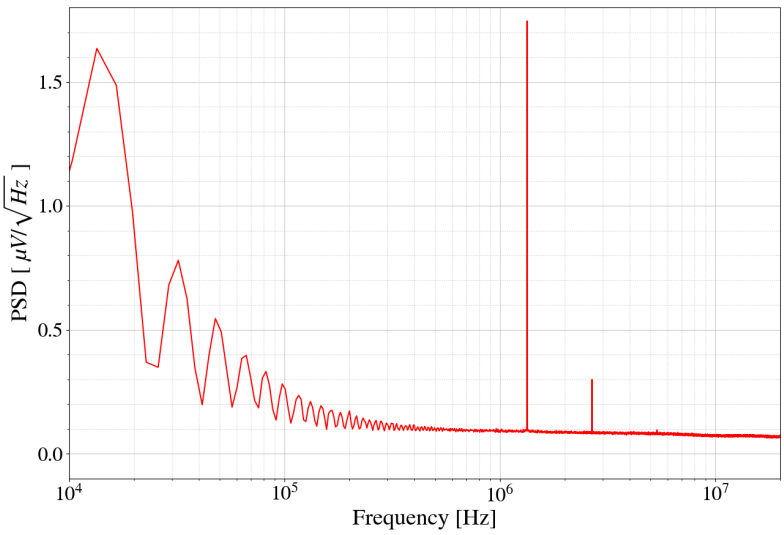


Figure 3.22: Power Spectral Density of the Signalpaths Noise - *The expected signal frequencies are at and above* 8 MHz. *At these ranges, the electronics noise is mostly below* 100 $nV/\sqrt{Hz}$.

While evaluating these results, the method of measurement has to be taken into account. The differential probe is active and will by itself generate a small error. Without connecting the probe to the PCB, the power density spectrum in figure 3.24 is measured. This curve is very similar to the data calculated in figure 3.22. Figure 3.25 plots both data arrays together. It is evident, that most of the measured noise is purely generated by the probe and the measuring apparatus. Two peaks around 2 MHz are generated by a USB port on the frequency analyzer and are amplified by the PCB. This is confirmed by disconnecting the USB-Port which eliminates these peaks.

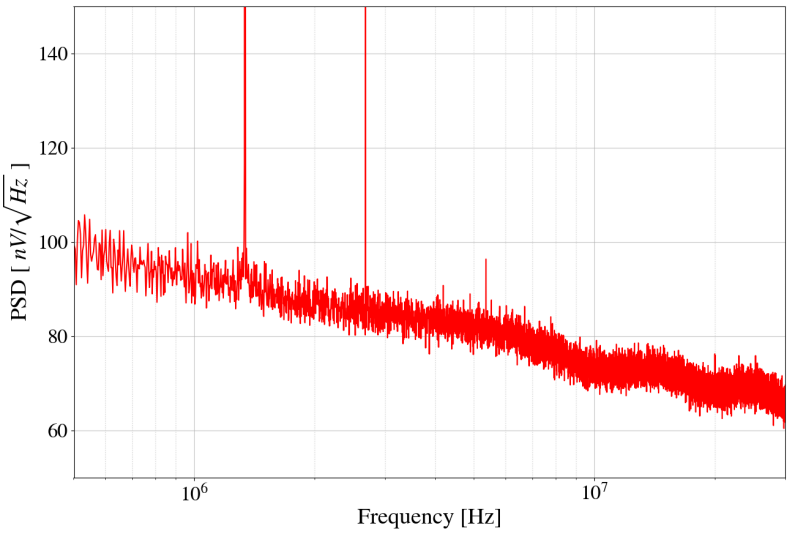


Figure 3.23: Detailled View of the PSD of the Signalpaths Noise - *The detectors output signal will change at* 8 MHz. *The noise power is at this frequency at* 74 $nV/\sqrt{Hz}$.

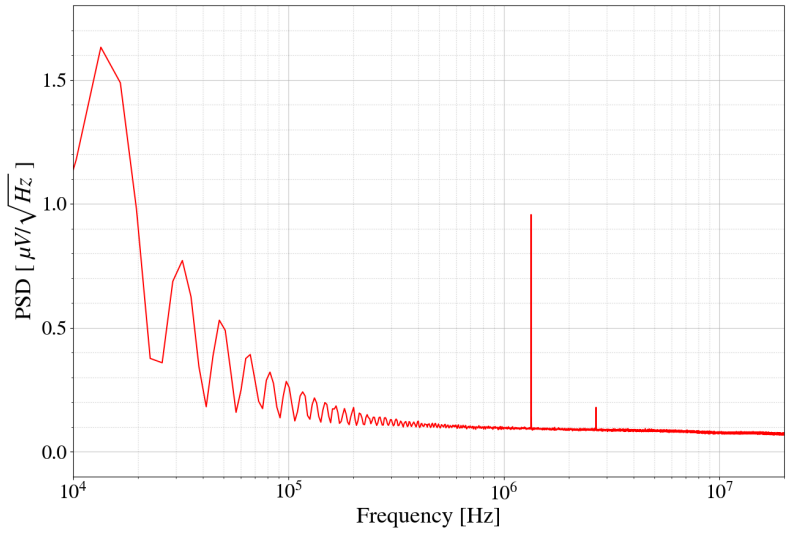


Figure 3.24: Noise PSD of the used Probe - *The probe is shorted and the resulting spectrum shows only the noise with no component or electronics connected.*

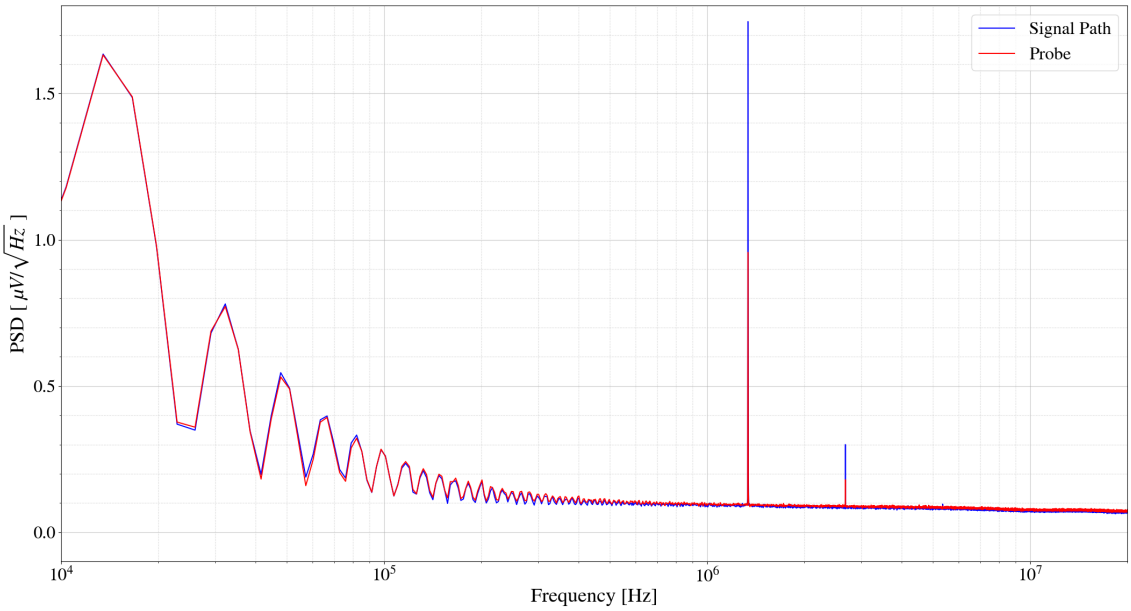


Figure 3.25: Comparision of PSD - *Comparing the results from both the probe and the electronic design shows their similarity. Most of the noise is identical, but the noise at the peak's frequencies is amplified.*

3.5.1 Noise on the power supply

The detector has very rigid requirements for its power supplies noise power spectral density. Figure 3.26 is given in the detector datasheet to indicate the expected values. The supply voltage is measured with the target value of $20nV\ /\ \sqrt{Hz}$ at frequencies of $1kHz$ in mind.

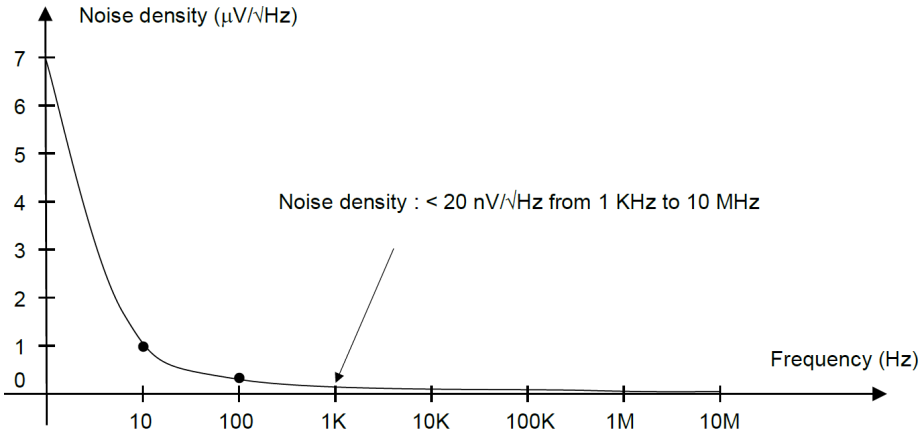


Figure 3.26: Noise Density Requirement [2] - *This diagram is provided by the detectors datasheet and defines the characteristic threshold of* $20nV\ /\ \sqrt{Hz}$.

The *numpy* library for Python allows for calculating the power spectral density with the function *periodogram*. The results are displayed in figure 3.27. As is evident, the calculated spectrum displays noise density values above the required threshold. This result may be flawed though, as a lot of noise is caused by the probe and the nonideal measurement setup. To put the acquired results into perspective, another measurement is done, where no circuit is connected. This way, only the noise not generated on the PCBs is included. With the same calculation done, the results are compared in figure 3.28.

The resulting noise is very similar to the result for measuring the probe's influence. The data is corrected by the probe noise in figure 3.29. The requirement was not met. But the results besides the peaks are very promising. The general noise level is low and almost within the very strict requirement. The results from figure 3.25 and figure 3.31 show that their noise level is mostly influenced by the probe and the method of measurement.
The origin of the large peaks in figure 3.27 could not be found. The peaks follow the typical pattern for harmonic signals and so it is speculated that they stem from the same source. Further testing is needed to find and eliminate it which will improve the test results towards acceptable levels.

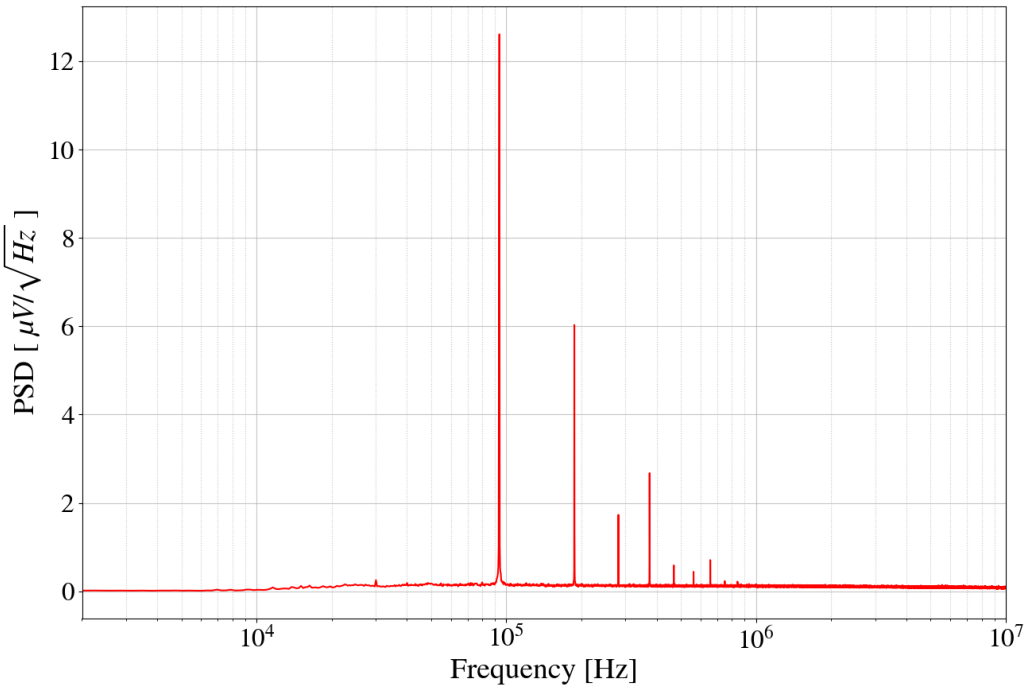


Figure 3.27: Supply Voltage Noise Density - *The calculated power spectral density of the 3.6V supply voltage. A large noise influence at* 93.8 kHz *is visible. Its source could not be found.*

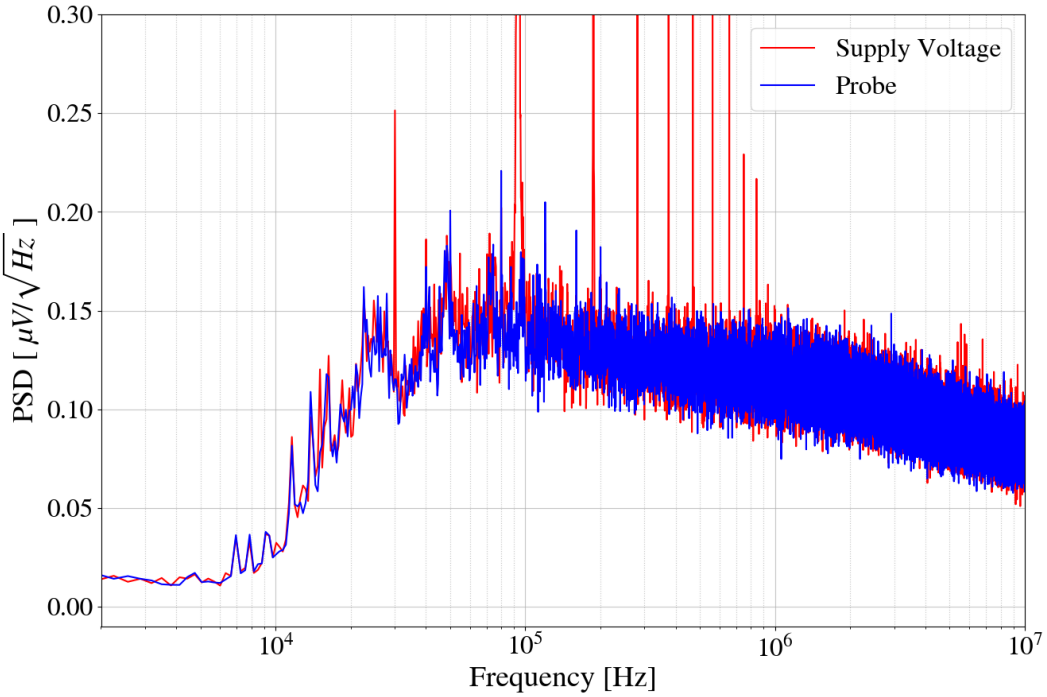


Figure 3.28: Noise PSD Comparison - *Comparing the measured noise with the probe noise shows, that the noise that is not in these prominent peaks is mostly caused by the probe.*

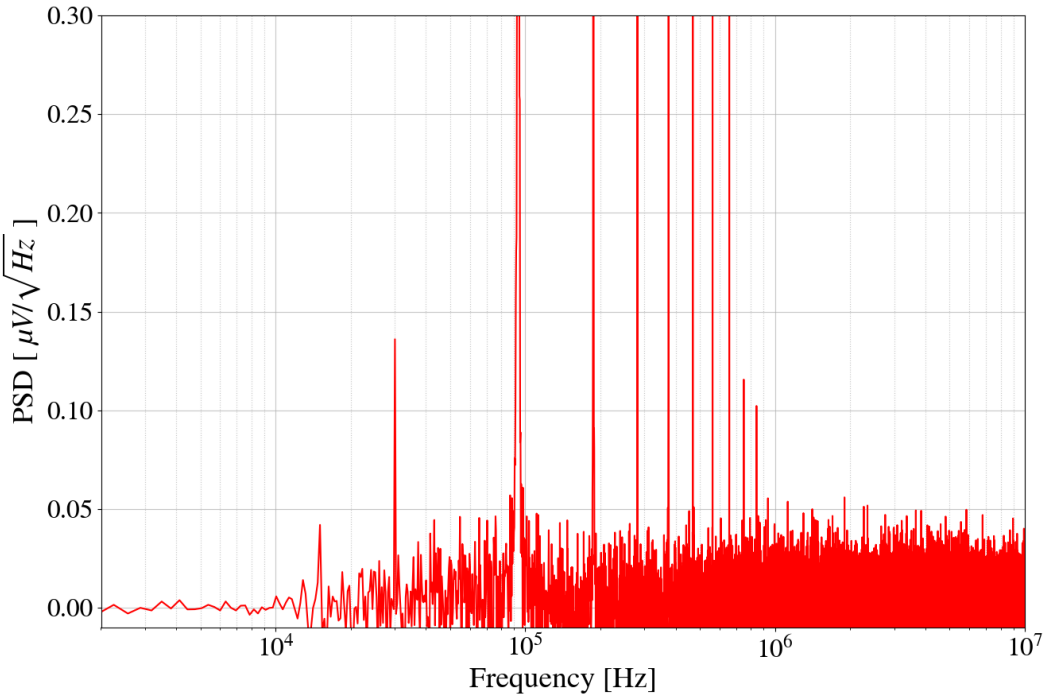


Figure 3.29: Probe Corrected Noise PSD - *This detailed view of the noise is corrected by subtracting the influence of the probe. The peak's maximum* 12.47 μV / $\sqrt{Hz}$ *is cut off to show that the result at other frequencies is on average just at the required specifications.*

3.6 Testing with FPGA

Close to the end of the allotted editing period, a simple build is finished for the FPGA. This allows testing the clock signals and the LVDS path. Three output pins generate clock signals as required in chapter 2.1.1. The masterclock (MC) is an 8 MHz rectangular signal. All other signals change their state only at the masterclock's rising edge. Figure 3.30 shows a cycle for the INT signal.

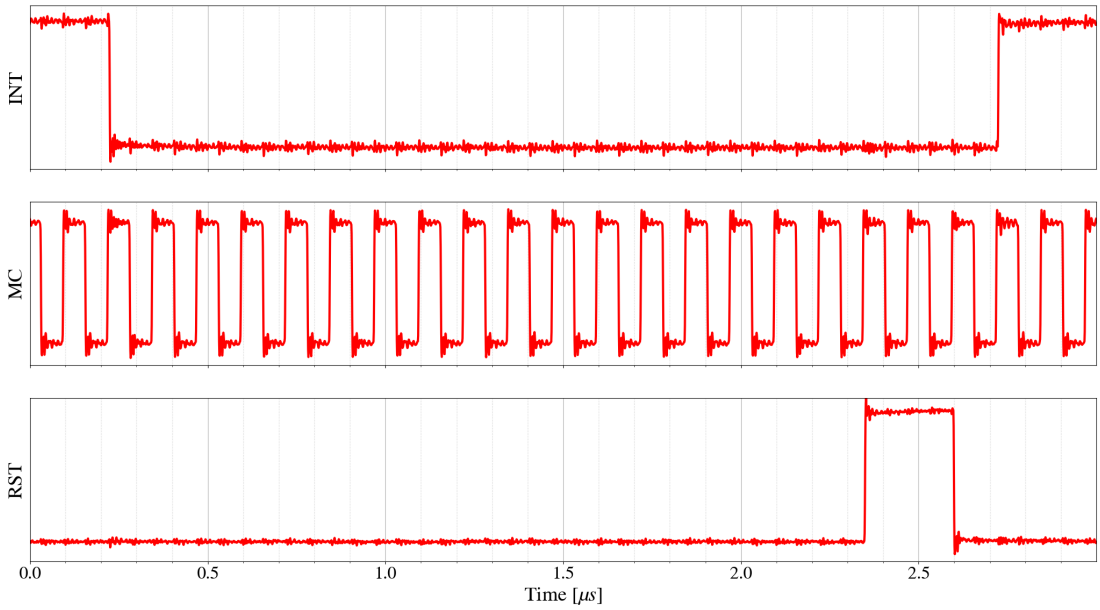


Figure 3.30: Clock Signals - *The clock signals as defined in chapter 2.1.1 are clearly visible.*

The ADC's input signal is influenced by the ADC sampling. With the sample clock at the FPGA activated a spectrum analysis shows this disturbance very clearly in figure 3.31. The marker "MR" is placed at the ADCs sample frequency of 8 MHz. The signals harmonic waves at multiples of 8 MHz can also be seen. Notable is the difference between the two data traces. The blue trace is the measurement of the circuit while the yellow traces show the probe noise only. The circuit's noise spectrum is only marginally larger than the probe noise itself. This is interpreted as very good noise behavior.

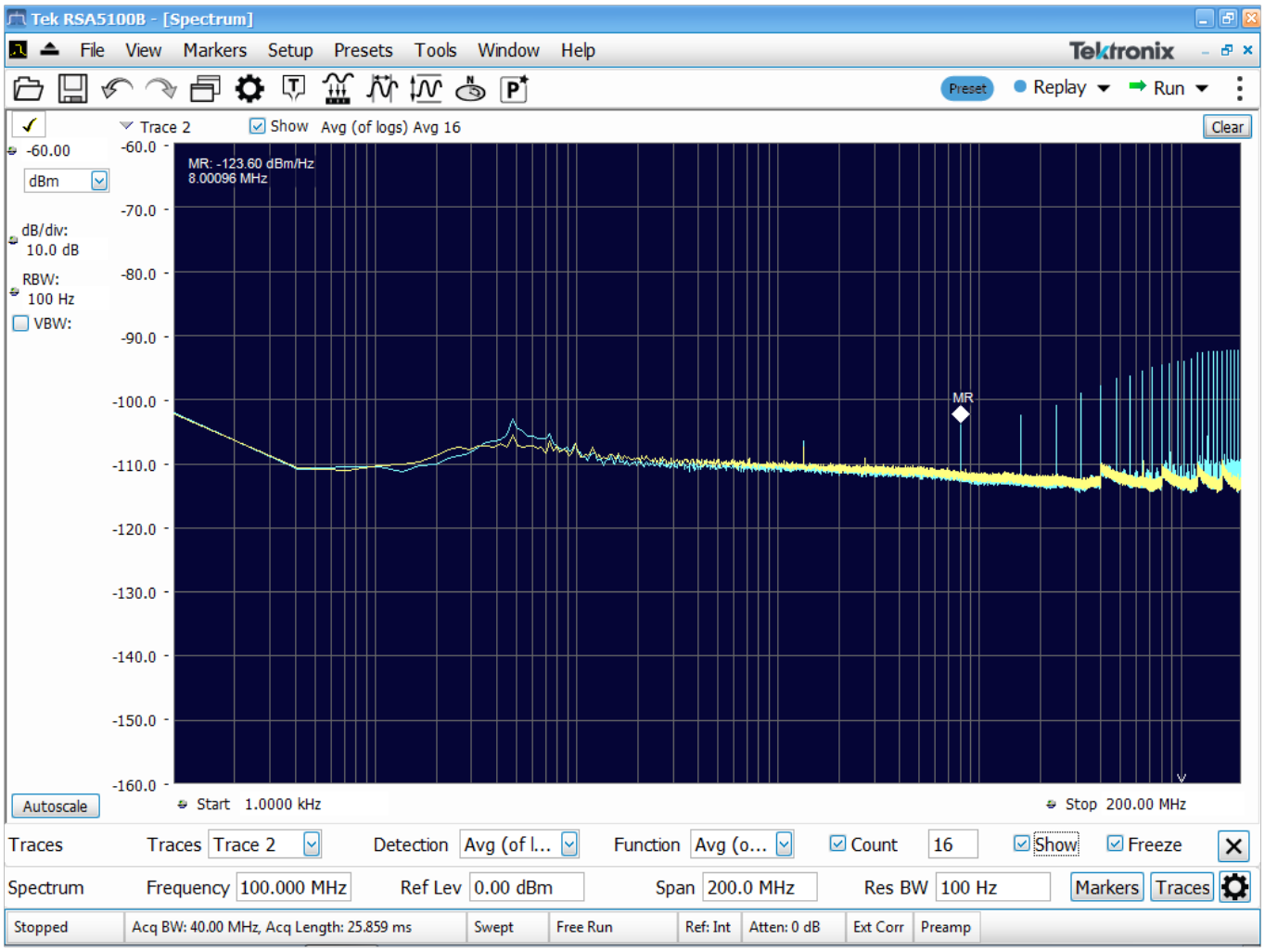


Figure 3.31: Sample Frequencies on the ADCs Input - *The yellow curve derives from measuring only the probe while the blue line is the measurement resulting from the circuit. This is a screenshot of the frequency analyzer.*

4 Conclusion

In this thesis, the frontend electronics for a microbolometer detector were designed and tested. The critical design requirements were identified and fulfilled with application-specific circuits and components. The detector and the other components were distributed among two PCB designs. The first PCB is the FPA. it houses the microbolometer sensor and the components that must be placed directly in its proximity. The second board is the PEU and it consists of the FPGA, voltage conversion circuits, and the ADCs with their respective required circuits.

A complete layout design was created for both PCBs. It takes signal integrity into account and distributes the power domains efficiently across the PCB areas. The completed designs were then manufactured and the components fitted. Fitting options to facilitate easy commissioning were implemented and used for the first function tests.

Tests were conducted to evaluate the performance of the design. Commissioning tests first ensured general functionality. Then the detector's output signals were tested. An appropriate test signal was imprinted on the FPA and the resulting output was measured on the PEU. After adjusting passive components along the signal path the measurements showed good results. The measurable noise power is only slightly higher than the probe's noise alone while the signals were swung in at the intended sampling point.
The noise on the detector supply is close to the required levels but suffers from an unknown disturbance at 93.8 kHz. The source of this noise influence could not be identified.

As expected, the power-on-sequencing is not in compliance with the detector's requirements. This is intended, as it depends on the FPGA configuration which was not implemented within this thesis. However, the tools and configuration signals are provided.
The implemented LVDS enables high-speed connections for the clock signals and shows very good transfer characteristics.

4.1 Outlook

The next step should be the implementation of the FPGA and its full functionality. Testing with the FPGA operating and therefore with the ADCs configured will provide further insight into the signal integrity. Chapter 3.6 provides some information on the results to be expected but the ADCs outgoing signals are yet to be evaluated.
As mentioned in chapter 3.4.2 when implementing the FPGA special consideration should be taken to the I/O-pins state during reset phases. This will directly influence the bias signals and the power-on sequence for the detector.

The implemented design reaches frame rates around 20 Hz. Future designs might aspire to faster frame rates which are possible with the chosen sensor. Switching from the 2-output mode to the 4-output mode alone would improve the frame rate by a factor of 2, but it would require additional circuits and analog-to-digital converters. The 2-output mode allows for frequencies of up to 60 Hz by increasing the masterclock frequency. Tests with the FPA have shown, that the used buffer possesses a limited rise time. Especially at higher amplitudes, this would disturb the signal immensely. To evaluate the performance of the detector at higher speeds, this component should be replaced and the surrounding circuits' dimensioning adjusted accordingly.

To adapt this design for space applications, additional work is needed. Most of the components have direct equivalents of space-grade certification. These are rated for different radiation and temperature levels that might destroy or disrupt conventional commercial components. Usually, these space-grade components have larger or at least different landing patterns. Therefore both PCBs will have to be adjusted.

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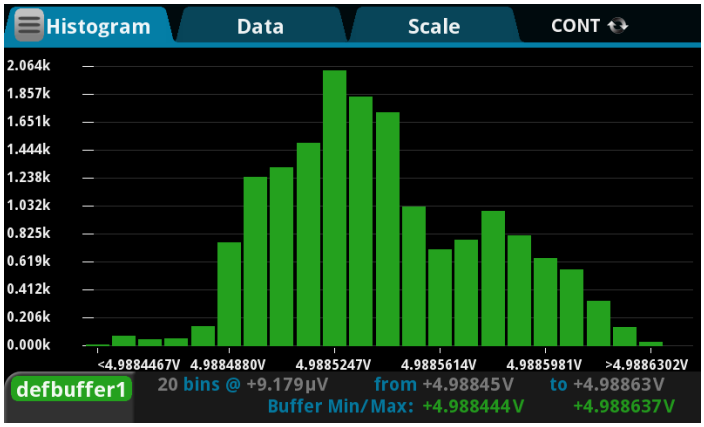
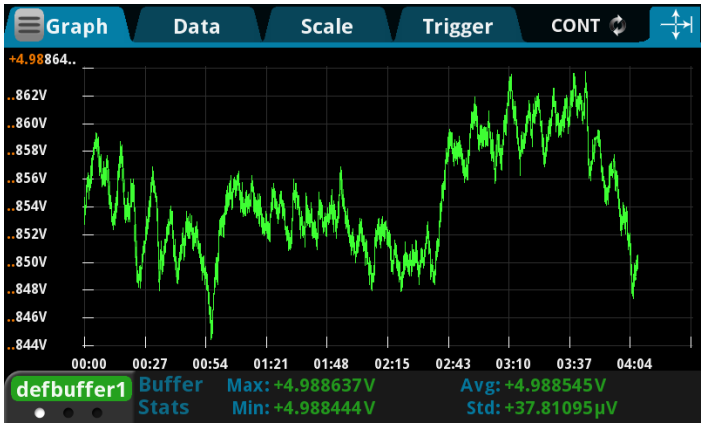
Appendix

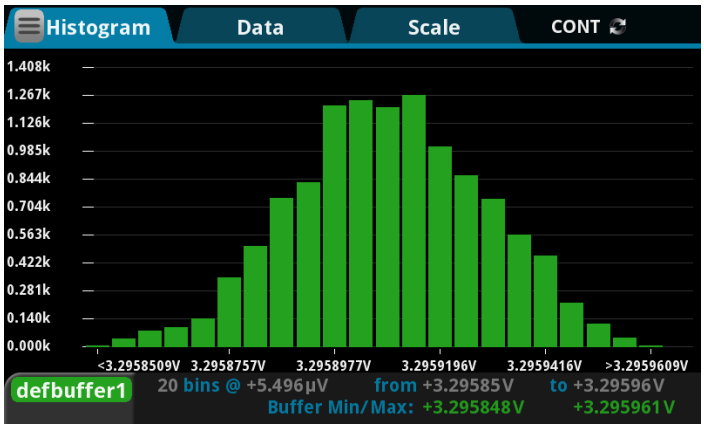


(a) Histogram

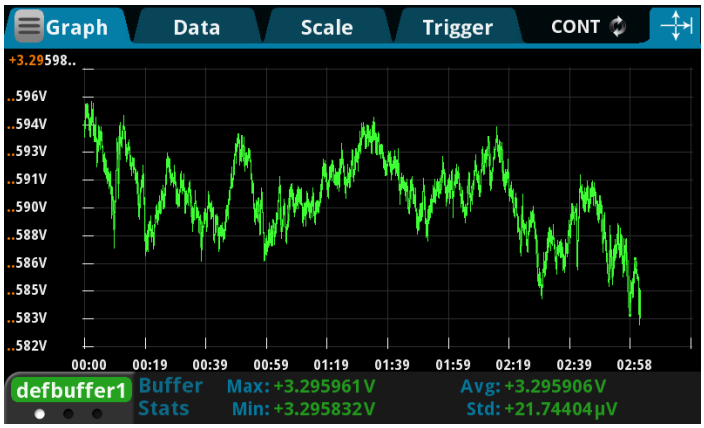


(b) Time signal

Figure 4.1: Measurements for the 5V supply

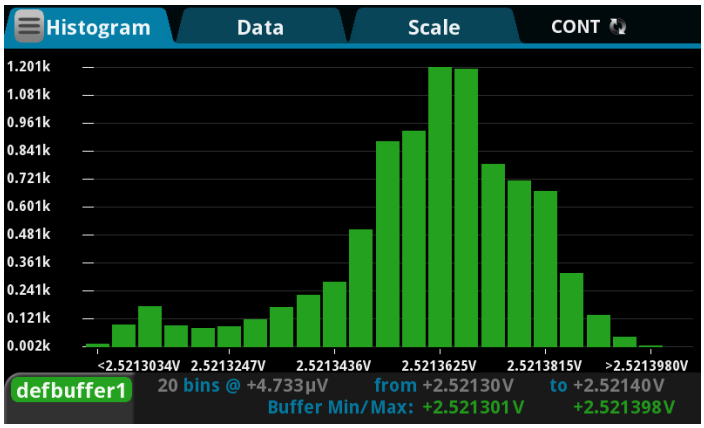


(a) Histogram

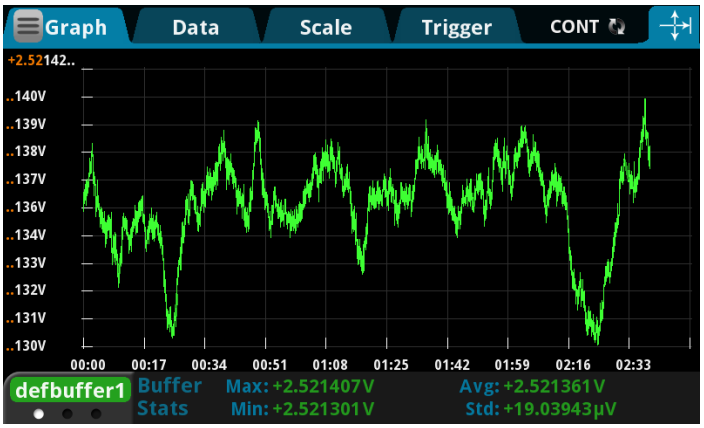


(b) Time signal

Figure 4.2: Measurements for the 3.3V supply

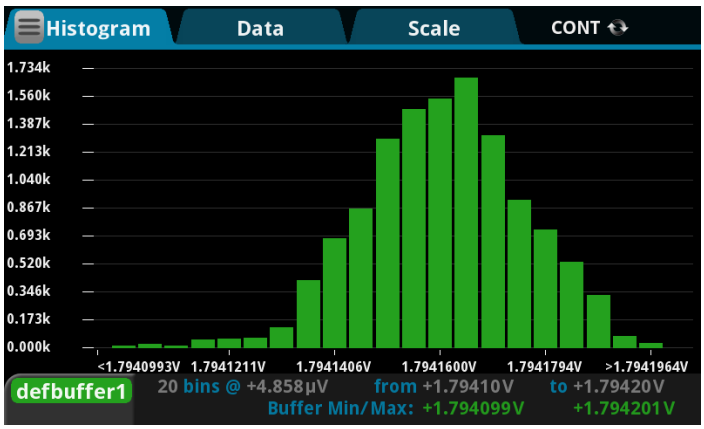


(a) Histogram



(b) Time signal

Figure 4.3: Measurements for the 2.5V supply



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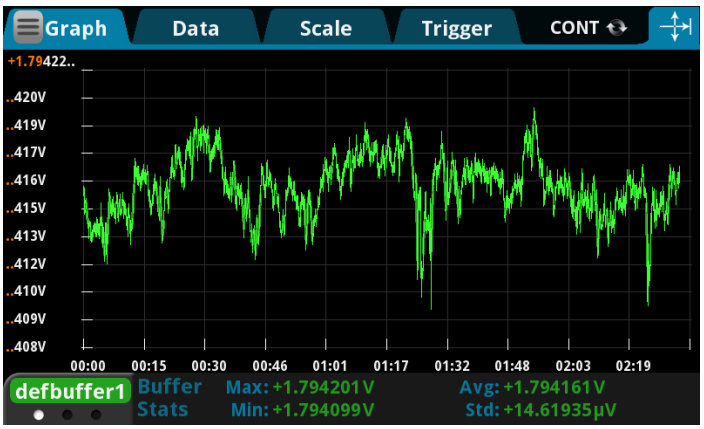
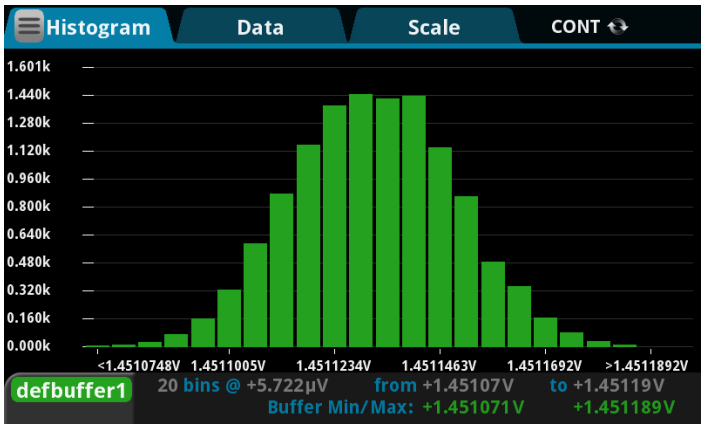
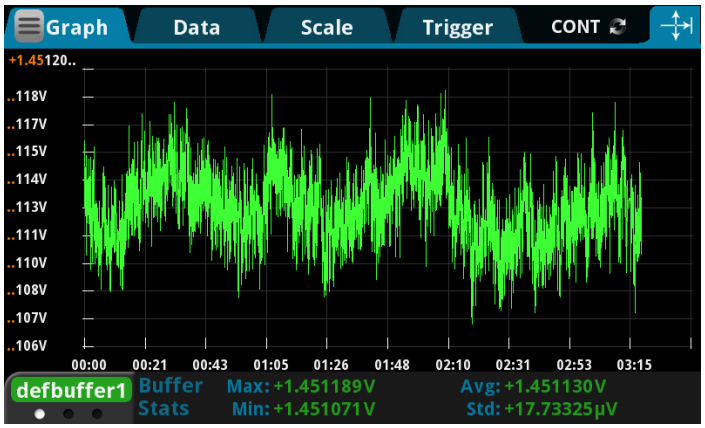


(b) Time signal

Figure 4.4: Measurements for the 1.8V supply

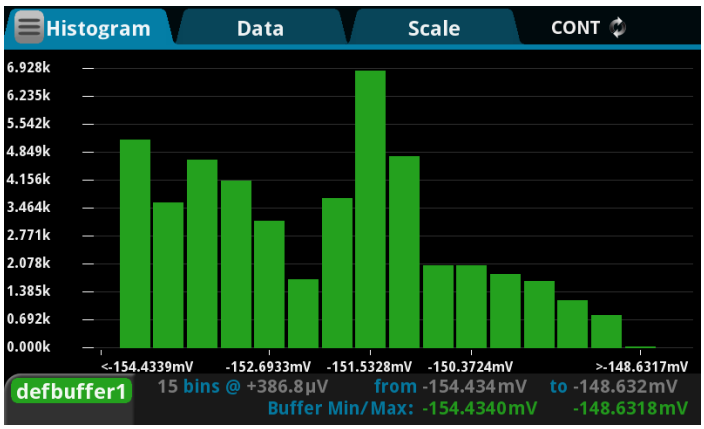


(a) Histogram

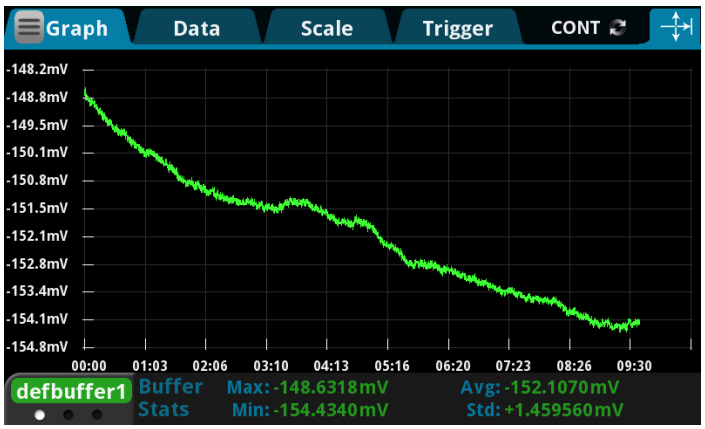


(b) Time signal

Figure 4.5: Measurements for the 1.5V supply

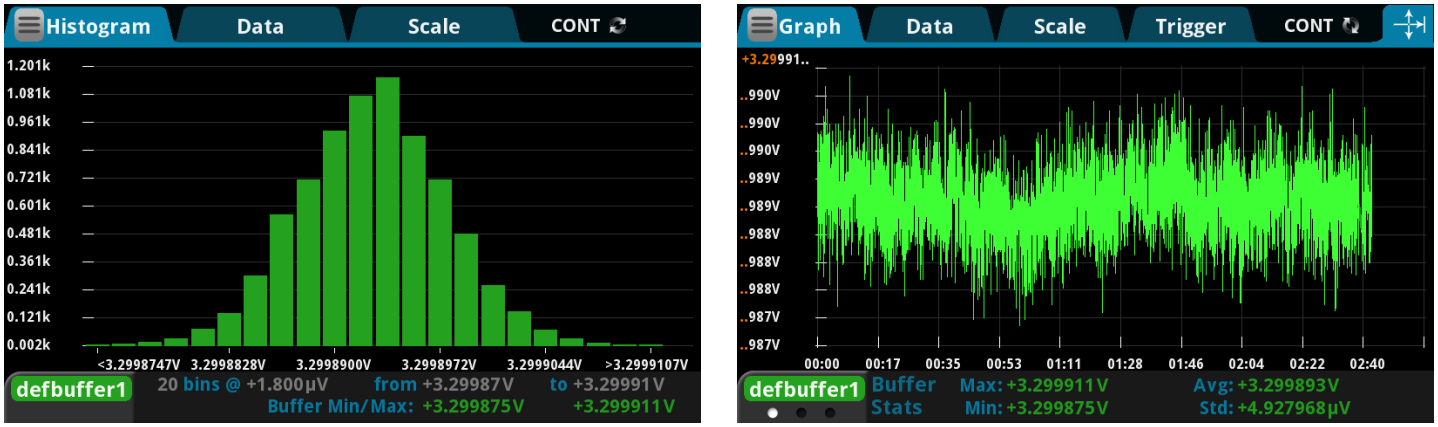


(a) Histogram



(b) Time signal

Figure 4.6: Measurements for the -0.23V supply



(a) Histogram

(b) Time signal

Figure 4.7: Measurements for the 3.3V reference voltage.

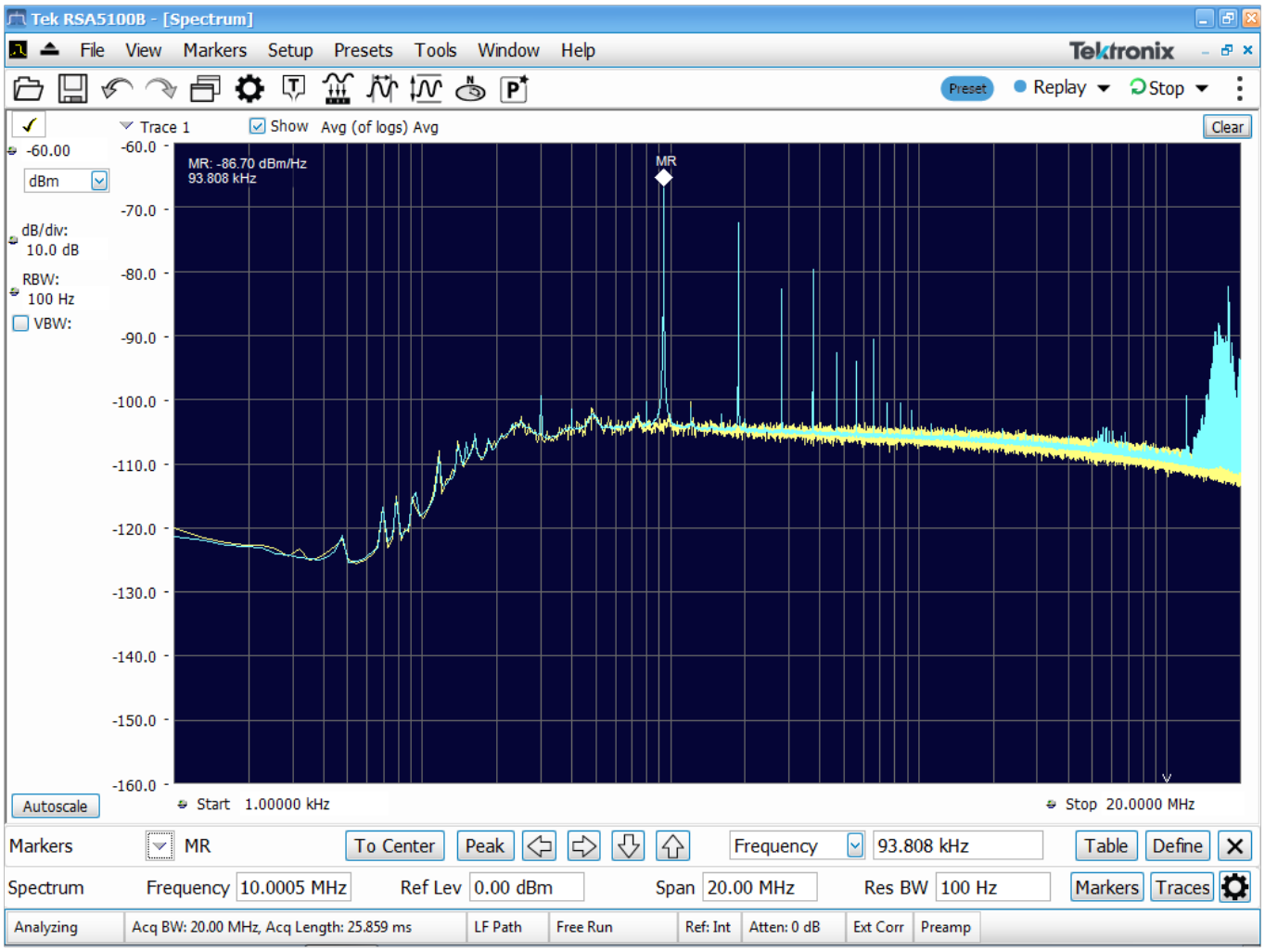


Figure 4.8: Spectrum 3.6V Supply - *The yellow curve derives from measuring the probe only while the blue line is the measurement resulting from the PCB. This is a screenshot of the frequency analyzer.*