Scale4Edge

Scalable Infrastructure for Edge Computing

Scaling RISC-V for Edge Applications

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The Scale4Edge ecosystem covers highly scalable components and extends them for edge applications on three levels

(1) CPU instruction level defined by the RISC-V Instruction Set Architecture (ISA) and Instruction Set Architecture Extensions (ISAX)
(2) software level defined by the C11 standard with compilers and libraries open to complementary standards like MISRA-C
(3) operating system and firmware level through system services, configuration interfaces, and drivers

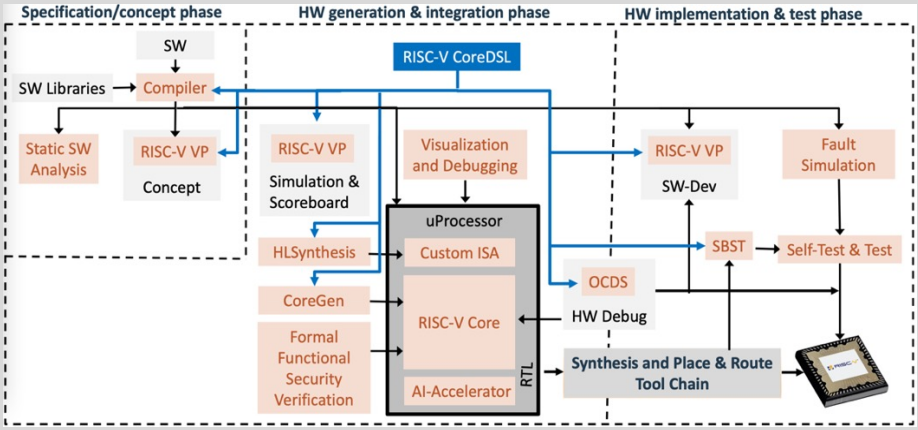
Scale4Edge tools customize, design, verify, and produce application-specific RISC-V based microprocessors

CoreDSL is a domain-specific language for the definition of base ISAs and ISA extensions (ISAX), usable for verification and HLS.

simple.core_desc

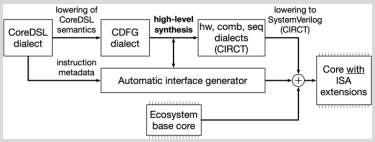
```
1  Core Simple {
2   architectural_state {
3    register unsigned short R[16];
4    extern unsigned char mem[1<<16];
5   }
6   instructions {
7    MOV{
8        encoding: 0b00 :: src[3:0] :: tgt[3:0] :: 0b110011;
9        behavior: {
10           R[tgt] = R[src];
11       }
12   }
13  }
14 }
```

TGC from MINRES is a highly flexible, scalable and extendable RISC-V processor for IoT applications, developed according to the safety standard ISO 26262



"Longnail": High-Level Synthesis for ISA Extensions

The custom HLS flow is based on LLVM, using the CIRCT framework for generating hardware for the ISAX.



Software Analysis & Synthesis

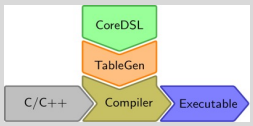
Static Software Analysis

AbsInt provides 3 static analysis tools

- *Astrée* analyzes C source code for runtime errors
- *StackAnalyzer* analyzes binary executables for worst-case stack usage
- *aiT* analyzes binary executables for WCET

Software Synthesis

Compiler generation for ISAX based on CoreDSL, gcc, and Clang/LLVM



Verification and Simulation, and Debugging

Virtual Prototype Based Simulation

DBT-RISE: environment to implement ISS interpreted/compiled execution, instruction accurate VP-VIBES: Ecosystem VP repo with peripherals und ISS models

ETISS: JiT based VP with varied ISA support customizable by plug-ins for different architectures and applications

Software based Self-Test (SBST)

- BMC-based ATPG (FreiTest) using Validity Checker Module (VCM)
- Stuck-at and cell-aware fault models

Fault Coverage and Fault Simulation

FEAR-V: QEMU based framework for RISC-V register fault injection and coverage analysis with fault tracing

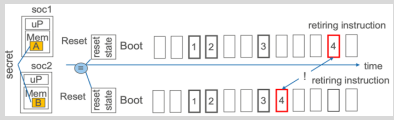
Visualisation and Debugging

- StarVisionPro visualizes test data, propagation of faults effects, and test coverage
- Lauterbach w/ RISC-V debug & trace solutions

Formal Verification for Functional Correctness and Security

Siemens EDA provides formal verification of processor cores for trojan & backdoor verification

- GapFree guarantees relevant processor behaviors for a given ISA
- Unique Program Execution Checking (UPEC) compares two program executions to detect side channels

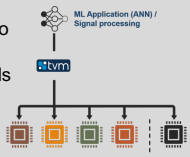


AI Edge Processing Demonstrators

TinyML

Complete end-to-end flow transforms ML model into deployable machine code including a kernel library for RISC-V MCUs (muRISCV-NN) uses and extends two frameworks:

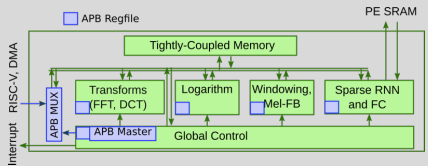
- Tensor Flow Lite for Microcontrollers (TFLM)
- Apache TVM



SpiNNedge

ML accelerator for signal processing and RNNs, applies delta encoding and sparsity exploitation

- windowing, filtering, frequency transformations
- different RNNs (GRU, LSTM, LMU)
- demonstrator chip in GF 22FDX technology

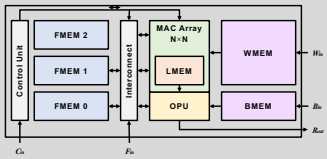


Applications

UltraTrail

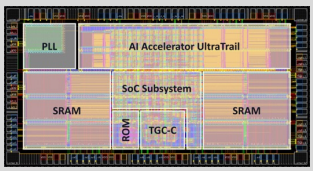
Ultralow-power AI accelerator for edge devices

- Real-time inference of temporal convolutional networks (TCNs)
- Total power consumption in the low microwatt range



Demonstrator Chip

- Neural-network based audio event detection model
- PULPissimo-based SoC platform using IP components and software of the Scale4Edge ecosystem
- GF 22FDX technology

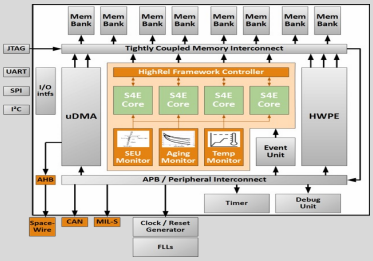


High Reliable Applications (HiRel)

for space, high altitude avionics, nuclear app.

TETRISC architecture with 4 CPU cores

- different modes: high performance, distress & fault tolerant modes
- monitors for SEU, aging, temperature
- Rad-tolerant memory protected with ECC
- based on PULPissimo plattform
- demonstrator chips in IHP130 technology



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