Deutsches Zentrum für Luft- und Raumfahrt

Scale4Edge

Timing instructions for RISC-V based hard real time edge devices

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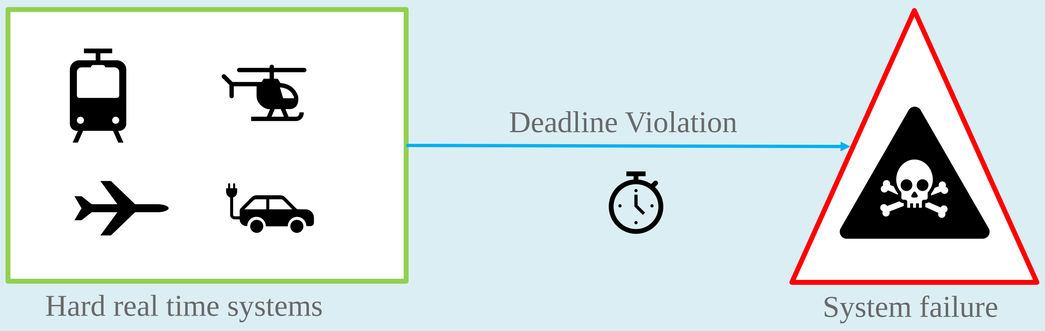
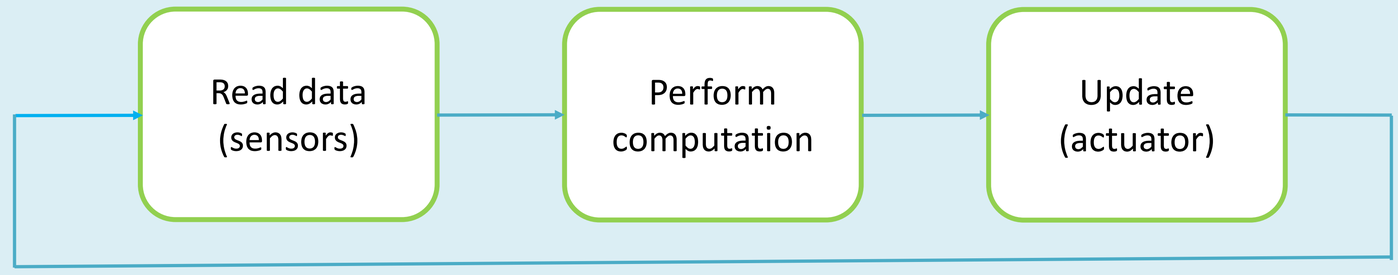
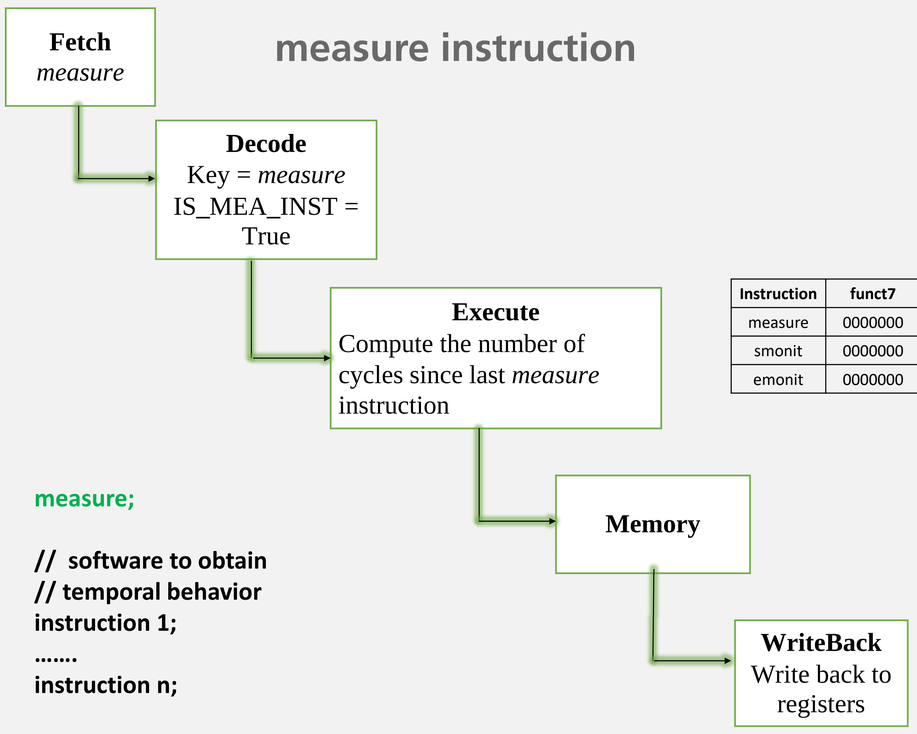
Introduction & Motivation



- Hard-real time systems demand precise timing
- Typical edge devices perform cyclic execution with defined period for each module
- Software solutions rely on timers/interrupts- adds additional overhead
- RISC-V ISAX to achieve low overhead -Three new instructions- **measure, smonit and emonit** are added to RISC-V ISA

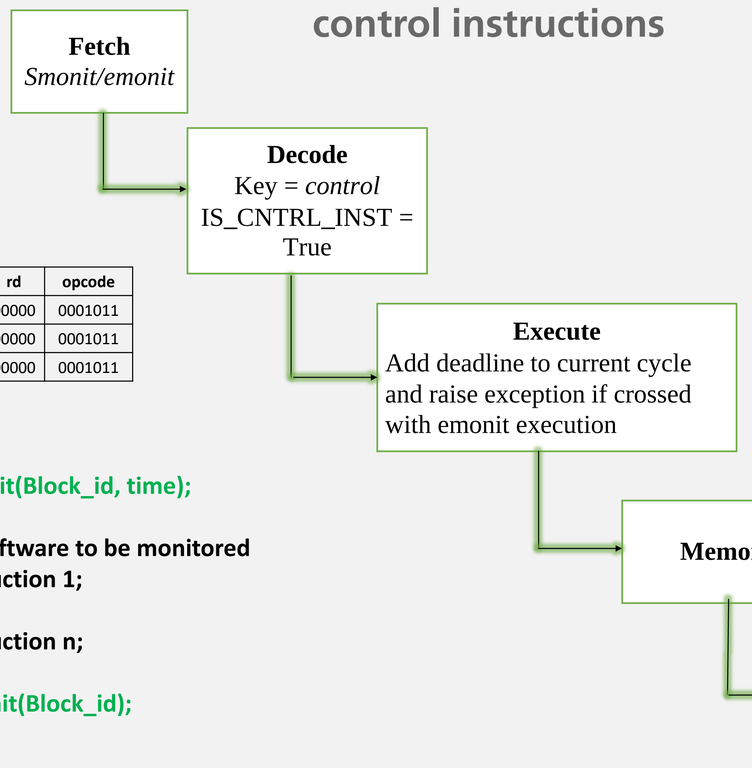


measure instruction



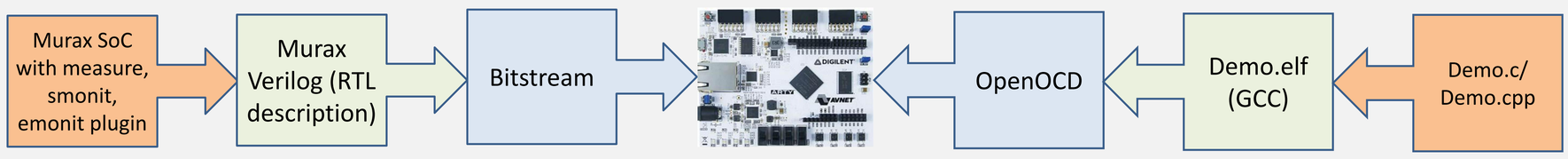

```
measure;

// software to obtain
// temporal behavior
instruction 1;
.......
instruction n;

measure;
```

control instructions



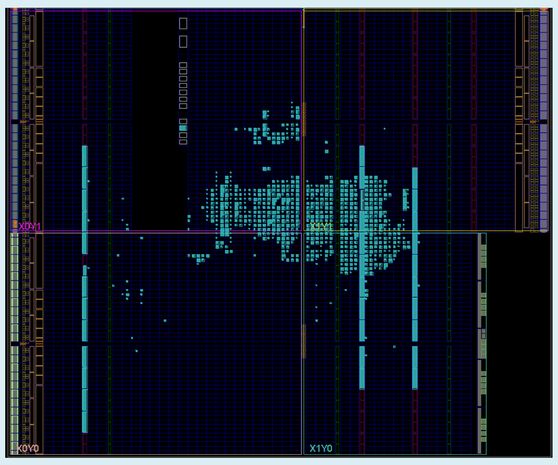
Instruction	funct7	rs2	rs1	funct3	rd	opcode
measure	0000000	00000	00000	000	00000	0001011
smonit	0000000	00000	00001	010	00000	0001011
emonit	0000000	00011	00001	011	00000	0001011

```
smonit(Block_id, time);

// software to be monitored
instruction 1;
.......
instruction n;

emonit(Block_id);
```



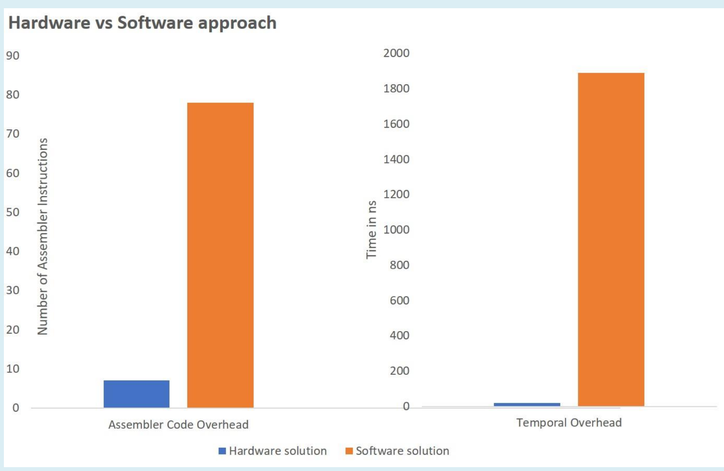
Results

Murax implementation layout



Hardware vs software solution

Measurement block	Assembler code overhead	Temporal overhead
Hardware solution	7	20 ns
Software solution	78	1.89 µs



Hardware (ISAX) vs Libbla solution

Measurement block	Assembler code overhead	Temporal overhead
Hardware solution	7 (0.5%)	20 ns
Libbla solution	1169 (101.5%)	3.002 ms

Hardware utilization

	LUTs	Registers
Measure	189 (11.5%)	200 (11.97%)
Control	276 (17.18%)	225 (13.47%)

Federal Ministry of Education and Research

This work has been developed in the ZuSE project Scale4Edge. Scale4Edge is funded by the German ministry of education and research (BMBF) (reference numbers: 16ME0122K-16ME0140). The authors are responsible for the content of this publication.

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