Intercalation of Thin Film Gd-doped Ceria Barrier Layers in Electrolyte Supported Solid Oxide Cells: Physico-chemical Aspects

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ABSTRACT

To minimize alteration of the $La_{0.6}Sr_{0.4}Co_{0.2}Fe_{0.8}O_{3-\delta}$ (LSCF)/$Gd_{0.2}Ce_{0.8}O_{2-\delta}$(CGO20)/$Y_{0.06}Zr_{0.94}O_{2-\delta}$(3YSZ) interface via strontium zirconate formation in solid oxide cells, electron beam physical vapor deposition (EB-PVD) was employed to manufacture dense, thin CGO interlayers. CGO layers with thicknesses of 0.15, 0.3 and 0.5 µm were integrated in state-of-the-art 5x5 cm^2 large electrolyte-supported cells (ESC) and their performance characteristics and degradation behavior were investigated. Electrochemical impedance spectroscopy measurements are correlated with a post-mortem SEM/energy dispersive X-ray spectroscopy (EDX) analysis to show that 0.15 µm thick layers lead to the formation of a continuous Sr-containing secondary phase at the CGO/YSZ interface, likely related to the formation of a $SrO\text{-}ZrO_2$ phase. Major performance losses were confirmed by an increase in both ohmic and polarization resistance with an increase in the frequency region ~10^3 Hz. Cells with 0.3 µm and 0.5 µm thick CGO layers showed similar high performance and low degradation rates over a testing period ~800 h. The YSZ/CGO interface of the cells with 0.3 µm thick CGO layer showed the formation of a discontinuous Sr-containing secondary phase, however, performance losses were still successfully prevented. Furthermore, it is observed that 0.5 µm thick CGO layers were sufficient to suppress the formation of the Sr-containing secondary phase.

1. Introduction

Solid oxide cells (SOC) are electrochemical energy conversion devices operating at high temperatures, typically around 800 °C. This enables high efficiencies in either operating mode, that is, in fuel cell mode in which a fuel is oxidized to produce electricity and heat, and in electrolysis mode in which steam or CO_2 are reduced into hydrogen or carbon monoxide, respectively. Besides hydrogen, solid oxide fuel cells (SOFC) can use a variety of other fuels such as hydrocarbons and ammonia. Solid oxide electrolysis cells (SOEC) are able to produce tailor-made syngas, which can be converted into synthetic fuels downstream. This unique versatility makes SOC an attractive technology to promote the decarbonization of the energy, transport and industry sectors via sector coupling.[1-2]

Conventional SOC mainly consist of ceramic components, which are brittle and susceptible towards mechanical failure during fabrication, stacking and operation. Thus, high mechanical strength of single cells is a key factor in the development of large-scale, mature SOC technology. However, since all functional cell layers also have to provide sufficient electrical conductivity (either electronic or ionic, or both), thick supporting substrates that could enhance the mechanical strength are usually associated with increased cell resistances and thus, often go at the expense of cell performance.

Two commonly used cell architectures are electrolyte-supported cells (ESC) and anode-supported cells (ASC). In ESC, a thick zirconia-based electrolyte (typically 65–200 µm) provides the mechanical strength to the cell. ESC is operated at high temperature (typically above 800°C) to reach sufficiently high ionic conductivity and to reduce the ohmic losses related to the thick electrolyte. In the ASC design, a thin zirconia-based electrolyte (5–15 µm) is supported by a porous nickel/yttria-stabilized-zirconia (Ni/YSZ) cermet substrate (300–500 µm). Due to the thin electrolyte, ohmic losses are significantly reduced which allows operation at lower operating temperatures (700–800 °C).

Rational material selection of the different functional cell components is a key aspect to achieve high SOC performance and durability. In this regard, the optimum material choices can vary due to the broad range of operating boundary conditions (operating temperature and pressure, inlet gas, SOEC or SOFC operation, etc.). In the past decades, extensive research and development efforts have been devoted to the improvement of the oxygen electrode since the historically used $La_{1-x}Sr_xMnO_{3-\delta}$ (LSM)/YSZ composite electrode shows only limited electro-catalytic activity. Presently, the state-of-the-art perovskite oxygen electrode is $La_{1-x}Sr_xCo_yFe_{1-y}O_{3-\delta}$ (LSCF), well-known as a mixed ionic and electronic conductor (MIEC) with high ionic and electronic conductivity and fast reaction kinetics. However, its significant reactivity with YSZ at high temperature leads to the formation of secondary $SrO\text{-}ZrO_2$ phases (mainly $SrZrO_3$) that show significantly reduced ionic conductivity and, thus, decrease the cell performance.[3] To prevent $SrO\text{-}ZrO_2$ formation at high processing temperatures (e.g. during LSCF processing at ~1040 °C) and operation temperatures, a diffusion barrier layers between LSCF oxygen electrode and YSZ electrolyte is necessary. This barrier layer should i) show high ionic conductance, ii) spatially separate YSZ and LSCF, and iii) mitigate cation interdiffusion across the layer via gas phase or bulk diffusion. Most commonly, 5-7 µm thick gadolinium-doped ceria (CGO) layers are cost-efficiently manufactured by means of screen-printing and a thermal treatment. However, starting at a temperature of 1200 °C a solid solution is formed at the CGO /YSZ interface that reduces ionic conductivity (which is still higher than the one of $SrZrO_3$).[4-5] The exact composition of this solid solution can vary on the material selection and the processing parameters. For example, $Gd_2(Zr_{1-x}Ce_x)_2O_7$ pyrochlore phase and $[(ZrO_2)_{1-x}(CeO_2)_x]_{0.92}(Y_2O_3)_{0.08}$ were reported.[6] To mitigate this effect, the CGO layer is often fired between 1200-1300 °C without full densification. Thus, the CGO layer still remains porous and permeable for volatile Sr-containing species evaporated from the LSCF electrode, such as $Sr(OH)_2$, which can diffuse to the electrolyte interface in the gas phase and react with YSZ.[7-8]

Furthermore, it is technically difficult to further minimize the layer thickness via screen-printing.

As alternatives to the conventional sintering method, different physical vapor deposition (PVD) techniques such as magnetron sputtering,[9] electron beam physical vapor deposition (EB-PVD),[10-11] and pulsed laser deposition (PLD)[12] have been investigated to produce dense and thin CGO diffusion barrier layers at lower temperatures (400-800°C). These approaches can ideally prevent both SrO-ZrO_2 and solid solution formation.

So far, thin film CGO layers have been mainly investigated in the ASC design in the intermediate operating temperature range 600-800 °C with the aim to reduce ohmic losses. [11, 13-16] Although dense PVD-coated diffusion barrier layers diminished or prevented gas diffusion, Sr diffusion along grain boundaries can still occur, leading to the formation of the SrO-ZrO_2 phase if their thickness is insufficient.[17] Therefore, most of these studies employed thin film CGO barrier layers with thicknesses of ~0.5 µm. When SrO-ZrO_2 phase formation was observed, it was reported to mainly occur during LSCF sintering and did not seem to proceed during operation in ASC at temperatures below 800 °C.[9, 18-19]

In contrast to ASC, there are few reports on the integration of PVD-coated CGO interlayers into ESC with significantly harsher boundary conditions due to higher operating temperatures over 800 °C and accelerated diffusion processes. For example, SrO-ZrO_2 phase formation has been observed during operation at 1000 °C in ESC with a screen-printed CGO interlayer.[20] Therefore, it is meaningful to study the functionality and properties of thin film CGO interlayers in ESC.

To identify the minimum CGO barrier layer thickness necessary to prevent performance losses in ESC operated at 860 °C, this study presents a systematic investigation of EB-PVD coated CGO interlayers with different thicknesses and their effect on CGO/YSZ interface degradation during processing and electrochemical durability testing.

2. Experimental Methodology

2.1 Thin film deposition

Commercially available 90 µm thick 3YSZ electrolytes (Kerafol, Eschenbach in der Oberpfalz, Germany) were used as substrates for thin film deposition and its further characterization. Before CGO layer deposition, the surface of the 3YSZ substrates was cleaned with acetone and fiber-free clean-room tissue in a laminar flow-box with low dust environment. The deposition of the thin film CGO barrier layers was performed by electron beam physical vapor deposition (EB-PVD) with a special technology that was developed for the growth of multi-component coatings on large area.[21] In each coating batch, up to 6 substrates of 5 cm x 5 cm^2 were placed on a rotating substrate holder of 23 cm in diameter. The substrates were heated to 600 °C and rotated with 5 Hz during deposition. The distance between target and substrate was 20 cm. The rotation in combination with the proper distance between evaporation zone and substrate leads to very homogeneous coatings with thickness variation of less than +-5% over the full deposition area. CGO20 target material in form of sub-mm grains is extracted from a funnel by a rotating, water-cooled copper plate and fed into the electron beam. As the material is continuously transported and completely evaporated in the hot zone, no composition gradient occurs in the films. The growth rate can be adjusted by the rotation speed of the copper plate and is controlled by a quartz crystal monitor. Deposition of the CGO layers was done with an effective growth rate of 20 nm/min. The coating chamber features an oxidation zone, where an oxygen pressure of $5x10^{-3}$ mbar can be reached, enough to fully oxidize the coating into CGO. After deposition, the films are cooled down in pure oxygen atmosphere.

To assess the thermo-mechanical compatibility of the thin layers and the substrates, as well as potential effects of grain growth at higher temperatures, thermal treatments of the bi-layer structure were carried out at 950°C and at 1040 °C to simulate typical LSCF air electrode processing.

2.2 Solid oxide cell manufacturing

Commercially used half cells (Sunfire, Dresden, Germany) consisting of a 90 µm thick 3YSZ electrolyte (5 x 5 cm^2), a screen-printed ~5 µm thick CGO interlayer on the fuel electrode side and a Ni/CGO fuel electrode (4 x 4 cm^2) including a functional layer and a more porous current collector layer with increased Ni content were used as substrates. On the oxygen electrode side, a thin film $Ce_{0.8}Gd_{0.2}O_{2-\delta}$ (CGO20) barrier layer was deposited as described above via EB-PVD. Different thicknesses of 0.15, 0.3 and 0.5 µm were employed. One cell with 0.5 µm thick EB-PVD CGO diffusion barrier layer was pre-calcined at 1040 °C for 1 h (see Table I) before the oxygen electrode deposition.

Two different batches of LSCF powders were separately mixed with α-terpineol containing 6 wt% of ethyl cellulose as binder, forming two homogenous inks, respectively. LSCF electrodes (4 x 4 cm^2) with a thickness of approximately 20 µm (thickness after sintering) were screen-printed onto the EB-PVD-coated half-cell substrates, dried at 75 °C in air, and subsequently calcined at 1040 °C for 1 h. The heating rate was 3 K/min and the cooling rate was 5 K/min. The same LSCF paste was used for all cells in each long-term test. However, between the two tests different pastes were applied. Thus, electrochemical performance characteristics of the two batches of cells cannot directly be compared.

2.3 Electrochemical characterization

The setup for cell testing enables the characterization of up to four cells simultaneously under variation of current density and has been illustrated and described in detail elsewhere.[22-23] The high reproducibility of measurements between the different positions has been demonstrated in previous studies.[24-25]

Two long-term experiments were performed with different cells for 640 h and 815 h. All tested cells are listed in Table I. All cells were operated at 860 °C with 97 % H_2 and 3 % H_2O at a constant total fuel flow rate of 1 L•min^{-1} and air supply at a constant flow rate of 1 L•min^{-1}.

The cells were heated (3 K/min) to 900 °C for sealing and NiO reduction. Proper sealing of all cells was confirmed by the open circuit voltage (OCV) to be higher than 1.2 V in supply of dry hydrogen. After initial characterization by means of electrochemical impedance spectra, fuel mixtures and current density were adjusted to the desired operating conditions and the long-term tests were started. In order to monitor the degradation process, regular impedance measurements were carried out at open circuit voltage (OCV).

Electrochemical impedance spectroscopy was performed with an electrochemical workstation (Zahner® PP-240 with Thales software) in a frequency range from 20 mHz to 100 kHz with 10 points per decade. The amplitude of the current stimulus was chosen to be 500 mA and did not trigger a voltage response of higher than 15 mV. SEM images were acquired using a Zeiss Ultra Plus SEM. The distribution of relaxation times (DRT) was calculated with the toolbox DRTools.[26] Equivalent circuit modeling was performed by using a complex non-linear square (CNLS) fit in the Zahner Analysis software.

Table I. Overview of test specifications.

	CGO diffusion barrier layer air side	Voltage degradation [mV]	Current density [A•cm^{-2}]
640 h test	0.15 µm	46	0.6
	0.3 µm	20	0.6
	0.5 µm	20	0.6
815 h test	0.15 µm	11	0.5
	0.3 µm	9	0.5
	0.5 µm, pre-calcined at 1040 °C (1h)	10	0.5

2.4 Characterization of thin films and cell assemblies

Thin film specimen was characterized by X–ray diffraction (XRD) with a D8 Discover GADDS equipped with a VÅNTEC-2000 area detector (Bruker AXS, Germany). The diffraction pattern was recorded in the Bragg-Brentano geometry with a tuned monochromatic and collimated Cu Kα radiation source. Crystalline phases were identified with the ICDD data base. The operated cells were prepared for analysis by removing the LSCF air electrodes with a HNO_3 solution. Morphology and microstructure were investigated with a Zeiss ULTRA PLUS scanning electron microscope (SEM) (Carl Zeiss AG, Germany) in combination with a Bruker XFlash 5010 energy-dispersive X-ray spectroscopy (EDX) detector for elemental analysis. Sample surface were investigated with a secondary electron (SE) detector for morphology investigation and an energy selective backscattered (EsB) detector for crack analysis. Fracture surface images were recorded with an EsB detector, and polished cross-sections were examined with an angle selective backscatter (ASB) detector for high phase contrast at the interfaces and phase analysis (coupled with EDX).

3. Results

As the first step, the surface morphology and microstructure of EB-PVD CGO layers were investigated to determine the optimum thickness. Subsequently, CGO barrier layers with varied thicknesses were integrated into full cells to identify the most promising cell configuration.

3.1 Characterization of EB-PVD CGO barrier layers

0.5 µm and 2 µm thick CGO films deposited on the 3YSZ substrates via EB-PVD at 600 °C were subsequently fired at 1040 °C (heating rate 3 K/min) for 1 h to simulate the thermal treatment of the LSCF oxygen electrode. The corresponding top view SEM images of as-coated and fired samples are presented in Figure 1(a-d). All samples showed a dense surface with no visible porosity.

Furthermore, differences in surface morphology and grain size are apparent between the 0.5 and the 2 µm thick layers in both the as-coated and fired samples. In case of the 0.5 µm thick layer, layered structures of the same crystallographic orientation were stacked on each YSZ grain, reflecting the underlying substrate surface structure (Fig.1a). After annealing, the crystallites merged into round-shaped single grains with the size of several hundred nanometers (Fig.1b). The morphology of the YSZ surface is not visible anymore in the top view image of the 2 µm thick CGO coating (Fig.1c+d), which is smoother and less dependent on the YSZ substrates. Columnar crystallite growth is shown in the fracture SEM image (Fig. 2a) which is consistent with previous reports.[10, 27] The columnar grain boundaries were reported to act as pathways for elemental diffusion.[12-13] However, the calcination at 1040 °C for 1 h led to the CGO grain growth in the submicronic range with a smooth surface (Fig. 1b+d) and the formation of a more homogeneous polycrystalline microstructure (Fig. 2b). Grain boundary areal density was significantly reduced due to grain growth. Although a few isolated pores with diameters of up to 150 nm can still be observed along the grain boundaries in the layer, continuous vertical grain boundaries as diffusion pathways are no longer visible. The formation of the isolated voids, or closed pores, is consistent with previous work and probably related to the columnar CGO growth.[28]

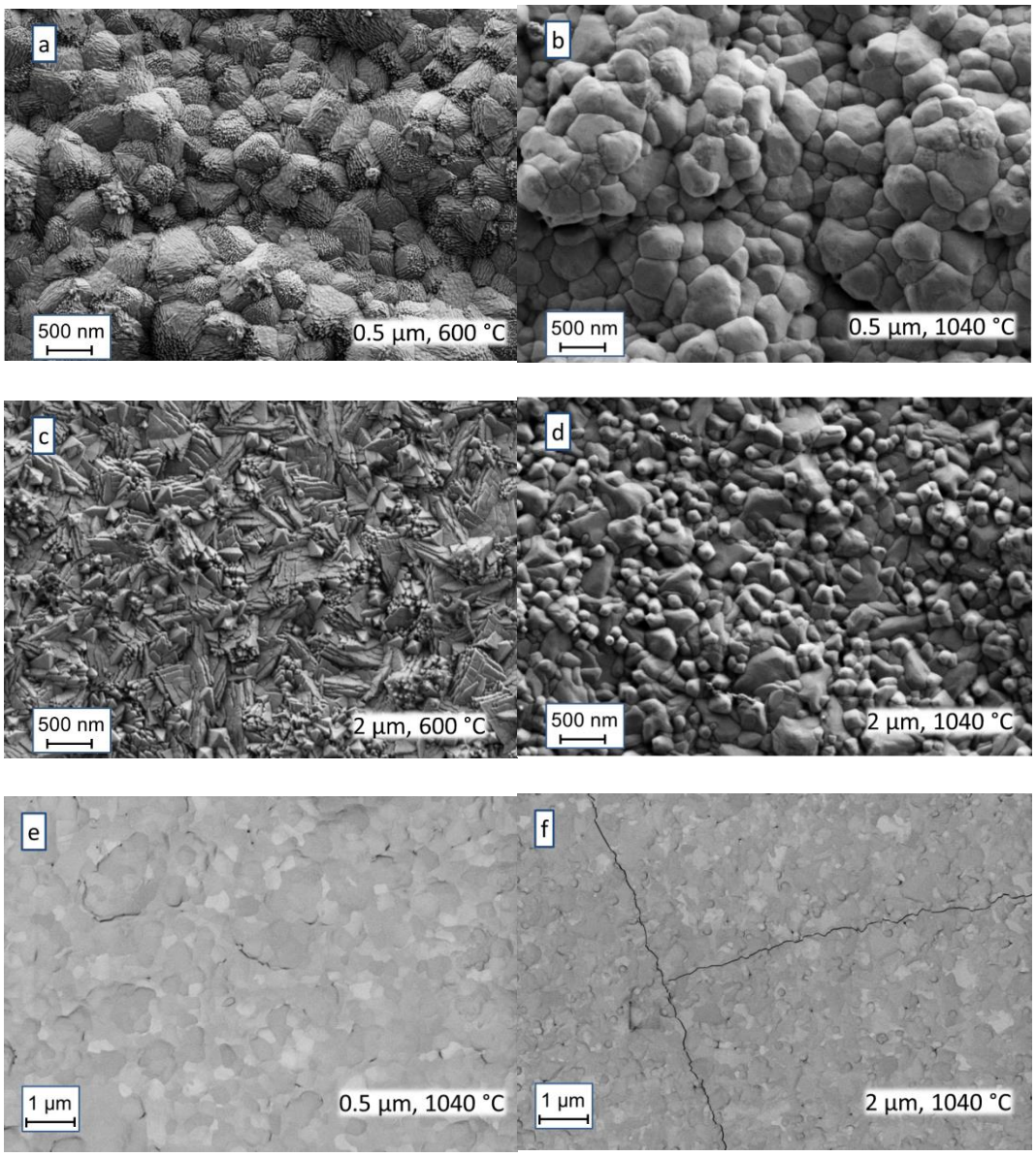

Fig. 1: Top view of a CGO interlayer with 0.5 µm thickness (a) as-coated at 600 °C and (b) fired at 1040 °C. Top view of a CGO interlayer with 2 µm thickness (c) as-coated at 600 °C and (d) fired at 1040 °C. Top view EsB electron detector SEM image of a 0.5 µm thick (Fig. 1e) and 2 µm thick CGO barrier layer (Fig. 1f) fired at 1040 °C.

It was observed that the 0.5 µm thick CGO film was crack-free (Fig. 1e) with clearly visible grain boundaries in the SEM image. However, channel cracks were found in the SEM image of the 2 µm thick CGO layer (Figure 1f). Cracking of thin layers due to high residual thermal stress is a common mode of failure. In a solid oxide cell configuration, the residual stress may

also increase the probability of potential crack penetration into the substrate. Elemental interdiffusion between oxygen electrode and electrolyte may occur along the cracks in the CGO layer.[29-30]

Cracking can occur when the steady-state energy release rate of the channel crack, ζ_{ch}, exceeds the critical energy release rate (the fracture energy) of the coating. ζ_{ch} can be calculated according to

$$\zeta_{ch} = \mathbf{\Omega} \frac{\sigma^2 h}{E_c}, \quad (1)$$

where σ is the residual stress, h the coating thickness and E_c the Young's modulus. $\mathbf{\Omega}$ is a non-dimensional function of the elastic properties of coating and substrate.[29, 31] Thus, cracking is more likely to happen with increasing residual stress in the coating and increasing layer thickness. Therefore, the risk of crack formation becomes higher with the increasing shrinking volume associated with CGO layer thickness. Thus, the ideal CGO layer should be as thin as possible to minimize residual stress, however, still thick enough to prevent undesired elemental interdiffusion.

At the CGO/YSZ interface considerable residual stress may arise due to the thermal expansion coefficients (CTE) mismatch between CGO ($\alpha_{CGO} = 12.5 \cdot 10^{-6}$ K^{-1}) and YSZ ($\alpha_{YSZ} = 10.8 \cdot 10^{-6}$ K^{-1}).[29, 32] The residual thermal stress in a coating at a temperature T, under the assumption of an infinite thick substrate, can be calculated according to

$$\sigma = (\alpha_{CGO} - \alpha_{YSZ})(T_p - T)\, E_c / (1-\upsilon_c) \quad (2)$$

with T_p being the thermal treatment temperature at which the multilayer is stress free, and ν_c the Poisson's ratio of the coating. As in the present case, $\alpha_{CGO} > \alpha_{YSZ}$ and $T_p > T$, the residual thermal stress in the CGO layer at room temperature is tensile. Since the CGO layer was initially deposited at 600°C, the bonding of the two layers was assumed to be stress-free at this temperature. During LSCF calcination at 1040°C, that is, the highest processing temperature in the present work, a compressive stress should evolve in the CGO layer upon heating. The stress

at the interface could be released at this temperature by grain boundary sliding during the grain growth in the layer. It is sometimes assumed that the highest processing temperature corresponds to the stress-free state in thin films, providing that the dwelling time was long enough to release the stress. Even though the stress conditions in the thin film CGO layer after calcination at 1040 °C could not be measured precisely, it is reasonable to expect very small or no residual stress at all. Since the CGO layers could not shrink freely during cool-down, a considerable residual thermal stress could be induced in the multilayer structure during cooling from 1040 °C to room temperature.

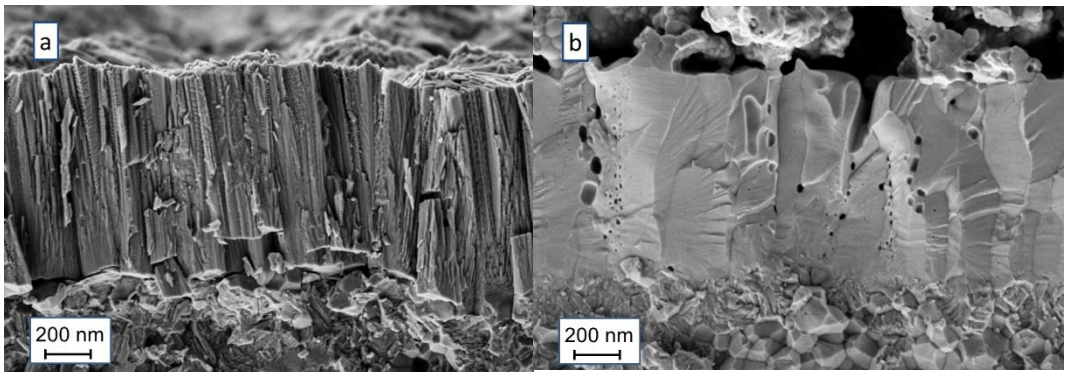

Fig. 2. Fracture cross section image of a CGO interlayer with 2 µm thickness (a) as-coated at 600 °C and (b) fired at 1040 °C.

To investigate the crystallographic characteristics of the CGO layer, XRD patterns of samples with 0.5 µm and 2 µm thick CGO coatings were analyzed. Observed peaks were identified as CGO and 3YSZ without any secondary or impurity phases in both as-coated samples. The XRD diffractograms of 0.5 µm thick CGO coatings on YSZ substrates are presented in Fig. 3a. The sharp diffraction peaks of the CGO layers indicate a high degree of crystallinity already after deposition. The CGO layer exhibited the powder diffraction patterns of the cubic fluorite phase. Thus, during the growth of the CGO film with EB-PVD no special crystallographic orientation was preferred.

The CGO diffraction angles of the samples annealed at high temperatures were apparently higher than those of the as-coated layers. Figure 3b shows the lattice parameters of the CGO layers determined by XRD analysis. It demonstrates the lattice parameter decrease with annealing temperature, which was more pronounced in thinner coatings. As discussed above, reduction of the out-of-plane lattice parameter should be more pronounced for thicker CGO layers when it originates mainly from residual stress. However, the lattice parameter change was larger in the 0.5 μm than in the 2 μm thick coating. Since the lattice parameters of the as-deposited coatings were close to the ones of CGO20, and those after the high temperature treatment were remarkably reduced and more significant in thin coatings and at higher temperatures, the lattice parameter reductions were most likely caused by compositional change. It is well-known that elemental interdiffusion between YSZ and CGO occurs at high temperatures.[33] Although such interdiffusion was mainly reported at temperatures >1200 °C, the SEM image in Fig. 2b also shows an interphase between the columnar structure of the CGO and the clearly defined 3YSZ grains after thermal annealing at 1040°C. Interdiffusion was shown to result in a mixture of various fluorite phases of different chemical compositions between CGO and YSZ.[6] In the diffractograms, the interdiffusion zone reflects as dissolution of Zr^{4+} into the fluorite CeO_2, and the resulting phase was identified as $(Ce, Gd)_{1-x}Zr_xO_{2-\delta}$. In this phase, x could be between a few and 10 mol% and the Ce-Gd ratio would be similar to CGO20. This hypothesis is also consistent with our recent work, where we observed an even more pronounced shift of the CGO peaks to higher angles after exposing the CGO/YSZ interface to temperatures ~1300 °C suggesting increased interdiffusion.[34]

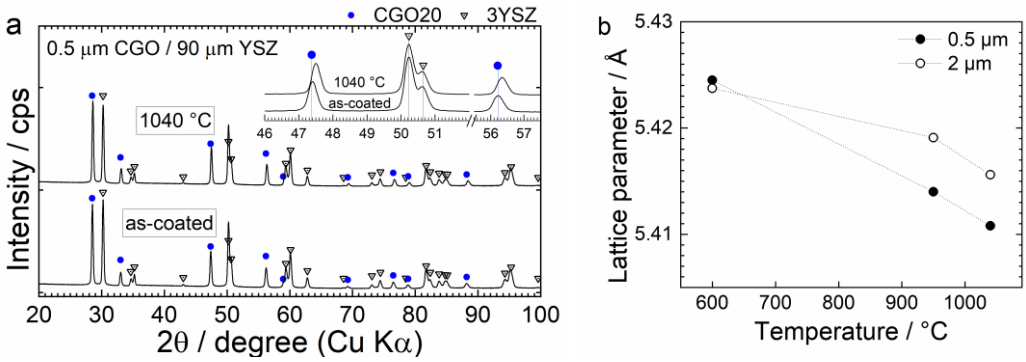

Fig. 3. (a) θ-2θ X-ray diffractograms of samples with 0.5 µm thick EB-PVD CGO layers on 3YSZ electrolytes that were as-coated and treated at 1040 °C for 1 h. Identified diffraction patterns are CGO20 and 3YSZ (CGO20: PDF#01-080-5535, 3YSZ: PDF#00-060-0503). (b) Lattice parameter comparison of the deposited CGO on 3YSZ substrates determined by the XRD analysis. As-coated and annealed samples are compared for 0.5 and 2 µm thick CGO. 950 °C and 1040 °C were the temperatures of annealing, while 600 °C was the substrate temperature during the EB-PVD process.

3.2 Electrochemical testing of electrolyte-supported cells

Since 0.5 µm thick CGO interlayers were shown to be sufficiently thin to avoid crack formation upon firing at 1040 °C, they were chosen as a starting point for further optimization and integrated into full cells. In addition to cells with 0.5 µm thick CGO layers, cells with even thinner EB-PVD interlayers of 0.15 µm and 0.3 µm thickness were investigated. Performance and long-term stability tests of the different cells were carried out in two batches and are described in the following subsections.

3.2.1 Initial characterization

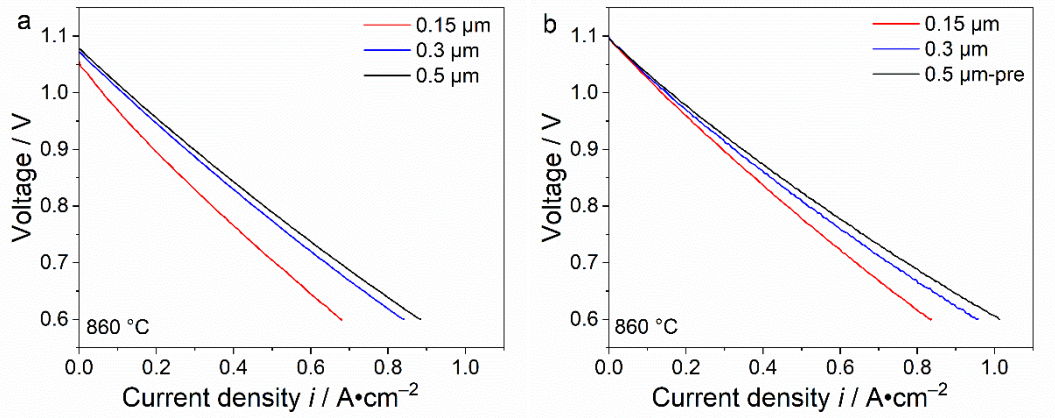

Fig. 4: Initial current-voltage curves of the cells in the (a) 640 h and (b) 815 h durability test.

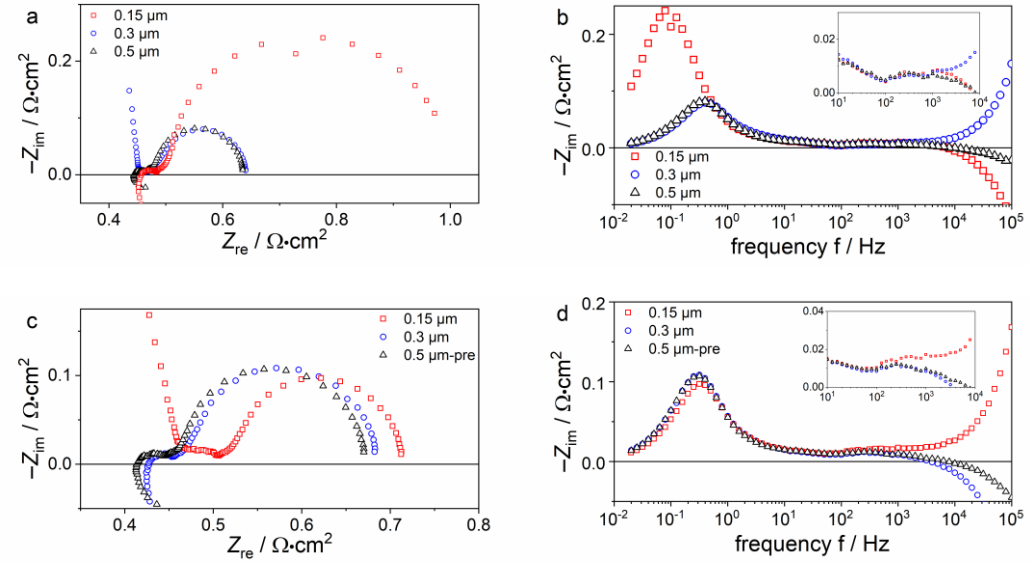

Fig. 5: Initial Nyquist and imaginary impedance plots of the cells in the (a+b) 640 h and (c+d) 815 h durability test.

First batch - The initial *i-V* curves of the cells with 0.3 and 0.5 µm thick interlayers in the first batch (Fig. 4a) showed a similar current density of 0.88 A•cm^{-2} and 0.84 A•cm^{-2} at 0.6 V. The cell with 0.15 µm CGO interlayer reached a significantly lower current density of 0.68 A•cm^{-2} at 0.6 V. In Fig. 5a+b, initial impedance spectra of all cells are depicted at OCV. All cells showed an ohmic resistance around 0.45 Ω•cm^2 confirming the high reproducibility of the test setup (the ohmic resistance of the 0.3 µm cell had to be estimated due to interference phenomena in the high-frequency region of the spectra). Moreover, all cells showed a nearly

identical first semicircle with a peak frequency of ~10^3 Hz, which was probably dominated by the LSCF electrode process.[35] The most striking difference between the cells was the increased low-frequency resistance of the cell with 0.15 µm thick CGO interlayer at 0.1-1 Hz. This was caused by a diminished fuel gas supply of the respective cell position in the test setup, which led to an increased gas conversion resistance.[36] The problem was fixed before the subsequent test.

Second batch - Another three cells with 0.15, 0.3 and 0.5 µm thick CGO interlayers were investigated. In contrast to the first batch, the cell with 0.5 µm thick CGO in this batch was pre-calcined at 1040 °C for 1 h before applying the LSCF electrode to assess if the pre-calcined CGO improves cell performance and diminishes Sr diffusion. Again, the same trend as in the first batch was observed with regards to performance of the three cells measured by current-voltage curves (Fig. 4b). The cell with 0.5 µm thick CGO layer showed the highest maximum performance (0.6 V/1.01 A•cm^{-2}), followed by the cell with 0.3 µm thick CGO layer that displayed a slightly lower maximum current density (0.96 A•cm^{-2} at 0.6 V), and the cell with 0.15 µm thick CGO layer that reached a significantly lower performance (0.84 A•cm^{-2} at 0.6 V).

The high frequency interference phenomena made it difficult to determine the exact resistance values from the impedance spectra (Fig. 5b). However, an increased resistance of the impedance of the cell with 0.15 µm thick CGO barrier layer at frequencies around 10^3 Hz and an increased ohmic resistance are clearly visible in Fig. 5c+d. Since the only difference between the three cells is the thickness of the CGO barrier layer, the increased resistance of this process was likely related to the degradation of the YSZ/CGO/LSCF interface. Interestingly, the increase of the impedance response at the frequency region of ~10^3 Hz was not observed for the nominally equal cell in batch 1.

3.2.2 Durability tests

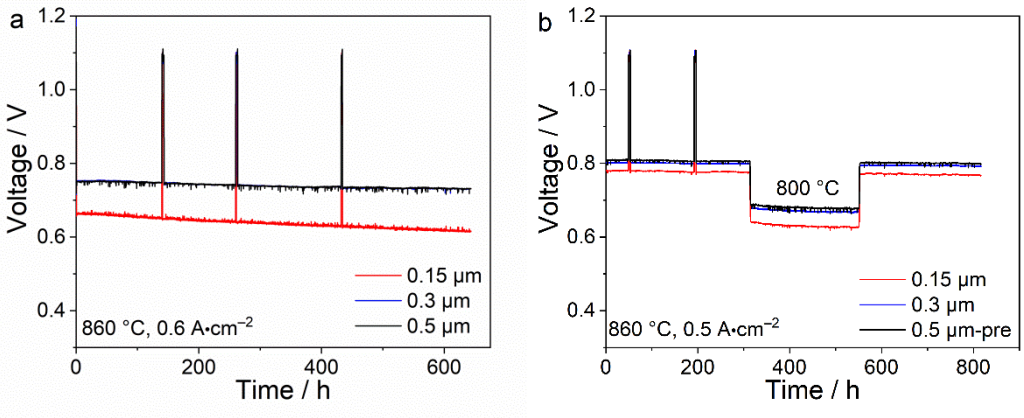

Fig. 6: Voltage-time plots of the (a) 640 h and (b) 815 h durability test.

First batch over 640 h - In the durability test, the three full cells were investigated at 0.6 A•cm^{-2} over 640 h (Fig. 6a). The cells with 0.3 and 0.5 µm thick CGO interlayers had an initial voltage of 0.751 V, while the 0.15 µm cell only showed 0.66 V and thus, a considerably lower performance. A significant higher voltage degradation of 46 mV (77 mV/kh) was observed for the cell with 0.15 µm thick CGO barrier layer. During the same period the cells with 0.3 and 0.5 µm thick barrier layers showed nearly exactly the same voltage evolution behavior with lower degradation of 20 mV (33 mV/kh).

To further analyze the different degradation behavior of cells with 0.15 and 0.5 µm thick CGO layers, the evolution of their impedance spectra at OCV is shown in Fig.7. In addition, the DRT of the spectra were calculated and depicted in Figure 7c+f.

Based on the DRT analysis of the cells, a minimum of four loss processes could be identified in the polarization resistance. In our previous work we have observed two main Ni/CGO fuel electrode processes at ~1 Hz and ~10^2 Hz.[37-38] They likely correspond to the low-frequency process $P_{A,LF}$ at 10 Hz and middle-frequency process $P_{A,MF}$ at 200 Hz and are associated with the anode charge transfer and a bulk or CGO/YSZ interface process, respectively. The gas

conversion process P_{GC} was identified at 0.1 Hz. [36] The additional process at ~10^3 Hz is then likely related to the LSCF electrode process P_C.[24, 35]

Based on this analysis, a simple equivalent circuit model consisting of an inductance, one resistor R_S and four resistor-constant phase elements (R-CPE) was applied to estimate the increased high frequency resistance values. R-CPE elements were shown to accurately reproduce the behavior of the two Ni/CGO anode processes and also the gas conversion process in the used test bench setup.[24, 37] A Gerischer element is often applied for the LSCF cathode process at 10^2-10^3 Hz.[39] However, due to a potential overlap of the cathode process with another process, a simplified R-CPE element was employed to reduce the number of fitting parameters. In this case, the derived values rather present a qualitative estimate than a fully physically meaningful model of the underlying processes. The obtained resistance, capacitance and exponent values of the different processes of cells with 0.15 µm and 0.5 µm CGO at 0 h, 140 h and 640 h are summarized in Table II.

In one case, the CPE describes a perfect capacitor when the exponent n of the capacitance equals 1. The value of Q_0 is the value of the capacitance C of the process and has the units of F•cm^{-2}. In another case, the CPE describes an imperfect capacitor when $0<n<1$. The Q_0 can be converted into the true capacitance of the R-CPE element as described in Ref.[40]. In the present study, P_C, $P_{A,MF}$ and P_{GC} could be described well with an ideal capacitance and thus, the values in the CNLS routine were set to 1. For $P_{A,MF}$, n = 0.85 was shown to consistently decrease the error of the fits. All n values were held constant in the respective fitting routines to decrease the number of fitting parameters. The obtained capacitance values $C_{A,MF}$ of 10-30 mF cm^{-2} and $C_{A,LF}$ of 0.1-1 F cm^{-2} are in the same order of magnitude as the values observed in our previous study of symmetrical Ni/CGO10 electrodes, thus, confirming our assignment of both processes to the anode.[37]

Between 0 and 140 h of the test there was a change in ambient temperature in the laboratory causing temperature changes in the water bubbler used for humidification. While the impact on

overall cell performance was probably small, impedance spectra at OCV showed a considerable increase of the gas conversion and the low-frequency anode surface process resistance for both cells in this time period (see Table II). This behavior is due to the dependency of both processes on the steam content.[35,36]. Since the water bubbler temperature did not change between 140 and 640 h, a comparison of these spectra can be used to assess the cell degradation more accurately at identical boundary conditions.

Between 140-640 h, the degradation of the cell with 0.5 µm thick CGO was mainly caused by an increase in ohmic (+12 mΩ•cm^2) and air electrode resistance R_C (+14 mΩ•cm^2), while the lower frequency process resistances R_{GC} did not change. This behavior was similar for the cell with 0.3 µm thick CGO. However, in the impedance spectra of this cell capacitive interference phenomena occurred at frequencies >10^3 Hz that hindered the exact determination of the resistance values (spectra in Fig. S1).

Between 140-640 h, the cell with 0.15 µm CGO showed an increased ohmic resistance degradation (+32 mΩ•cm^2) in comparison to the cell with 0.5 µm CGO barrier layer (+25 mΩ•cm^2). In addition, in the cell with 0.15 µm CGO barrier layer the cathode process P_C of at 10^3 Hz showed an increased degradation between 140-640 h (+30 mΩ•cm^2). Its initial resistance value of 18 mΩ•cm^2 at 0 h was even lower than the one at 140 h (23 mΩ•cm^2) confirming the gradual degradation of the process over the course of the experiment. The initial resistance values of the process P_C at 0 h were both higher than the one of the cell with 0.5 µm thick CGO (8 mΩ•cm^2 at 0 h, 11 mΩ•cm^2 at 140 h). Thus, the increase of the resistance of the high frequency process for the cell with 0.15 µm CGO was already present after manufacturing, but progressed to a greater extent during operation.

The peak frequency of this process coincided with the one that showed an increased resistance in the initial impedance characterization of the cell with 0.15 µm thick CGO layer in batch 2 (Fig. 5d). Thus, it is likely that the increase of the imaginary impedance in this frequency region was of the same origin. The impedance increase in this region is only visible for the cell with

the thinnest CGO interlayer, suggesting that it is related to the formation of $SrZrO_3$, which was shown to reflect in the polarization resistance in previous studies.[41-42]

Table II. Results from CNLS fitting of impedance spectra shown in Fig. 7 at OCV including resistance values R, and parameters Q_0 and n of the R-CPE element. For the cases where n<1, Q_0 was converted into the true capacitance C which is given in parenthesis.

	P_S	P_C			$P_{A,MF}$			$P_{A,LF}$			P_{GC}		
Cell (time)	R [mΩ•cm^2]	R [mΩ•cm^2]	Q_0 [mF•cm^{-2}]	n	R [mΩ•cm^2]	Q_0 [mF•cm^{-2}]	n	R [mΩ•cm^2]	Q_0 [s^n•cm^2•Ω^{-1}] (true capacitance C [F•cm^{-2}])	n	R [mΩ•cm^2]	Q_0 [F cm^{-2}]	n
0.15 µm (0 h)	452	18	2	1	12	24	1	24	1.65 (0.93)	0.85	484	3.69	1
0.15 µm (140 h)	454	23	1.5	1	21	11.3	1	27	0.76 (0.38)	0.85	570	3.21	1
0.15 µm (640 h)	486	53	1	1	22	22	1	22	0.54 (0.25)	0.85	579	2.74	1
0.5 µm (0 h)	443	8	6	1	12	35	1	17	1.3 (0.66)	0.85	157	2.8	1
0.5 µm (140 h)	438	11	2.43	1	20	14.27	1	24.7	0.54 (0.25)	0.85	220	2.64	1
0.5 µm (640 h)	463	12	7.9	1	21.7	25.45	1	23.2	0.825 (0.41)	0.85	222	2.56	1

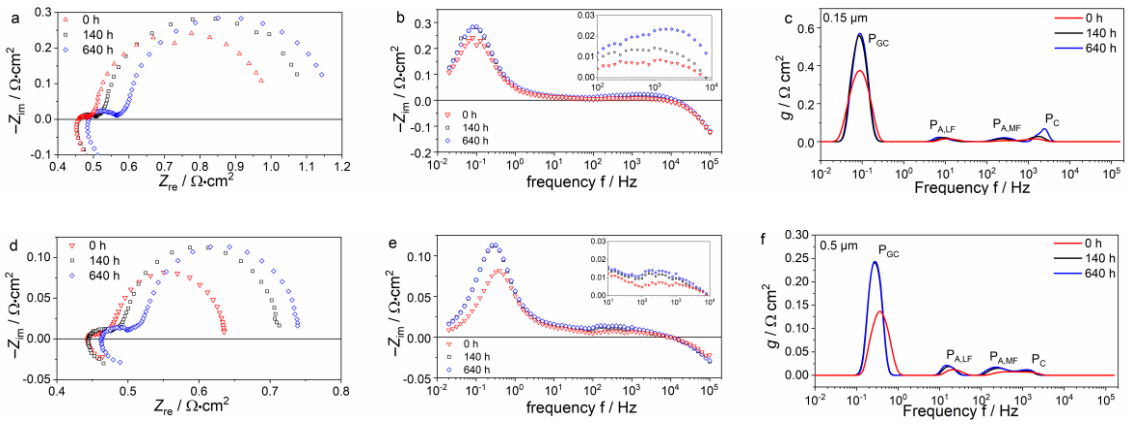

Fig. 7: Nyquist, imaginary impedance and DRT plots at 0 h, 140 h and 640 h of durability test 1 of (a-c) the cell with 0.15 µm thick interlayer and (d-f) the cell with 0.5 µm thick interlayer.

Second batch over 815 h - During the durability test at 0.5 A•cm^{-2} over 815 h, the oven temperature was accidentally decreased to 800 °C between 315-550 h and afterwards set back to the nominal oven temperature of 860 °C. The cell with 0.15 µm thick CGO layer showed lower initial operating voltage in the durability test (0.769 V) than the other cells (0.809 V for the cell with pre-calcined 0.5 µm thick CGO layer, 0.801 V for the cell with 0.3 µm thick CGO layer). However, the voltage degradation values were very small for all cells (see Table I), which showed values between 9 mV (11 mV/kh) and 11 mV (13.5 mV/kh). The observed voltage degradation values were not sufficiently different to clearly identify any dependency on CGO layer. In any case, it can be concluded that the main degradation of the YSZ/CGO interface occurred during the manufacturing and not during cell operation in this test which is consistent with observations made on ASC. [9, 18-19]

3.3 Post-mortem analysis

All cells were investigated by SEM/EDX after cooling down. Representative images of the LSCF/CGO/YSZ interface of the cells from the second durability test are shown Fig. 8. The SEM image in Fig. 8a indicates a discontinuous coverage of the electrolyte by the 0.15 µm thick CGO layer. The EDX mapping in Fig. 8b confirms the presence of a considerable amount of Sr at the CGO/YSZ interface indicating the formation of a Sr-containing secondary phase, likely

$SrZrO_3$. The Sr signal at the interface was very strong along the interface, suggesting the correlation of the formation of a continuous secondary phase and an associated severe performance loss.

The SEM cross-section image of cell with 0.3 µm CGO in Fig. 8c suggests that the PVD CGO covered the whole electrolyte surface and formed a dense layer. The corresponding EDX mapping in Fig. 8d indicates Sr at the CGO/YSZ interface in some spots, however, not continuously along the interface. The EDX mapping of the cell with pre-calcined 0.5 µm CGO interlayer in Fig. 8f shows a nearly pristine CGO/YSZ interface indicating no or little $SrZrO_3$ formation. EDX analysis of the 0.5 µm interlayer without pre-calcination from the first durability test over 640 h was also carried out. The respective images (Fig. S2) show a Sr-free CGO/YSZ interface that is comparable with the one in Fig.8f. These results confirm the hypothesis that cell performance deteriorates significantly upon the formation of a continuous $SrZrO_3$ layer.[42]

By removing the LSCF electrode from all cells, it was possible to investigate the CGO layer and the CGO/YSZ interface by XRD. For all cells, the diffraction peaks were identified as $(Ce,Gd)_{1-x}Zr_xO_{2-\delta}$ and 3YSZ similarly to that in Fig. 3, and the peak positions of this phase coincide with the ones directly after annealing at 1040 °C, indicating no further progression of interdiffusion during operation at lower temperatures. The diffraction intensity of these peaks increased with increasing CGO layer thickness, while their diffraction angle nearly stayed the same for all thicknesses. This suggests the interdiffusion of Zr^{4+} ions across the entire CGO layer thickness in all cells. For all samples, an additional phase was observed in the diffractograms that fits to the $SrZrO_3$ phase as suggested in the EDX mapping. In comparison to the $SrZrO_3$ phase from the database, these peak positions are observed at higher angles, that is, the lattice spacings are smaller than that of $SrZrO_3$. This could be explained by the substitution of smaller La^{3+} ions into the Sr site of the $SrZrO_3$ perovskite; ionic radii of La^{3+} and Sr^{2+} are 1.36 and 1.44 Å, respectively, for CN=12 on the A site.[43] By comparing the diffraction

intensities of $SrZrO_3$ (particularly at 55° or higher) it can be concluded that the $SrZrO_3$ layer is indeed thicker with thinner CGO coatings, confirming the observations made by EDX in Fig. 8.

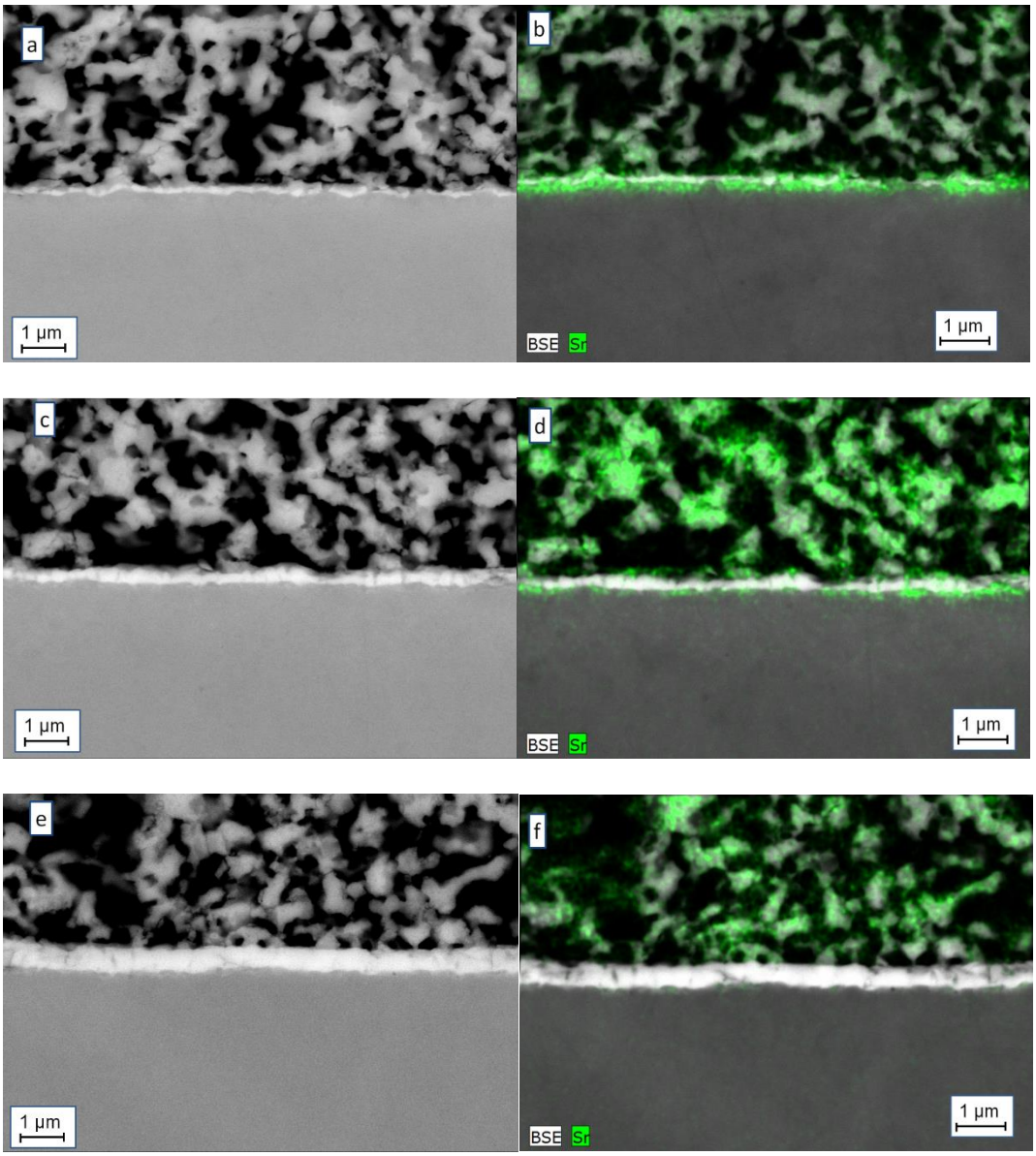

Fig. 8: Post mortem SEM/EDX analysis of the CGO/YSZ interface of the cells of the second durability test with (a+b) 0.15 µm,(c+d) 0.3 µm, and (e+f) 0.5 µm thick pre-calcined CGO layers.

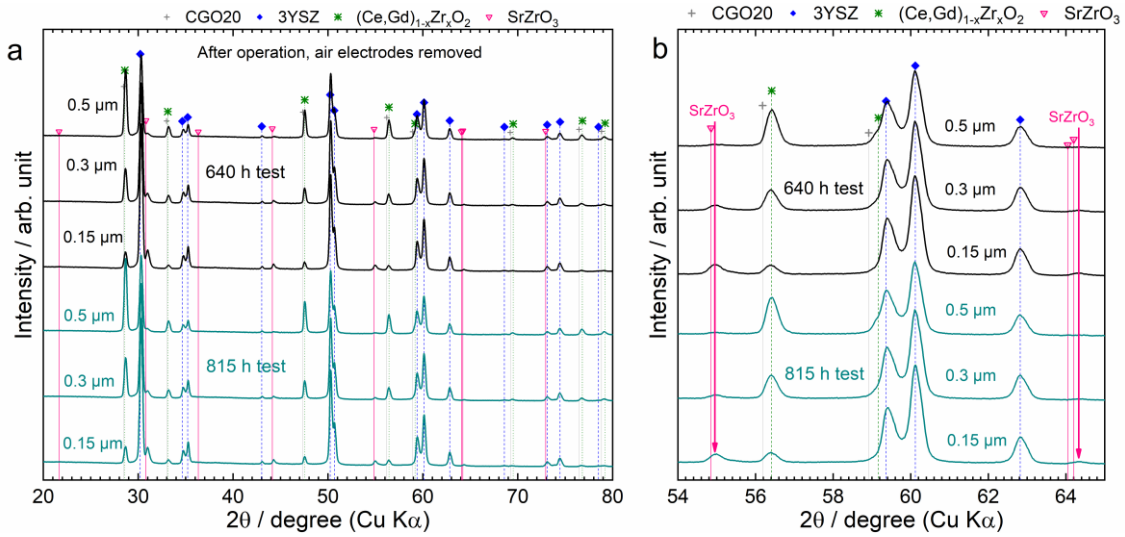

Fig. 9. θ-2θ X-ray diffractograms of all cells with different CGO layer thickness after operation after removal of the LSCF air electrodes. The upper three curves show the cells after the 640 h test, the lower ones the cells after the 815 h test.

Discussion

The present study shows that the spatial distribution of Sr-containing secondary phases (probably $SrZrO_3$) at the CGO/YSZ interface significantly affected the performance of 3YSZ-based ESC and was influenced by the thickness of EB-PVD CGO barrier layers.

Dense EB-PVD CGO interlayers with a thickness of 0.5 µm were effective to fully prevent Sr diffusion via gas phase and Sr diffusion through the layer itself. At 0.15 µm thickness, a $SrZrO_3$ phase was still formed at the CGO/YSZ interface, either during manufacturing or during operation. Transport then likely occurred via the grain boundaries, since the grain boundary diffusion coefficient of Sr in CGO20 is 5 orders of magnitudes higher than the bulk diffusion coefficient.[17, 44-45]

A clear correlation between the formation of a Sr-containing secondary phase at the CGO/YSZ interface and increased polarization resistance could be observed. This seemed to be the case only when the secondary phase layer was continuous as in the samples with 0.15 µm thick CGO layers. Discontinuous secondary phase layers as in the cells with 0.3 µm thick CGO layers had

neither a significant effect on polarization resistance nor on cell performance. This has also been observed by Szasz et al. to be the case for $SrZrO_3$ formation after studying ASC by means of FIB/SEM and STEM/EDXS.[42, 46]

The increased cell resistance was caused by an increase impedance response at frequencies ~10^3 Hz. While this frequency range coincided with the one of the LSCF surface process, it was more likely that the observed secondary phase formation caused an additional interfacial resistive and capacitive contribution to the cell impedance. This hypothesis is supported by the shift of the corresponding peak to slightly higher frequencies in the DRT analysis which indicates the emergence of a second impedance feature at these frequencies that cannot easily be deconvolved. With an ionic conductivity σ_{ion} of ~10^{-5} S•m^{-1} ([47] at 750°C), an active area A of 16 cm^2 and an estimated thickness of the $SrZrO_3$ phase of d = 200 nm (Fig. 8b), an additional resistance $R = A / (\sigma_{ion}\, d)$ = 32 mΩ•cm^2 was calculated for the cell with 0.15 µm thick barrier layer. This is close to the values in Table II showing that the high frequency process P_C of the cell with 0.15 µm thick barrier layer after 640 h test was increased by 41 mΩ•cm^2 in comparison to the cell with 0.5 µm thick barrier layer. In general, all materials show a relaxation behavior due to the coupling of conductivity σ and permittivity. The relaxation frequency f_0 of the process can be calculated according to $f_0 = \frac{\sigma}{2\pi\epsilon_0\epsilon_r}$ with ϵ_0 the vacuum permittivity and ϵ_r the relative permittivity (or dielectric constant). With an estimated ϵ_r of ~50 [48] and 10^{-5} S•m^{-1} [47, 49], f_0 = 3.6•10^3 Hz, which is consistent with the affected frequency range in the present study. Moreover, in a study on ASC a impedance range around ~10^3 Hz was affected when $SrZrO_3$ was formed.[50] This suggests that the observed high frequency contribution was caused by the low ionic conductivity of the $SrZrO_3$ phase, which is in contrast to a previous report suggesting that it is not the $SrZrO_3$ phase itself but its interface with the adjacent YSZ and CGO phases that inhibits the ionic transport.[51] However, there is also a literature study that reported strontium zirconate formation to reflect at frequencies ~10^6 Hz.[41] This can be explained by the dependency of the relaxation frequency of the $SrZrO_3$ phase on its exact composition due the

non-stoichiometry in the $SrZrO_3$ phase that can change after partial substitution of $SrZrO_3$ with aliovalent cations such as La, Fe and Gd. This can lead to the occurrence of a chemical capacitance and one order of magnitude lower relaxation frequencies at 800 °C for $Sr_{0.95}La_{0.05}ZrO_{3.025}$(LSZ) than for un-doped $SrZrO_3$.[49] Furthermore, the presence of Y-doped $SrZrO_3$ was recently reported in ASC to exhibit higher relaxation frequencies than $SrZrO_3$. [49, 51] In general, considerable differences of the affected relaxation frequency can be expected depending on the exact composition (3YSZ vs. 8YSZ, CGO10 vs. CGO20) of the used materials and their processing conditions. For the present LSCF|CGO20|3YSZ system, the emergence of an increased impedance feature at ~10^3 Hz can be used as quality control indicator to detect the formation of a continuous Sr-containing phase. In addition, the impedance response of the formed $SrZrO_3$ phase was shown to be divided into a higher frequency bulk, and a grain boundary contribution at approximately one order of magnitude lower frequencies.[49] However, at temperature above 750°C, the bulk contribution was reported to be dominant.

Insufficient CGO layer thickness and $SrZrO_3$ formation increased not only the polarization resistance, but the ohmic resistance as well. While several studies have observed that $SrZrO_3$ formation only increased the polarization resistance,[41-42] Constantin et al. also reported a reduction of the ohmic resistance upon introduction of a thin PVD CGO layer.[52] It is possible that the ohmic resistance contains additional contributions related to $SrZrO_3$ phase formation with relaxation frequencies of >10^5 Hz which is beyond the resolved high frequency limit in the present study.

The pre-calcination of the 0.5 µm thick PVD layer at higher temperatures was not required to achieve a dense diffusion barrier. This is in contrast to a study by Morales et al., where thermal pretreatment of a 1.8 µm thick PLD layer at 1150 °C was necessary to prevent diffusion along the columnar grain boundaries.[12] In their study, the thermal pretreatment also led to a lowered ohmic resistance of the ASC at 750 °C, which is consistent with our observations. However, the lowered ohmic resistance of the cell with pre-calcined 0.5 µm barrier layer was likely rather

due to beneficial effects of the pre-calcination step on the increased ionic oxygen transfer across the CGO layer than due to the reduced secondary phase formation. Increased ionic conductivity could be caused by changed grain size, film stress and microstrain in the CGO layer.[53-54] It is also possible that the annealing of the CGO layer led to a surface modification (as shown in Fig. 2b) and this had a beneficial effect on the contact with the LSCF electrode in the subsequent sintering step.

With regards to degradation of the LSCF/CGO/YSZ system during operation, studies investigating ASC operated at intermediate temperatures ~700 °C suggested $SrZrO_3$ formation to occur mainly during the manufacturing process.[9, 18-19] In contrast to that, Matsui et al. reported a sixfold increase of the $SrZrO_3$ phase after 400 h of operation at 1000 °C which was accompanied by an increase in ohmic resistance (but not necessarily caused it).[20] In the present study, the interface of a 0.5 µm thick EB-PVD CGO layer still remained completely free of SrO-ZrO_2 phase after ~800 h of operation at 860 °C. However, long-term stack experiments will have to be carried out for several thousand hours to determine if the formation of a continuous strontium zirconate layer can be excluded. In the case of a 0.15 µm thick CGO layer, electrochemical impedance spectroscopy showed that the degradation of the two durability tests mainly occurred during the manufacturing (batch 1, 640 h test) and the operation (batch 2, 815 h test), respectively. Based on the discussion above, it is likely that the difference was influenced by the time point of continuous $SrZrO_3$ formation related to the manufacturing process. One difference between the two cells with 0.15 µm thick barrier layer could originate from the difference in LSCF air electrodes, for which different inks were used. It was confirmed that the composition of the two powders was the same and no secondary phases could be observed by an XRD analysis of the two inks in Fig. S3. Electrodes in batch 1 were slightly thicker (24.5 µm vs. 20.2 µm) and had a denser microstructure than the electrodes in batch 2, as illustrated in Fig. S4. This could have had an effect on the amount of Sr that diffused across

the barrier layer during manufacturing and could explain the different time points of the formation of a continuous $SrZrO_3$ phase layer.

There is good reason to assume that the decreased CGO layer thickness and the lowered processing temperature during EB-PVD decrease residual stress in the cell structure and, thus, improve the mechanical properties of the cell.[29] According to eq. 2, the residual thermal stress of a PVD CGO layer at room temperature can be expected to be ~20 % lower than a screen-printed and sintered CGO layer. These values are derived based on the conditions: (a) the thermal treatment for air electrode processing at 1040 °C corresponds to the stress-free state of the PVD-CGO layer (see discussion above), (b) the screen-printed CGO layer is fired at 1300 °C, (c) the density and thickness of both CGO layers are identical. In the present case, the higher porosity and thickness of the screen-printed CGO layer might also influence the residual stress in the coating. All in all, it is expected that the reduction of residual thermal stress can contribute to mechanical strength enhancement of the cell.[30] The systematic investigation of these thermo-mechanical effects will be the focus of future work.

4. Summary and conclusions

In an effort to improve the mechanical strength properties of ESC, thin film CGO interlayers were integrated into state-of-the-art 5x5 cm^2 large cells as interdiffusion barriers via EB-PVD. 2 µm thick CGO layers coated on 3YSZ substrates developed macroscopic channel cracks after annealing at 1040 °C due to residual stress. 0.5 µm thick CGO layers remained crack-free. Subsequently, cells with CGO layer thicknesses between 0.15 and 0.5 µm were electrochemically investigated at 860 °C by means of current-voltage characteristics and impedance spectroscopy. In addition, two durability tests were carried out for 640 h and 815 h, respectively. Cells with 0.15 µm thick CGO interlayer showed a decreased performance after manufacturing that was reflected by an increased LSCF electrode resistance at frequencies of 10^3 Hz. In one case, also an increased ohmic resistance was observed. The lower performance

could be correlated with the formation of a continuous $SrZrO_3$ secondary phase at the CGO/YSZ interface. Cells with CGO layer thicknesses of 0.3 µm and 0.5 µm showed similar performance and degradation rates. Locally confined $SrZrO_3$ formation was observed in the case of 0.3 µm thick CGO interlayers. 0.5 µm thick CGO interlayers were able to fully suppress secondary phase formation during manufacturing and operation. It is discussed that the thickness reduction and lowered fabrication temperature of the CGO interlayer can probably enhance the mechanical strength of the cells, which will be further investigated in future work

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