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Implementation of variable data rates in transceiver for free-space optical LEO to ground link

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ABSTRACT

FSO systems present many advantages like high data rate, license-free bandwidth and tap-proof communication allowing the download of vast amounts of data from LEO satellites. However, the atmospheric channel is quite challenging, because of spurious effects such as absorption, scattering and scintillation that in turn vary the link losses in correspondence to the elevation. In order to maximize the downlink throughput, it should start around 5° elevation. This leads to a design with suboptimal performance for higher elevations when constant data rates are used. Therefore, DLR is developing a system to adjust the data rate according to elevation and atmospheric channel conditions.
This data rate variation is achieved by determining the maximum rate for higher elevation and then for lowering the data rates a bit-level repetition is performed. The presented system enables a fast transition between the different data rates. Additionally, this system allows the satellite to transmit data at rates even lower than those nominally supported by the physical transceiver.
At the receiver side, the system complexity increases as it should be able to acquire, detect, and filter the signal for different data rates. DLR proposes a system that mirrors the operation of its transmitter counterpart by sampling the acquired signal at the maximum data rate. Then an FPGA processes the signal by majority decision algorithm followed by voting system that filters and detects the intended data rate in real-time. This enables replication and parallelization of the filtering and detection processes enabling the automatic detection of the received data rate. In order to provide noise stability, the transition between data rates is governed by a hysteresis process. This scheme allows the detection and selection of the proper data rate in the range of few microseconds for a system operating between 10 Gbps and 1.25 Gbps in steps of factor of 2, ignoring the propagation delays.

Keywords: Variable data rate, FPGA implementation, FSO, majority decision, LEO downlink

1. INTRODUCTION AND BACKGROUND

Free space optical communication offers various advantages compared to conventional RF like very high data rate, secure and license free communication [1]. FSO has gained popularity mainly in Low earth orbit (LEO) satellite to ground scenario as it enables to download abundance of data generated by earth observation satellites to ground in near real time. However, there are several challenges like cloud blockage [2], index of refraction turbulence (IRT) [3], atmospheric attenuations due to atmospheric absorption, Rayleigh and aerosol scattering [4], etc. For LEO to ground links, ground station and satellites need to track each other. During one contact path, elevation angle varies from low angle (at the beginning and end of the path) to maximum (at zenith). The elevation angles during one contact time are mostly lower (between 5°to 15°) [5] . At lower elevation angles the signal travels longer through the atmosphere therefore the signal suffers more from the atmosphere. As the elevation angle increases, the signal gets less affected by the atmosphere. Finally, towards the link termination the elevation angle decreases again. This variation of elevation angle during one path causes variation of link budget. In addition to varying link budget due to elevation, the weather condition could also vary the atmospheric effects during one link. Therefore, for a fixed rate system one needs to design a system that works in the worst condition using sophisticated coding and interleaving techniques. This will however result in waste of resources for the time when channel conditions are good. One of the optimum ways is to design adaptive system that can change the data rate as per the channel conditions and/or elevation. For LEO to ground scenario, data rate variation can be done simply by lowering the data rate for lower elevation angles. The orbit of LEO satellites can be predicted very well, therefore different data rates for different elevation angles can be either pre-programmed or varied as per the measured channel conditions [6].

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Data rate can be modified by varying the user data rate by altering the pulse length, symbol length, modulation order, etc. [7]. It can also be achieved by keeping the user data rate but just varying the channel data rate by adjusting the code rate (adding more redundancies to lower the data rates), retransmitting data with certain delay [7,8], etc. One of the simplest ways to lower the data rate is to increase the width of the pulse. This can be digitally implemented by simply repeating the bits at the transmitter side. At the receiver side the signal is sampled at maximum data rate and filtered. The filtering and voting algorithm to detect the data rate in real time is implemented in FPGA. The detailed description about the implementation and results are presented in later sections of the paper.

2. OPTICAL LEO DOWNLINKS

2.1 Optical channel

Transmitting a coherent directed optical beam in a point-to-point approach through free-space and the atmosphere sees various influences on the optical beam. The atmosphere can be seen as an incoherent (turbulent) medium with bubbles of air of different temperatures, which depends on height above ground and other meteorological parameters. The optical beam thus experiences variations in index-of-refraction which lead to deformation of the optical wavefront. These again lead to self-interference, varying the intensity distribution of the beam in the regime of centimeters to decimeters. These spatial structures heavily depend on the link geometry, length, turbulence strength progression along the link, and of course the optical wavelength [3].

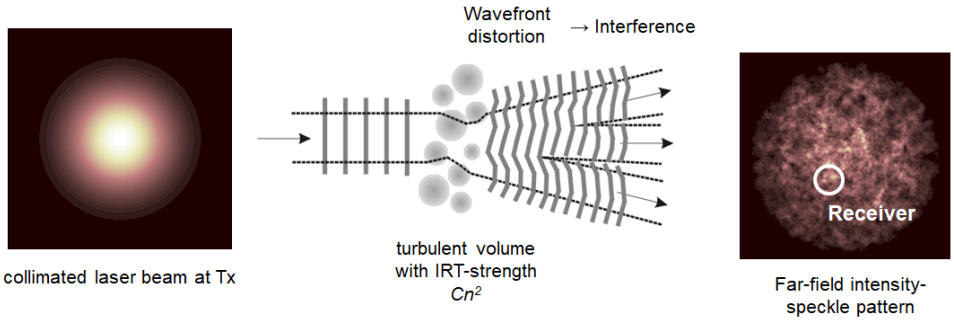

Figure 1. Effect of turbulence-induced self-interference of a coherent beam sent through Earth' atmosphere.

2.2 LEO downlink geometry

For the LEO satellites we assume circular orbits at a fixed height above ground (typically 400km to 900km), most often these are polar orbits to cover the whole globe in an Earth observation scenario. The satellite is then seen from starting horizon to its highest elevation and then symmetrically down to the ending horizon. Link durations are typically ten minutes or shorter. The momentary link elevation in a certain orbit dictates main free-space parameters as distance, atmospheric attenuation, and atmospheric turbulence impact. Figure 4 indicates relation between these parameters.

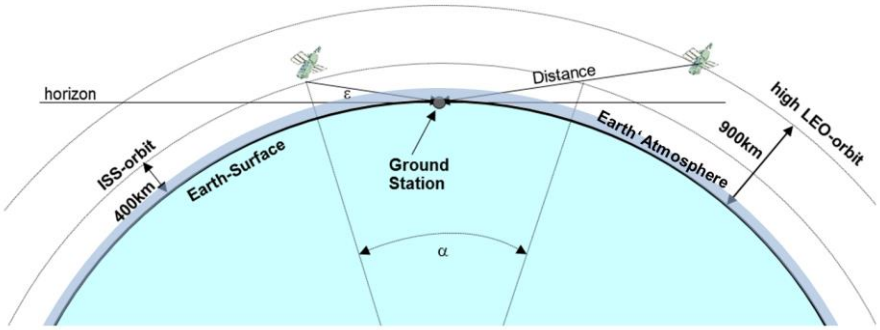

Figure 2. Typical geometry in LEO-downlinks from 5° to 5° elevation. Taken from [9]

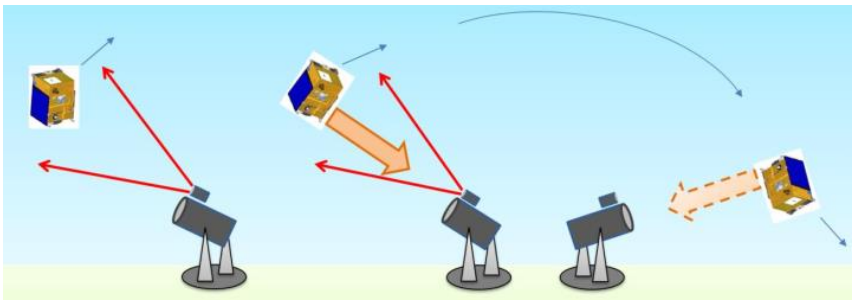

Figure 3. Optical LEO downlink (OLEODL) starting at minimum elevation near the initial horizon, via maximum elevation in the middle of the link, to end at same low elevation near the opposite horizon. Typically, 5° define the minimum elevation

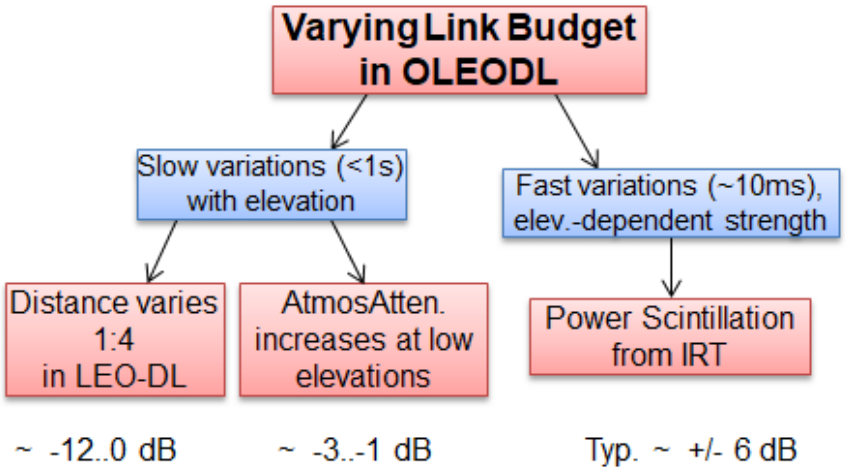

Figure 4. Elevation-dependent link attenuation and scintillation parameters.

Typical atmospheric attenuation loss plus free-space loss (distance) and typical scintillation loss (which depends on receiver aperture averaging) show ranges in a 500km orbit as indicated in Table 1. 5° is used as minimum and zenith as maximum elevation, and 15° is the typical mean elevation taking into account typical satellite visibilities above ground stations, as calculate elsewhere [5]. Scintillation loss as depicted in [9]

Table 1. Typical link loss parameters for 500km orbit altitude and 1% outage and 1550nm signal wavelength [7], [3].

	highest attenuation (5°)	**mean (15°)**	**lowest attenuation (zenith)**
Free-space loss (relative to least attenuation at zenith)	-12 dB	-9 dB	0 dB
atmospheric attenuation	-3 dB	-2 dB	-1 dB
scintillation loss (10 cm Rx)	-10 dB	-5 dB	-1 dB
scintillation loss (40 cm Rx)	-6 dB	-3 dB	-0.5 dB
SUM (10 cm):	-25 dB	-16 dB	-2 dB
SUM (40 cm):	-21 dB	-14 dB	-1.5dB

3. VARIABLE DATA RATE ALGORITHM

We have understood from previous sections that one of the efficient ways to cope with variable link budgets due to elevations and fluctuating channel conditions is to adapt the data rate accordingly. This section focuses on the algorithm where the system operates at maximum data rate at nominal channel condition and it can be reduced by factor *n* according to the channel conditions. Table 2 presents an example list of the data rates reduced from maximum data rate of 10 Gbps by various factors. For this paper we are considering On-Off Keying modulation, therefore one symbol will be referred as one bit for the rest of the paper.

Table 2. Data rates and reduction factor n

Replication factor *n*	1	2	3	4	5	*n*
Channel Rates	10Gbps	5Gbps	3.33Gbps	2.5Gbps	2Gbps	10/*n* Gbps

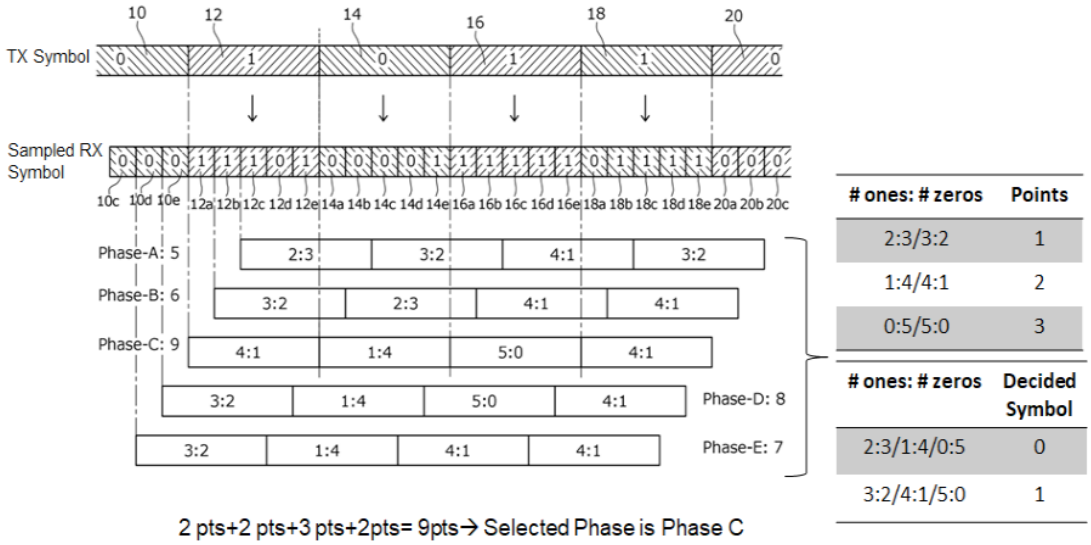

Figure 5. Example of majority deciding detection algorithm [10]

The algorithm presented here is based on a patent "DE102017202879A1 Verfahren zur drahtlosen seriellen Datenübertragung"[10]. At the transmitter side, data rate is lowered simply by increasing the pulse width. This can be achieved digitally by repeating the bits *n* times. This way, the channel data rate remains the same and only the user data rate is reduced. This avoids requirement of any changes in the receiver hardware. At the receiver, the clock shall run at maximum rate and low pass filtering is done using majority decision and the voting algorithm. This algorithm not only helps on decoding the original data by oversampling but also on selecting the correct phase as shown in Figure 5. In this figure, we define different phases (A, B, C, D, E), each corresponding to different possible data shifts inside the sampled bits. Figure 5 shows an excerpt of transmitted bit streams (for example 10^{th}, 11^{th}, .. 20^{th} bits) when the data rate is reduced by factor 5. Below the Tx symbol are the sampled received symbols at the receiver. Effectively at the receiver one original transmitted symbol is sampled 5 times (a - e). For example, the 12^{th} symbol is sampled five times 12a, 12b, 12c, 12d and 12e at the receiver. Ideally all samples should be the same at the right phase. However, because of the imperfect channel and clock synchronization, oversampled bits might be different. Therefore, majority decision can be done to recover original data bits. For example, if 3 or more of the sampled bits are zeros then it is decoded to one single zero bit. Similarly, if 3 or more of the sampled symbols are ones then it is decoded to a single one symbol. This is intuitive if the data rate factor *n* is an odd number. If *n* is even, there is a chance that we have equal numbers of zeros and ones, in such cases the symbols are decoded to zero in our implementation. In addition to the atmospheric attenuation, bits might be also shifted due to clock synchronization imperfections. If the sampling phase at the receiver is a bit off the majority decision might be completely wrong as it is using part of the one original bit and part of another. Therefore, we repeat the majority decision and voting algorithm multiple times with slightly shifted phases (Phase A, B, C, D and E in the figure above). For each phase, majority decision algorithm is run and points are assigned depending on how many resampled bits were zeros and ones. For the example above either 1, 2 or 3 points are given. If out of 5, 2 are zeros/ones

and 3 are ones/zeros then 1 point is assigned to the particular phase. If out of 5, 1 is zero/one and 4 is one/zero then 2 point is assigned, and if out of 5, all 5 of them are zeros/ones then point 3 is assigned. At the end for each Phase, these points are added to calculate the final score and the one with the maximum score is the winner Phase. In the example above, it is phase C. Therefore, the algorithm not only helps on deciding the bits correctly at lower rate but also can follow the phase drifting.

4. VARIABLE DATA RATE IMPLEMENTATION

This algorithm is being developed into two independent Intel Altera FPGA boards using the VHDL language. One FPGA was used as the transmitter whereas the other was used as receiver as shown in Figure 6. The modules containing the algorithm implementation, called VDR, are integrated into the system between the serializer-deserializer (SerDes) and the rest of the system so only the serial data (and thus the optical data) sees the effects of the variable data rate expansion-reduction. This means that the variable data rate only affects the physical layer of the communication stack directly. However, it is important that the transmitted data are scrambled or equivalent, prior their transmission to the VDR modules. This is required not only to ensure enough transitions for the clock and data recovery (CDR) to operate properly but also for the correct detection of the data rates. The implementation can be split into two main blocks, one for the data rate expansion in the transmitter and another one for the data recovery in the receiver.
In this section it is also important to understand the difference between channel bits and data bits. Data bits are those bits that contain user data. They are not affected by the variations in the data rate. Channel bits are bits transmitted in the channel at maximum rate. A data bit may consist of several channel bits.

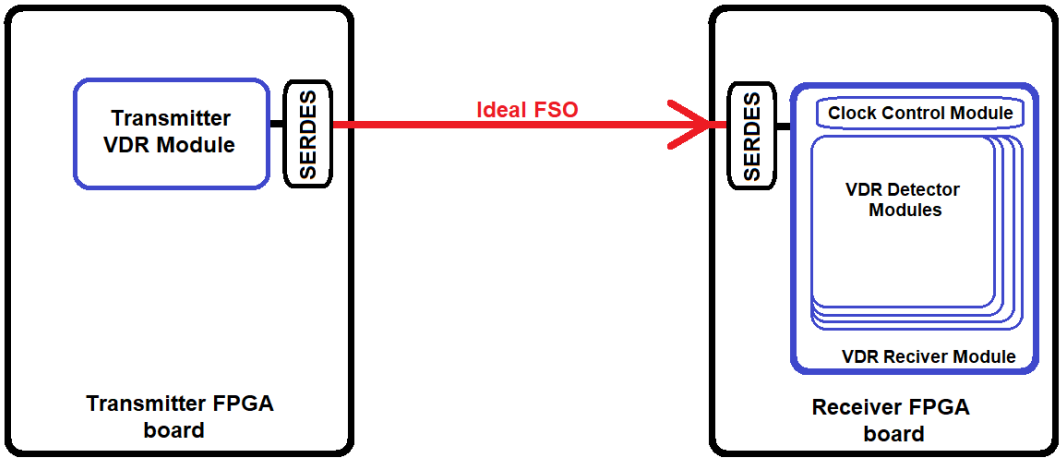

Figure 6. Internal structure in the FPGA. In blue the main blocks described in this section

4.1 Transmitter hardware implementation

On the transmitter side, the VDR module is the responsible to adjust the bit duration of the data in the serial line generating the different data rates. Since it has to operate at the highest data rate as well as the lowest, it needs a back-pressure control signal to indicate the rest of the system when the VDR module is ready to process a new data word.
In order to implement the bit replication, we need a replication factor for each intended data rate. Since the stepping between data rates has been chosen as a factor of 2, the replication factors (*n)* are 1, 2, 4 and 8 for the data rates of 10 Gbps, 5 Gbps, 2.5 Gbps and 1.25 Gbps respectively. These replication factors represent how many channel bits have to be produced out of each data bit. The VDR module will then take a data word and split it into *n* parts. Then, one by one, all the bits will be expanded by this replication factor forming a new word, with the same length as the input word. This means that the VDR module will require as many clock cycles to process a new data word as the intended replication factor.
This module has as a special a control signal as input to indicate the desired data rate. This signal is controlled by an external subsystem currently commanded by human interaction. The system also has to synchronize these commanding with the bit replication process to avoid a system corruption, especially when decreasing the replication factor, i.e. from 8 up to 1. This synchronization avoids changes in the data rate during the full processing time of a single input data word, but it does not consider any upper layer structure or protocol.

4.2 Receiver hardware implementation

On the receiver side, the VDR modules require a higher complexity. They have to receive data at an unknown data rate, thus they have to be analyzed for all possible data rates in parallel. This parallel analysis is done at the clock frequency required for the maximum data rate. In order to analyze each replication factor, the algorithm described in Section 3 is used. If a given phase of a given data rate scores higher than prefixed throughput for several consecutive data words, a data rate is detected and selected. Finally, if a new data rate is detected, a signal is triggered in order to indicate the synchronization systems that the data rate changed. Additionally, due to the limitations of the CDR systems in the FPGA, a new module had to be developed to follow deviations in the CDR frequency and then switch to a reference internal phase-locked loop (PLL). This module is needed in order to ensure a stable clock for both the high and lower data rates. All these processes are done in different submodules described below.

VDR receiver module

This module is the top component and it processes the incoming data buffering as much channel words as required by each of the different submodules. This means that for each replication factor it has to buffer as many channel words as the number of the replication factor. VDR receiver also provides control signaling to the VDR detectors indicating when new valid data is available for each of them. It is also in charge of analyzing the winning score of each of the VDR detectors and determining the data rate, and then it outputs the recovered data. In order to minimize the effect of spurious transitions between different data rates caused by noise in the channel, it implements a hysteresis mechanism to ensure that only stable transitions in the data rate are considered. The optimization of this hysteresis is still under analysis. It highly depends on the different channel conditions and it is one of the major contributors to the delay in the automatic detection of the data rate. Finally, this module also generates the required signaling to inform the synchronization system about a change of the data rate. This signaling is obviously controlled by the hysteresis process and only triggers when a new data rate is selected.

Clock control module

Clock control module ensures that the system always has a valid reference clock. It constantly compares the CDR frequency with the one provided by the internal PLL. These two frequencies are theoretically identical, but minor differences in both communication nodes make them differ slightly. This difference renders the PLL frequency unsuitable for recovering data when the system operates at factors 1 or 2. On the other hand, the CDR frequency, as it requires transitions in the incoming signal and channel bits, can present problems when reducing the data rate below factor 3. Therefore, this module requires the synchronization signaling provided by the VDR receiver but it also can generate its own when the system detects a significant difference in both frequencies. The clock switching ensures a glitch free transition between the clocks.

VDR detector modules

These modules contain the implementation of the patented algorithm [10]. Currently they implement four different replication factors, 1, 2, 4, and 8 but due to similarities in the implementation, the modules for factors 1 and 2, and the modules for factors 4 and 8 are similar respectively.

With factor 1 and 2, the module only compares the channel bits with its adjacent bits. In the case of a replication factor of 1, the correlation between any two consecutive bits should be significantly lower compared to the case when the replication factor is 2. In these cases, for the replication factor 1, a low score in the two measured phases is desired and no further action is required. For the replication factor 2, a high score is desired in one of the phases whereas in the other phase the score should be minimal. For determining the data bits, the odd channel bits are selected since in case of discrepancies between both corresponding channel bits, the system lacks further information to optimize the decision.

For the replication factors 4 and 8, it is important to notice that the system is operating with the internal PLL clock frequency. This means that time to time, depending on the deviation from both clocks on both communication nodes, the received data will present a random-like shifting. This shifting can be handled into these modules and will represent a shifting through the different phases that has to be considered since it could also rotate through all the phases. These rotations are handled by the system with the inclusion of some controlling signals to indicate the VDR receiver module if it has to provide the next processing word a clock cycle earlier later than usual. A clock cycle earlier means that the PLL frequency is slower than the transmitter real frequency and vice versa if the data has to be delivered one clock cycle later. Additionally, a phase monitor has been implemented to keep track of the phase. This control ensures that the proper

phase is being selected and it avoids jumps between not adjacent phases. In this case, the first and last phases are considered adjacent. In the example presented by Figure 5 the phases A and E are first and last phases respectively.
Scoring in each of the phases is done in two steps. Firstly for each phase, the system calculates how many ones and zeroes are in each consecutive group of channel bits of a size defined by the replication factor. Then, in the second step all the individual points for each candidate of the data bit are added in order to determine the winning phase. This process requires adding several numbers and thus it is prone to optimizations to reduce the maximum delay required. In this sense, we have implemented an adding structure based on the binary tree concept. This tree has been inverted and in the first level all the scores of the candidates to data bits are added in pairs. In the second level, the results from the first level are added together in pairs and so on for the other levels until we produce a single number which is the score of the given phase. In this *adding tree* the implementation limits the size of the added numbers in order to optimize its implementation. This limit can be calculated during the design by checking how big the partial scores can go in each step of the tree. Finally, the resulting scores of each phase are compared, together with the current phase and then, the winning phase is computed. This resulting phase can only be the same as the previous phase or an adjacent one. This condition only applies to the detected data rate. This is done in order to facilitate the detection of a change in the data rate since when the system is operating at a given data rate, the phase calculated for a different data rate is not reliable.

Finally, two extra modules have been implemented. The first one is implemented in the transmitter side and it allows the user to manually change the data rate through some switches in the FPGA board. It samples the switches and avoids metastability issues in the commanding signals for changing the data rate. The second module is implemented on both boards. On the transmitter side, it triggers a control signal that is transmitted through a low speed I/O pin to the receiver board. On the receiver side, this control signal is sampled and used to synchronize the data collection for acquiring the presented results. This signal has been added only for synchronizing the results acquired during the laboratory testing and measuring the detection and transition delays presented in the results section. This means that the system can work independently of this signal.

5. RESULTS

The system has been tested in laboratory conditions with an ideal channel without introducing noise or outages. In this case, we used confined optics through optic fiber as a channel. SignalTap tool from Intel Quartus was used for monitoring and sampling the internal signals on the receiver side. A control signal commanded from the transmitter has been used to trigger the sampling and thus enable an accurate measurement of the delay between the change in the data rate at the transceiver and its detection on the receiver.

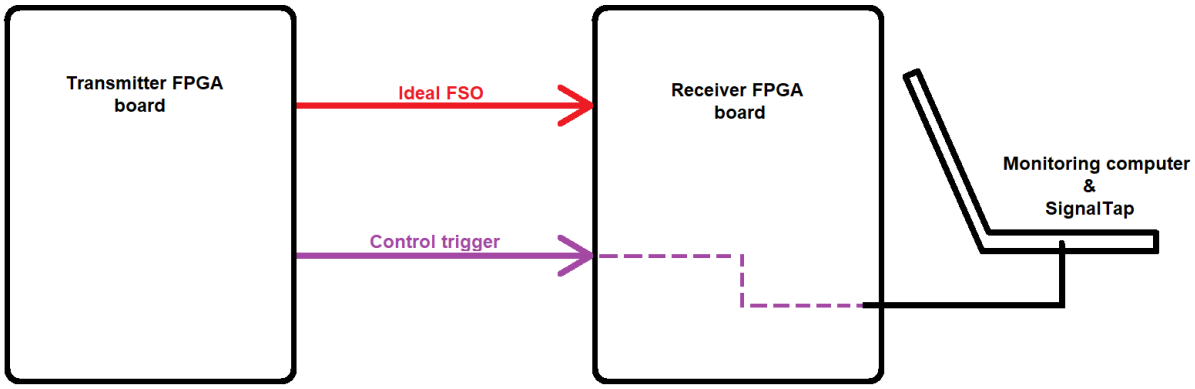

Figure 7. Laboratory setup

Figure 7 presents the experimental setup. As already indicated, the control trigger signal can be removed without affecting the operation of the system since it is only used for synchronizing the data collection. With this configuration, all the different transitions between different data rates were tested and the delays they presented between the control trigger, and the detection of the data rate were measured. Table 3 shows the measured preliminary results for each transition presenting the minimum and maximum delay registered by SignalTap. These results show that the maximum transition time, although susceptible to optimizations, is always below 100 µs, which for most of the FSO channels, can be considered at least 1 order of magnitude lower than the coherence time of the channel. In this previous assessment we

exclude the case of going from 2.5 Gbps down to 1.25 Gbps. This is important because FSO communications systems that provide protection against the outages in the channel can also cope with the losses caused by the change in the data rate.

Table 3. Measured delays for each transition between different data rates

Data rate origin → destination	Minimum measured delay	Maximum measured delay
10 Gbps → 5 Gbps	208 ns	237 ns
10 Gbps → 2.5 Gbps	221 ns	246 ns
10 Gbps → 1.25 Gbps	1968 ns	14486 ns
5 Gbps → 10 Gbps	355 ns	454 ns
5 Gbps → 2.5 Gbps	320 ns	336 ns
5 Gbps → 1.25 Gbps	19296 ns	41600 ns
2.5 Gbps → 10 Gbps	1155 ns	3225 ns
2.5 Gbps → 5 Gbps	566 ns	912 ns
2.5 Gbps → 1.25 Gbps	> 46000 ns	< few seconds
1.25 Gbps → 10 Gbps	1808 ns	2336 ns
1.25 Gbps → 5 Gbps	1174 ns	1459 ns
1.25 Gbps → 2.5 Gbps	960 ns	979 ns

Analyzing the results in detail, we have observed an issue while reducing the data rate down to a replication factor of 8 i.e. 1.25 Gbps. The cause of this issue is still under investigation. This issue is most evident when going from factor 4 down to factor 8 in which, although we have seen that the transition takes place, we could not measure its duration. We could only assess that it last longer than our observation window of 46 µs but below few seconds, which was the time needed to manually trigger SignalTap to confirm that the transition took place.
Another optimization area is in the transitions from the internal PLL clock at the receiver to the CDR clock. This transition happens when reducing the replication factor from 4 or 8 down to factors 1 or 2. The measured delay is in a range close to microseconds, when we should expect it to be in the range of hundreds of nanoseconds.
As a final note, despite the further optimizations analyzed, the system has proven its reliability since each commanded transition was eventually detected.

6. CONCLUSIONS AND FUTURE WORK

Through this paper, we have presented a method and some guidelines for its implementation in an FPGA for a variable data rate scheme for LEO downlinks. The system is still under development and therefore susceptible to optimizations and improvements. However, initial laboratory results have been proven reliable. In combination with an error correction system suitable for the outages of the optical channel, the losses induced by the delays and transitions in the data rate should have a negligible impact.

Some of the advantages of this variable data rate method are that it can cope with the high dynamic range of received power in LEO downlink scenarios. The reduction in the data rate also improves the stability in the signal improving the signal to noise ratio for lower, or challenging, elevation angles during the transmission. Additionally, this method could allow in the future satellites with high data rate transmitters to communicate at lower rates with ground stations that can only receive data at lower rates and vice versa.

The presented system has been optimized for operation at 10 Gbps as the maximum data rate but their structure is rate independent, so it can be migrated to slower systems where the replication factors are maintained and will work. For migrating the system into faster systems, timing constrains have to be considered. Additionally, due to its modular structure, it can be replicated and concatenated to expand the number of data rates supported by a system.

Currently we are analyzing and optimizing the challenges presented in Section 5. We are also working towards newer results, including a channel emulator for the optical channel in order to assess the stability of the system against outages and noise. Finally, some options to formally test the concatenation of multiple modules to expand the data rate range are being studied.

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