An Integrated Radar Tile for Digital Beamforming X-/Ka-Band Synthetic Aperture Radar Instruments

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Abstract—This paper presents the first experimental assessment of a highly integrated dual-band dual-polarized antenna tile designed for synthetic aperture radar (SAR) digital beamforming (DBF) satellite applications. The demonstrator described in this paper is the first comprehensive experimental validation of an RF module providing the X-band and Ka-band (9.6- and 35.75-GHz) operation with custom downconversion stages. All the antennas, transitions, and downconversion chips are integrated in the same antenna tile fabricated using a customized 15-layer high density interconnect process. The designed tile goes to the limits of the proposed technology and for the high trace density and for the size of the vertical transitions. The proposed results represent the state of the art in terms of compactness for a DBF SAR RF module even though the demonstrator was manufactured with a standard low-cost technology. The experimental assessment proves the validity of the proposed manufacturing and integration approaches showing a substantial agreement between the performance of the individual blocks and of the integrated system.

Index Terms—Antenna, digital beamforming (DBF), integrated systems, radar, small satellite, synthetic aperture.

I. INTRODUCTION

EARTH observation (EO) is one of the fastest growing sectors in the space market [1]. Main growth drivers for EO data and services are not limited to defense and security applications but include also mapping of infrastructure and natural resources, monitoring and responding to natural disasters, and addressing public health and maritime safety. New applications are constantly developed requiring competitively priced technological solutions which should lower the cost of both sensors and satellite platforms while providing increased

sensitivity, resolution, and coverage. In this perspective, small satellites represent a relevant opportunity that is being undertaken by several satellite operators.

However, even though optical sensors can be easily integrated in cube sats, the use of synthetic aperture radars (SARs) has been typically precluded to small satellite platforms due to the inherent volume and mass limitations. Recently, in [2], it has been demonstrated how high-resolution wide-swath SAR imaging sensors could be designed employing digital beamforming (DBF) techniques in a receive-only multistatic satellite constellation. The introduction of these architectures allows the development of new SAR systems where a single master satellite illuminates the surface of the earth and a constellation of small satellites equipped with compact DBF SAR sensors scans the scattered field following the echo on ground [3]. The implementation of this new architecture relies on the possibility to exploit highly integrated DBF SAR sensors. However, existing DBF SAR spaceborne instruments do not match these compactness and modularity requirements [4]. Several concurrent research activities are tackling the development of compact DBF SAR sensors proposing different solutions. For example, in [5], it is presented a three-channel DBF SAR antenna providing dual-polarized L-band operation. This system uses a hybrid analog beamforming/DBF scheme where groups of four subarrays share the same digital channel. Another possible implementation is being developed within the framework of the EU Project "DIFFERENT" [6]. The challenge of this project is to implement a receive-only SAR sensor capable to acquire data in two bands, namely, in the X-band and Ka-band, in the single-pass full polarimetric mode. The adopted center-band frequencies in the X-band and Ka-band are 9.6 and 35.75 GHz, respectively. In the proposed architecture, a DBF feed array with 60 digital channels is used to illuminate a deployable reflector [7], [8], as shown in Fig. 1(a). High resolution is achieved combining the benefits of the multistatic constellation with the multichannel capability enabled by the DBF technique and with the dual-band single-pass full polarimetric acquisitions [9]. Moreover, the flexibility of this SAR receiver platform will support the realization of a variety of spaceborne SAR missions [10].

The feasibility of this approach relies on the capability to realize a highly integrated and modular DBF reflector feed. The required compactness is reached distributing different components into three boards named: 1) RF board; 2) analog-to-digital converter (ADC) board; and 3) DGT board

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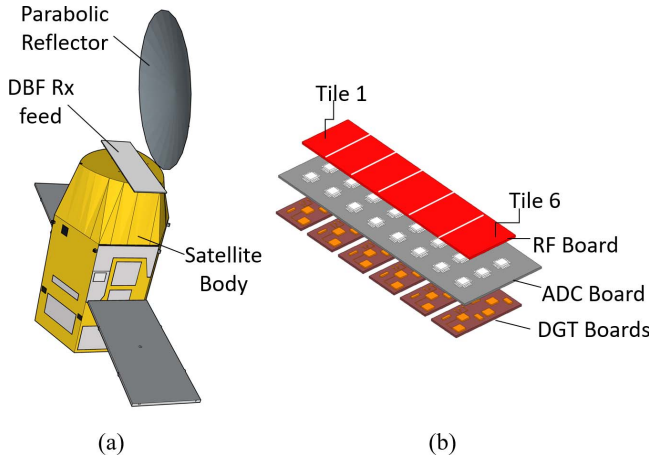
Fig. 1. DBF SAR architecture. (a) Pictorial view of the DBF Rx SAR instrument integrated on a satellite. (b) Tile-based architecture of the DBF Rx SAR feed.

[see Fig. 1(b)]. The basic design principles underpinning the adoption of the proposed configuration are described in [6] where the simulated and measured results of the isolated subsystems of the RF board are also presented. This paper expands upon the previous work by providing an extensive report on the integration strategy along with a detailed numerical and experimental assessment of the fully assembled RF-board tile. This work, thus, demonstrates the radar tile feasibility by combining the blocks presented in [6] and by presenting the experimental results representative of the complete RF chain. As it will be shown, the integration of the tile subsystem was made possible by simplifying the RF-board stack-up and its manufacturing process.

This paper is organized as follows. Section II describes the architecture of the SAR instrument. Section III illustrates the integration strategy and the board stack-up. Sections IV and V present the configuration and the integration of the microwave monolithically integrated chips (MMICs) and of the antennas, respectively, while Section VI describes the most critical manufacturing issues. Finally, the measured results are presented in Section VII.

II. SAR INSTRUMENT ARCHITECTURE

The architecture of the proposed SAR instrument, shown in Fig. 1(b), is designed to guarantee a modular approach easily adaptable to different mission contexts. One of the fundamental building blocks is the antenna tile which embeds dual-band dual-polarized array cells and MMICs which operate the downconversion of the RF signal to an intermediate frequency (IF). Combinations of tiles constitute the RF board which can be used to form a feed array reflector [11]. As shown in Fig. 2, each tile is a self-consistent module providing 10 IF output channels, 8 in the Ka-band, and 2 in the X-band. It accommodates as follows.
- One H-polarized X-band antenna.
- One V-polarized X-band antenna.
- The 16 Ka-band dual-polarized antennas arranged in subarrays of four elements.
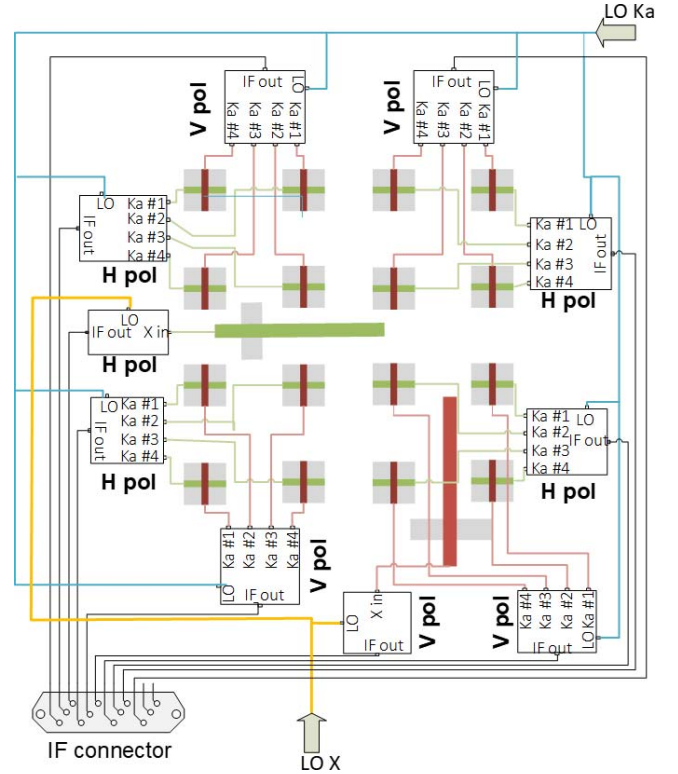- Two MMICs at the X-band (for V-polarized signals and H-polarized signals).

Fig. 2. Architecture of the single radar tile.

- Eight MMICs at the Ka-band (four for V-polarized signals and four for H-polarized signals).
- Two local oscillator (LO) distribution networks for the two bands (X and Ka).

The function of the chips is to amplify and downconvert the received V-pol and H-pol signals to an IF. For the case at hand, two types of MMICs are employed. Hence, each X-band antenna is connected to a single-channel MMIC while the signal received by each 2×2 subarray of the Ka-band elements in a single polarization is power combined and downconverted using a dedicated chip. The IF signals generated by each chip are routed, through an output IF connector, to the ADC board where they are digitalized. Finally, the digital data corresponding to each polarization and to each radiating element are weighted and combined in the DBF network implemented using six digital boards. The electrical connection between the boards shown in Fig. 1(b) is ensured by special connectors that allow a simple mounting/dismounting of the modules also during the assembly and testing phases. This approach is extremely important to experimentally assess the final demonstrator which embodies six tiles [Fig. 1(b)] and 60 digital channels.

III. STACK-UP VERTICAL DESIGN AND KEY BUILDING BLOCKS

This paper describes the design, manufacturing, and experimental validation of a single radar tile demonstrating the correct operation of the subsystem composed by several components integrated in a single board. The radiating elements, RF circuits, and MMICs are embedded on the same multilayer printed circuit board (PCB) to reduce the complexity
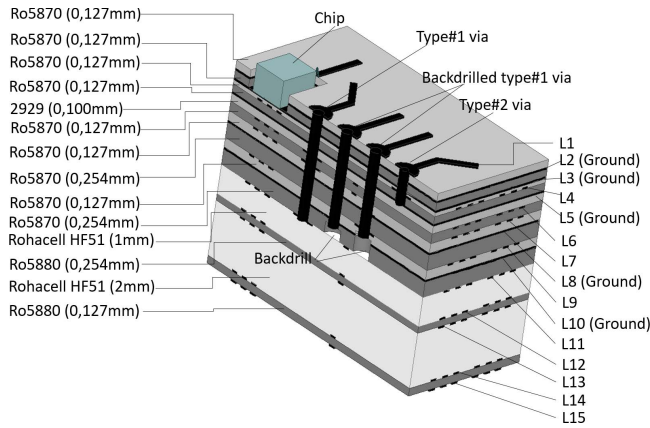
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Fig. 3. Stack-up employed to design the proposed RF-board tile. This figure shows the 15 copper layers (L1, L2,…, L15) and the dielectric cores. A special fabrication procedure has been used to avoid the use of prepreg between core layers.

Fig. 4. Quasi-coaxial vertical transition between layers L1 and L9, realized with a central backdrilled via.

of the system obtaining an extremely compact component. In general, the required high density of the manifold could be implemented using low-temperature cofired ceramics (LTCC) [12] that can guarantee low loss and a variety of vertical transitions. However, this technology is costly, and manufacturing reliability cannot be guaranteed over large areas [13]. For this reason, in this paper, the challenge was to design a highly dense PCB using a standard industrial process yet guaranteeing the required level of density and limiting the losses. A first example of complex stack-up for this application was presented in [6]. However, this configuration allows only the integration of a subset of the tile components. In this paper, the previously presented buildup is simplified with the objective to reduce the manufacturing complexity and costs while guaranteeing the full tile integration. This goal has been achieved through the minimization of the layers' number, of the blind and buried vertical interconnect access (via) typologies, and of via aspect ratio. However, although the reduction of the fabrication steps limits the manufacturing cost, it has a direct impact on the electromagnetic performance of all the integrated components, thus requiring a tradeoff between technological constraints and electromagnetic requirements. Details about this optimization process are given in Section III-A which describes the solutions employed to design the antennas and their vertical transitions using a simplified buildup.

Fig. 3 shows the proposed stack-up used to design the radar tile where black areas refer to metallization, dark gray areas refer to dielectric substrate, light gray areas refer to foam spacers, and black circles correspond to metallized vias passing through the layers. The technology used in this paper is based on an advanced multilayer PCB technology, which includes 15 layers of metallization. Cavities are carved between layers L1 and L3 to accommodate MMICs. Layers between L9 and L15 have been used to integrate the antennas (see Section V). Layers L6 and L7 are employed to route the six output IF channels and to provide the power distribution between the integrated chips. Layer L4 implements two LO distribution networks for the X-band and Ka-band (see Section IV-A). Layer L1 is used to route the IF signals
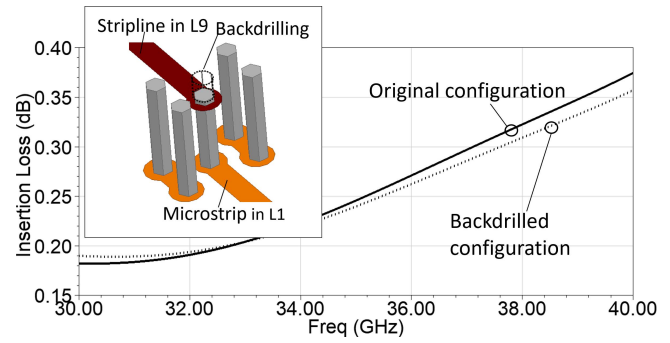
generated by each chip (see Sections III-B, IV, and V-C) and for the integration of input and output connectors.

With respect to the stack-up model employed in [6], in the one here proposed, the types of vias are reduced from 4 to 2.

- *Type#1:* From L1 to L11.
- *Type#2:* From L1 to L5.

In fact, when necessary, backdrilling is used to remove the lower part of type#1 via (as shown in Fig. 3) to allow the connection also from L1 to L9 and L10. Backdrilling is a controlled depth drilling technique that removes the part of the via with conventional numerically controlled drill equipment. As a further simplification, the proposed stack-up has been manufactured using a fusion technique which allows bonding the core layers without using prepregs. In this way, a more homogeneous layup, without unwanted dielectric constant variations in the vertical direction, is available for the integration of the high-frequency antennas and transmission striplines. This technique also reduces the roughness of the printed striplines as all the metal layers can be based on the rolled copper. For the case at hand, core layers are based on Rogers Ro5870 and Ro5880 substrates. These materials present the relative dielectric permittivities of 2.33 and 2.2, respectively, while the loss tangents are equal to 0.0012 and 0.0009, respectively.

A. Analysis and Simplification of the Vertical Interconnections

One of the most critical components in the design of the RF-board tile is the vertical transition between antennas and chips which are placed on the opposite sides of the stack-up. To avoid high insertion losses (ILs), these interconnections were realized using a quasi-coaxial configuration [14], [15], where a central signal via is surrounded by a number of ground vias (see image inside in Fig. 4). Ground vias form an outer conductive boundary within which the field configuration is similar to that of a coaxial transmission line. In order to simplify the stack-up, in the proposed board, all transitions were realized employing a single via type, namely, type#1. However, this solution can be critical for the transition between Ka-band antennas on L9 and MMICs on L1. Indeed, a portion of signal via would extend beyond the stripline on L9, thus behaving as a stub. A simple and effective method to reduce the impedance mismatch caused by these stubs without
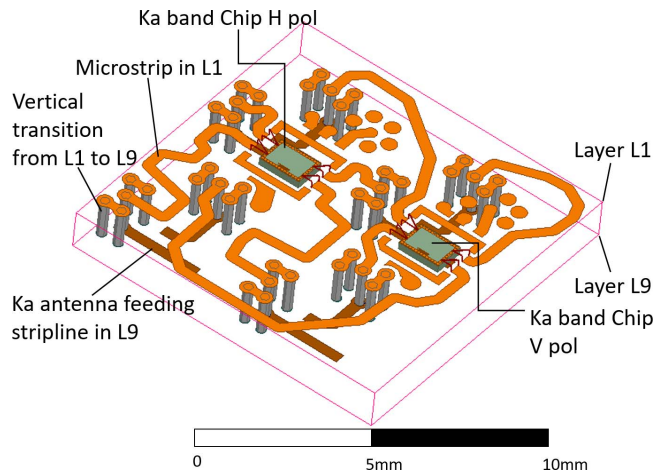
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Fig. 5.   Ka-band elementary cell composed. (Just layers L1 and L9 are shown.)

Fig. 6.   (a) Ka-band chip integrated in the top cavity. (b) X-band chip integrated in the top cavity.

changing the board buildup is to employ a backdrilling technique which removes a portion of the via from L11 to L9 with numerically controlled drill equipment. However, even in this case, the via stub can be reduce but not canceled. Indeed, in order to avoid the risk of disconnection between the via and the stripline in L9, the drilling machines have to be stopped at a safe distance of about 100 μm. Nevertheless, it has been evaluated that the remaining part of the stub and the dielectric discontinuity created by the drilled hole causes only an increase of 0.1 dB of ILs as it can be observed in Fig. 4 which compares IL of the original and the backdrilled configuration.

B. In-Phase Design of the Vertical Transitions and Routing

Fig. 5 shows the elementary 2×2 subarray of the Ka-band elements with the two MMICs used for the vertical and horizontal polarizations. The involved layers, as shown in Fig. 5, are L1 and L9 incorporating the antenna input ports and the MMIC access ports, respectively. The most critical factor in the design of this block is to ensure phase coherence of the two groups of paths driving each MMIC. The phase coherence must be guaranteed in the 100-MHz bandwidth around the central frequency (both for Ka-band and X-band case) being this value determined by ADC mounted on the ADC board [Fig. 1(b)]. The phase difference of the Ka-band MMIC input signals will result in lower signal-to-noise ratio (SNR) of the output signal. For the case at hand, the maximal phase difference dictated by the chip minimal SNR is equal to 15° over the entire bandwidth [6]. In order to achieve this goal, the routes of the transmission lines interconnecting each Ka-band antenna to the corresponding MMIC have been carefully designed and optimized in the limited unit-cell area.

IV. CHIP INTEGRATION

As discussed in Section II, two types of MMICs are used to receive the output of the X-band and Ka-band antennas. The functions of each chip are to amplify, combine, and downconvert the received X-band and Ka-band signals to the IF band (0–100 MHz) as requested by ADCs. Each X-band antenna
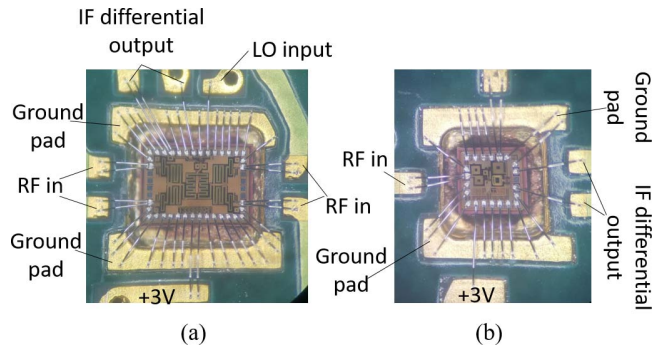
is connected to a single-channel MMIC which operates the downconversion using a 9.6-GHz LO signal generated off-chip and distributed across the board. The employment of a monolithically integrated power-combining stage is essential to reduce the density of the L1 layer.

Both MMICs receive single-ended RF and LO input signals matched at 50 Ω, whereas the output signal is differential and it is matched to 100 Ω in accordance with the input impedance required by ADC used in the ADC board (see Fig. 1). A detailed description of the chip used in this paper is available in [6].

One of the most critical aspects of the RF-board design is the integration of MMICs. Bare dies are used in order to reduce the integration area. It is worth noticing that the high number of input–output ports of the Ka-band chips does not allow the use of flip chip integration techniques as the density of the traces is not compliant with a standard PCB process. For this reason, it was necessary to employ a wire-bonding technique. Furthermore, in order to reduce the length of the bonds (i.e., their parasitic inductance), laser cavities were carved into the upper layers of the stack-up (from L1 to L3) to accommodate MMICs, as shown in Fig. 3. Considering the limited available space around the chips on layer L1 (see Fig. 5), the bond wire inductance has been compensated inside the chip in the input matching network for each LNA. Fig. 6 provides an image of the X-band and Ka-band MMICs integrated in the manufactured radar tile prototype. Chip ground pads are wire bonded to the two microstrip pads printed near the upper and lower borders of the cavity which is entirely metallized. Microstrip pads are soldered to the internal metallic walls of the cavity.

A. LO Distribution Networks

Two LO distribution networks are required to provide phase coherent inputs to the LO ports of the Ka-band and X-band chips. As shown in Fig. 2, the LO network of the single radar tile at the Ka-band is composed by one input and eight outputs while at the X-band, there are just two outputs. Looking at Fig. 5, it is clear that the density of the upper layer L1 does not allow the integration of these networks. Fig. 7 shows the two LO distribution networks. Input and output ports are located on the upper layer L1, while the rest of the network is accommodated in the intermediate layer L4. Connection

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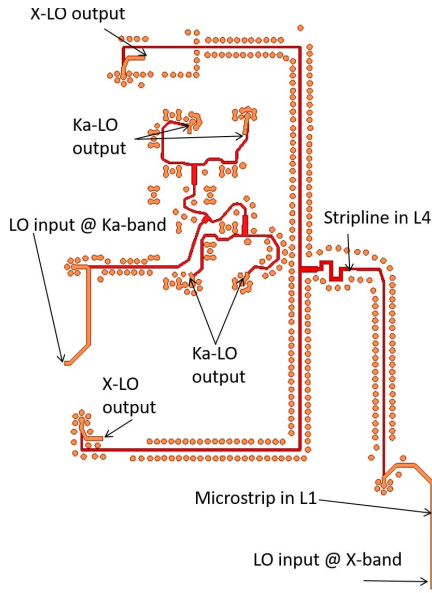
Fig. 7. LO distribution networks at the X-band and Ka-band integrated in the radar tile stack-up. Just layer L1 (in orange) and layer L4 (in red) are shown. The Ka-band LO network is mirrored to feed all the eight MMICs included in the single tile.

between the two layers is guaranteed by quasi-coaxial vertical transitions similar to the one presented in Section III-A. As shown in Fig. 7, several shielding vias have been placed around the stripline to avoid the excitation of unwanted modes in the parallel plate between L3 and L5 ground layers.

B. Power Distribution Network

A power distribution network has been integrated in the internal layer L6 of the radar tile to distribute low noise and stable power to MMICs. The maximum absorbed current by the Ka-band and X-band chips is equal to 40 and 20 mA, respectively. Therefore, the 10 MMICs present on each tile absorb 660 mW of dc power.

V. ANTENNAS' INTEGRATION

The basic principles underlying the Ka-band and X-band antenna design have been presented in [6] where they have been validated using a simplified seven-layer mock-up. In this paper, the antennas have been optimized to fit into the 15-layer stack-up shown in Fig. 3.

A. Ka-Band Antenna Integration

Ka-band antennas are dual-polarized stacked patches electromagnetically coupled to the feeding lines through slots (Fig. 8). The driven patch has been integrated in the layer L11 of the stack-up. A slot in ground layer L10 is used to couple the patch with the feeding stripline printed in L9. Connection between microstrips in the top L1 layer and feeding strips in L9 is obtained using the quasi-coaxial vertical transitions described in Section III-A. Two orthogonal parasitic dipoles and a patch have been added in layers L12, L14, and L15 to improve the radiation patterns and gains.
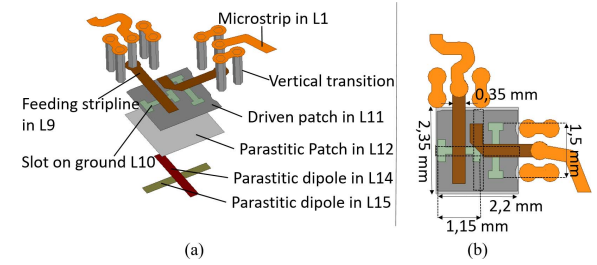

Fig. 8. Single Ka-band antenna integrated in the 15-layer stack-up. (a) 3-D view. (b) Top view (from layers L1 to L15).
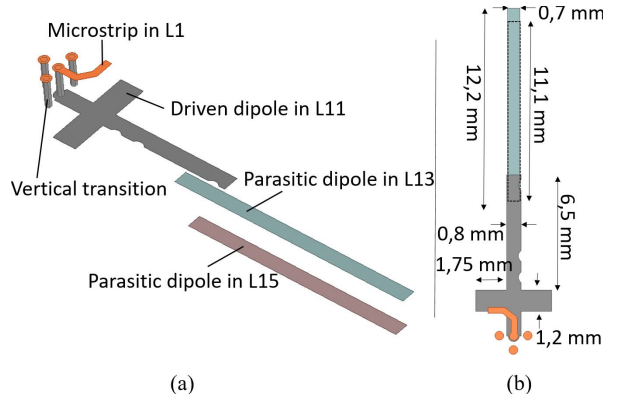

Fig. 9. Single X-band antenna integrated in the 15-layer stack-up. (a) 3-D view. (b) Top view (from layers L1 to L15).

B. X-Band Antenna Integration

The X-band antenna is realized with a pair of cross-dipole antennas printed on layers L13 and L15 (Fig. 9) proximately coupled to a driven dipole printed on L11. In order to reduce the number of layers in the proposed stack-up, the Ka-band driven patch and the X-band feed are arranged on the same layer (L11). A quasi-coaxial vertical transition is used to connect the antenna to the microstrips in L1. As for the Ka-band case, parasitic elements are used to enhance the gain and the bandwidth of the antenna. As shown in Fig. 3, 2 mm of foam are used as a spacer between the dipole in L13 and the dipole in L15. Small cuts have been added on the driven dipole to maintain an appropriate distance between the dipole and vias placed near the antenna.

C. Antenna Array Integration

A partial view of the tile layout is shown in Fig. 10, where two X-band antennas and eight Ka-band elements are shown. Fig. 10 shows (in red) the Ka-band LO distribution network integrated in the intermediate layer L4 (see Section IV-A). In order to validate the manufacturing process of the tile, the remaining Ka-band antenna elements were not bonded to MMICs but were fed by four-connector SMD connectors (Figs. 11 and 13) to allow a direct measurement of the antenna parameters. Furthermore, the signal detected at the output of these antennas was also used as a reference during the chip measurements (see Section VII-B).

VI. STACK-UP MANUFACTURING PROCESS

The radar tile prototype has been fabricated (Fig. 13) using the 15-layer stack-up presented in Fig. 3. A complex manufacturing procedure with tailored solutions was used during the

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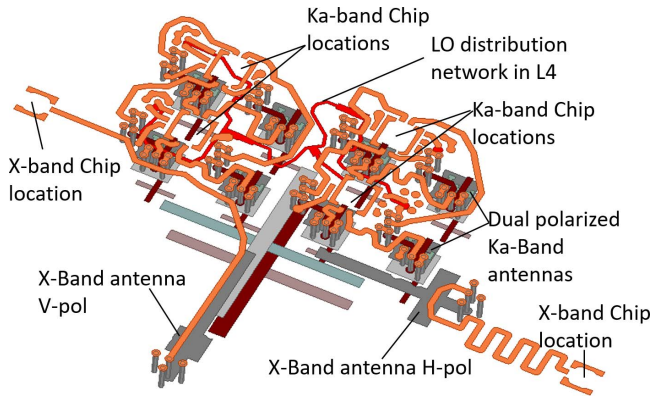IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES

Fig. 10. Integration of the antenna arrays in the 15-layer stack-up of a single tile. The tile accommodates four 2×2 arrays at the Ka-band and two antennas at the X-band (see architecture shown in Fig. 2).
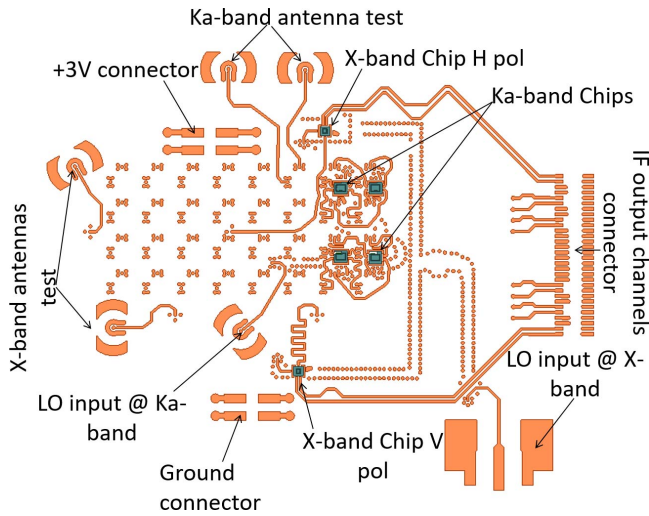

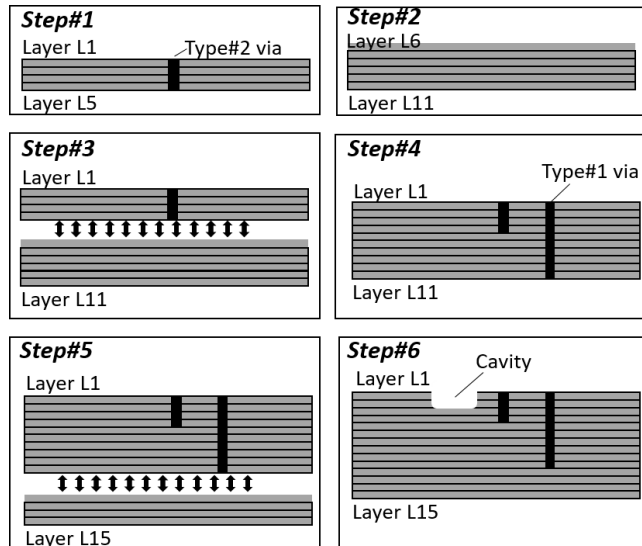Fig. 11. Final configuration of the board. (Just layer L1 is shown.)

Fig. 12. PCB stack-up manufacturing steps.

production steps. An innovative process that uses a dedicated fusion bonding technique has been employed. In this process, developed by Nuova Eurotar S.r.l, Italy, different core layers are glued together without using any prepreg.
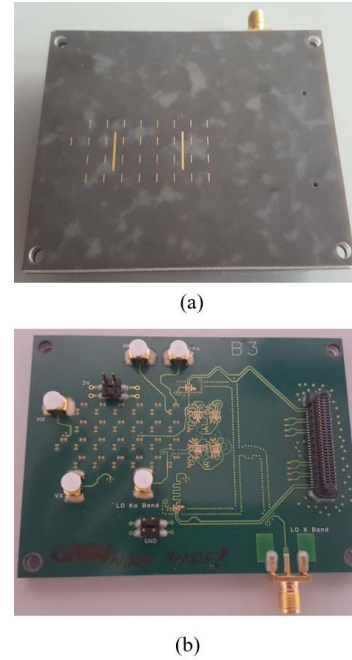

Fig. 13. Photograph of the manufactured board. (a) View from layer L15. (b) View from layer L1.

The fabrication process of the advanced multilayer PCB can be divided in six main steps as follows (Fig. 12).

- *Step#1:* Manufacturing of the subboard composed by layers from L1 to L5. (Type#2 vias are fabricated in this step.)
- *Step#2:* Manufacturing of the subboard composed by layers from L6 to L11.
- *Step#3:* The two subboards are bonded together under high temperature and pressure to produce an 11-layer assembly.
- *Step#4:* Type#1 vias are fabricated, and backdrilling is performed where necessary.
- *Step#5:* Layers from L12 to L15 are added.
- *Step#6:* Laser drilling and metallization of the cavities used to accommodate MMICs are performed.

Step#3 is the most critical one, because high pressure and temperature used to bond together the two boards can damage the vias fabricated in step#1; this might be caused by the deformation of the laminate used between L1 and L5. Fig. 14 shows an X-ray image of a via damaged after the competition of step#3. Arrows show some breaking point where the via has lost the electrical connection with inner ground layers L2, L3, and L5. This problem was solved reinforcing the vias fabricated in step#1 by the following measures.

- After the metallization, the inner part of the vias was filled with a special reinforcing.
- Maximum diameter of the vias was reduced to 0.2 mm.
- Circular pads were added at the top (layer L1) and bottom (layer L5) of each via.
- Rogers 2929 (instead of Ro5870) was used between layers 5 and 6; this dielectric allows using a lower pressure/temperature to bond together the two boards in step#3.

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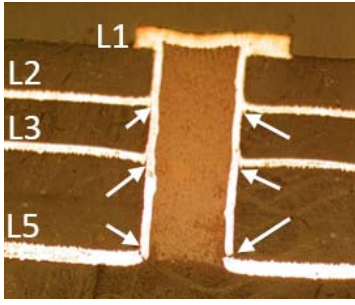ARNIERI *et al.*: INTEGRATED RADAR TILE FOR DBF X-/Ka-BAND SAR INSTRUMENTS

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Fig. 14.   X-ray image of type#2 via damaged after the production step#3.

Fig. 13 shows the top and bottom views of the successfully manufactured board.

VII. Experimental Validation

The objective of the experimental validation of the board was twofold. First, it was necessary to assess the manufacturing process. Second, measurements on the entire receiving chain were operated to verify the coherence of the experimental data with the design employing, for the first time, a fully integrated subsystem. For this reason, two types of tests were planned within the same tile.

- A subset of the tile radiating elements was fed using SMD connectors to directly characterize the S-parameters and the radiation patterns.
- The entire downconversion chain including both antennas and MMICs (using the configuration shown in Fig. 10) was validated illuminating the board with horn antennas and measuring the IF signals of the six output channels.

In the following, two sets of measurements will be presented.

A. Direct Antenna Measurement

As outlined in the previous section, antennas integrated in the tile are not directly accessible because they are connected to the chips. For this reason, in order to characterize the antenna performances within the final stack-up, one Ka-band and two X-band antennas were employed as test vehicles and fed with SMD connectors. In particular, the Ka-band radiator was fed with two ports for the V-polarization and H-polarization placed on layer L1 while the V-polarized and H-polarized elements in the X-band were individually fed. Fig. 13 shows the assembled prototype board that was used for the measurements. Fig. 13(a) shows the antenna layer (L15 shown in Fig. 3), and Fig. 13(b) shows the layer with chips and connectors (L1 shown in Fig. 3).

Fig. 15(a) shows the measured S-parameters of the Ka-band antenna. Matching for both antenna ports (H-pol and V-pol) is shown. Coupling between the two polarization ports is lower than -23 dB over the whole bandwidth. Fig. 15(b) shows the normalized gain of the Ka-band antenna when only the horizontal polarization port is excited. A similar pattern is obtained in the case of the vertical port excitation. The measured peak gain is 6.8 dBi at 35.75 GHz.

Fig. 16(a) shows the measured S-parameters of the X-band antenna. Matching for both antennas (H-pol and V-pol)
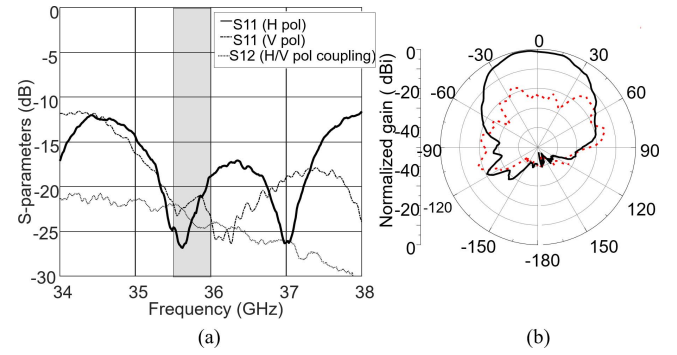

(a)

(b)

Fig. 15.   (a) Measured S-parameters of the Ka-band antenna. (b) Co-polar and cross-polar normalized radiation patterns of the vertically polarized Ka-band antenna at 35.75 GHz. Continuous line: co-pol. Dashed line: cross-pol.
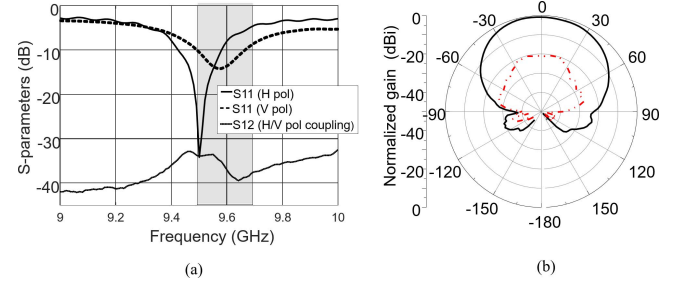

(a)

(b)

Fig. 16.   (a) Measured S-parameters of the X-band antennas. (b) Normalized co-polar and cross-polar radiation patterns of the X-band horizontally polarized antenna at 9.5 GHz. Continuous line: co-pol. Dashed line: cross-pol.

is shown. Coupling between the two polarizations is lower than -33 dB over the whole bandwidth. The reflection coefficient of the two polarizations is roughly acceptable as it is narrower than the expected bandwidth. This problem was caused by a minor manufacturing error. Indeed, a 1-mm foam layer between L13 and L14 (see Fig. 3) was used in instead of 2 mm. Measurement tests and simulations confirmed that this manufacturing error has a minor effect on the performance of the tile. In particular, the main effect is confined to the X-band antennas' matching. For this reason, and in the view of the high cost/time of manufacturing, it was decided that a new prototype was not necessary. Fig. 16(b) shows the normalized gain of the X-band horizontally polarized antenna at 9.5 GHz. A similar pattern is obtained for the vertically polarized radiator. The measured peak gain is 11.7 dBi.

B. Antenna and Chip Measurement Procedure

The results presented in the previous section demonstrate the correct behavior of the radiators integrated in the full PCB. In this section, the whole receiving chain composed by antennas, chips, and all other integrated components was tested.

Fig. 17 shows the measurement setup used to characterize the tile board. For each band, the tile has been excited by signals radiated by the X-band and Ka-band horn antennas placed in the far-field area.

As a first step, signal levels received by the X-band and Ka-band antenna test elements were measured. This measurement is necessary to evaluate the signal power present at the input of the X-band and Ka-band MMICs. In a second phase, the output IF signals of the X-band and Ka-band

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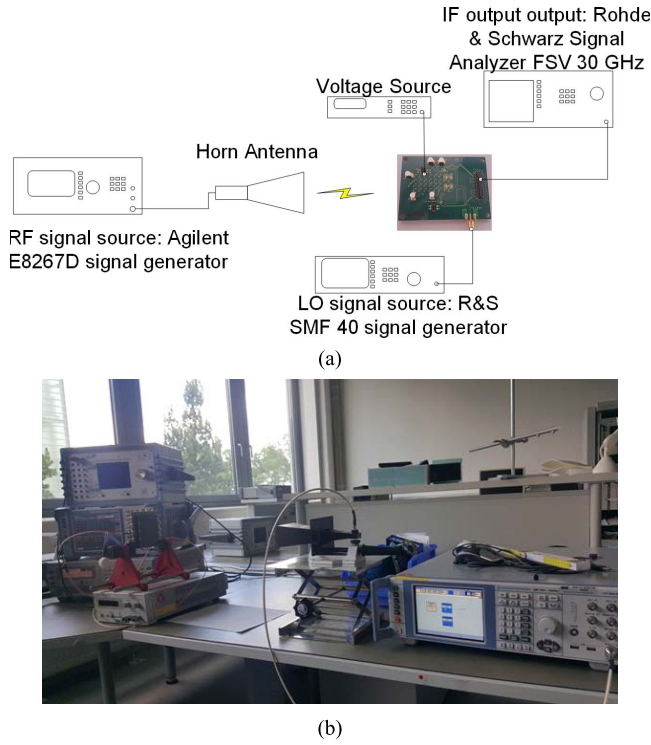IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES

Fig. 17. Measurement setup at the X-band. (a) Schematic view. (b) Photograph of the actual setup used.

chips are measured while the connectorized antenna elements are matched to 50Ω loads. These two steps, along with de-embedding techniques, are necessary to identify the conversion gains of MMICs. Moreover, the $P_{1 \text{ dB}}$ point and dc current consumption were also measured. Conversion gain has been measured versus LO frequency (by keeping constant RF), LO power, RF power, supply voltage, and RF (being the LO frequency kept constant).

The X-band measurements were done with 50-cm distance between the horn antenna and the board, while at the Ka-band, the illuminating horns were positioned 25 cm apart. The goal of the measurement is to verify that the X-band and Ka-band receiver chips have similar performance on the prototype board as for the on-wafer chip measurements presented in [6].

C. Measurement Results for the X-Band RECEIVER

The X-band measurements have been performed using the following equipment (Fig. 17).

- *RF Signal Source:* Agilent E8267D signal generator (up to 20 GHz).
- *LO Signal Source:* R&S SMF 40 signal generator (up to 43.5 GHz).
- *IF Output/Antenna Output:* Measured single ended with Rohde & Schwarz Signal Analyzer FSV 30 GHz.
- Eight channel voltage sources.
- X-band horn antenna (with coax input).

Fig. 18 shows the comparison of the measured conversion gain versus LO frequency for constant IF frequency of 100 MHz. Supply voltage for all measurements is 3 V while the expected current consumption for two X-band and four Ka-band MMICs is equal to 182 mA ($2 \times 25 + 4 \times 33 = 182$ mA).
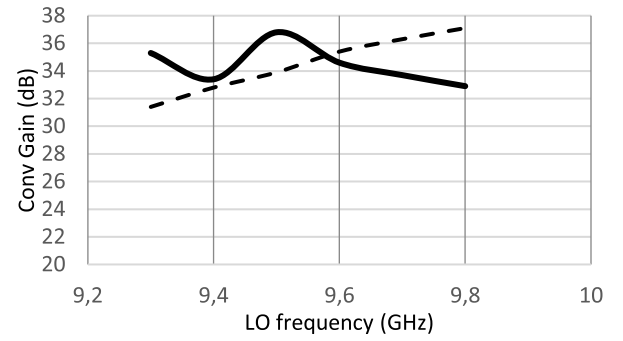

Fig. 18. Measured conversion gain of the X-band receiver versus LO frequency. Continuous line: current prototype. Dashed line: on-wafer measurement.
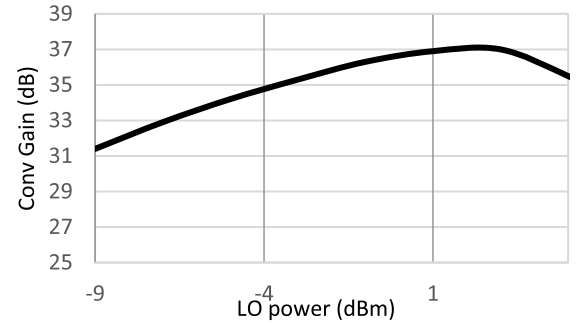

Fig. 19. Measured conversion gain of the X-band receiver versus LO power.
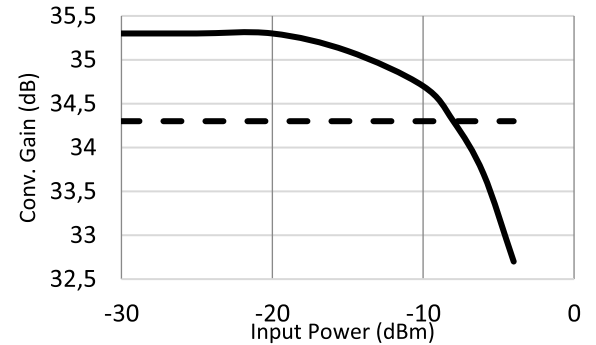

Fig. 20. Measured conversion gain of the X-band receiver versus RF input power. Continuous line: current prototype. Dashed line: maximum conversion gain −1 dB. The 1-dB conversion points for the prototype and on-wafer measurement are the same.

Conversion gain at 9.6 GHz is 34.6 dBm while 35.4 dBm were measured on-wafer. Fig. 19 shows the conversion gain versus the LO power from the generator. All the measurements were performed with an LO power of −3 dBm where the gain is 2 dB lower than the maximum gain. The power level at the board connector is −5.2 dBm. Fig. 20 shows the conversion gain versus RF signal generator power. $P_{1 \text{ dB}}$ at the output is −2.1-dBm single ended or 0.9-dBm differential. Fig. 21 shows the conversion gain versus supply voltage. As it can be observed, a gain variation of less than 1 dB is shown when the voltage is varied by 10%.

D. Measurement Results for the Ka-Band Receiver

Ka-band measurements have been performed using the following equipment (Fig. 22).

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ARNIERI *et al.*: INTEGRATED RADAR TILE FOR DBF X-/Ka-BAND SAR INSTRUMENTS
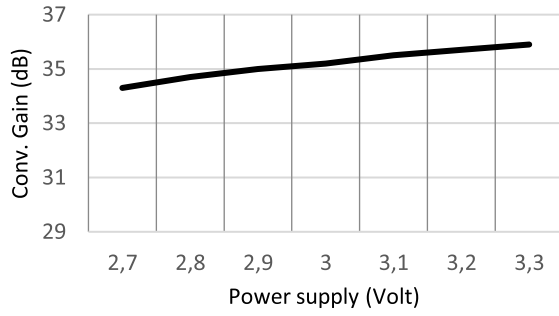
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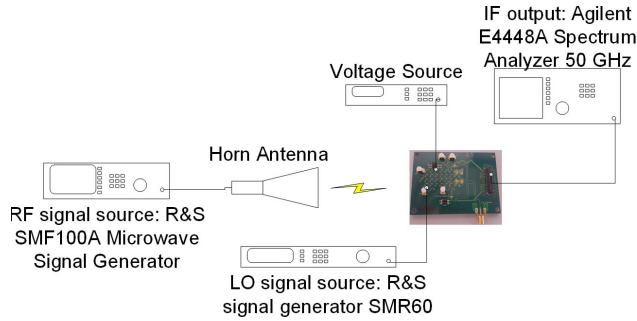Fig. 21. Measured conversion gain of the X-band receiver versus supply voltage.

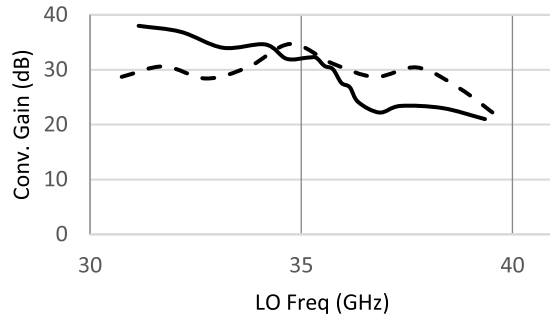Fig. 22. Measurement setup at the Ka-band.

Fig. 23. Measured conversion gain of the Ka-band receiver versus LO frequency. Continuous line: current prototype. Dashed line: on-wafer measurement.

- *RF Signal Source:* R&S signal generator SMR100A (up to 43.5 GHz).
- *LO Signal Source:* R&S signal generator SMR60 (up to 60 GHz).
- *IF Output/Antenna Output:* Single-ended measurement with Agilent E4448A Spectrum Analyzer 50 GHz.
- Eight channel voltage sources.
- The Ka-band horn antenna with waveguide input + coax to waveguide adapter.

Fig. 23 shows the comparison of the measured conversion gain versus LO frequency of the Ka-band receiver chips for constant IF frequency of 100 MHz. The bias voltage in all measurements is 3 V. Measured conversion gain at 35.75 GHz is 30.1 dB while 30.7 dB were measured on the on-wafer configuration [6].

Fig. 24 shows the conversion gain versus LO power. All the measurements were done with an LO power of 3 dBm, i.e., approximately 2 dB below the maximum gain. The power level measured at the board connector is −1.8 dBm. Fig. 25 shows
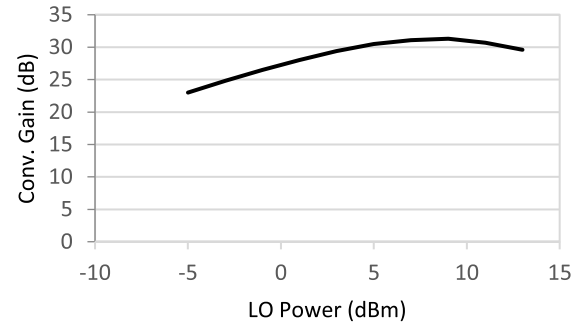

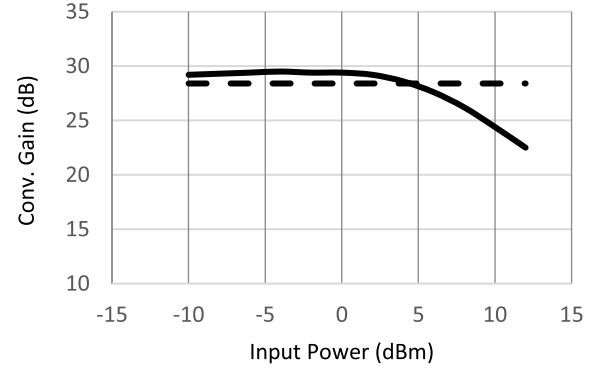Fig. 24. Measured conversion gain of the Ka-band receiver versus LO power.

Fig. 25. Measured conversion gain of the Ka-band receiver versus RF input power. Continuous line: current prototype. Dashed line: maximum conversion gain −1 dB. The 1-dB conversion points for the prototype and on-wafer measurement are the same.
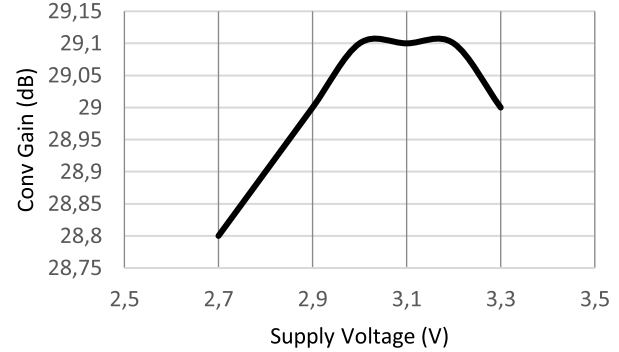

Fig. 26. Measured conversion gain of the Ka-band receiver versus supply voltage.

the conversion gain versus RF signal generator power. P_{1dB} at the output is −3.6-dBm single ended or −0.6-dBm differential. As for the X-band case, the conversion gain is highly stable with respect to the supply voltage variations (see Fig. 26).

E. Final Remarks

The experimental assessment of the integrated tile has shown that the X-band and Ka-band receiving chains behave as expected with a chip conversion chain substantially agreeing with the on-wafer measurements [6]. Limited differences are present, and they appear to be within the expected chip-to-chip variations. Measured S-parameters were extrapolated through a de-embedding procedure using the antenna ports as a reference. The agreement between measured and simulated values confirms the validity of the proposed integration process

and of the associated design. It was not possible to measure the noise figure of the whole Ka-band MMICs, but the data of the single LNA were evaluated in [6]. However, the on-chip power combining was characterized indirectly through the estimation of the conversion gain of MMIC which was in agreement with the single-channel value plus 12 dB.

VIII. CONCLUSION

In this paper, a first example of highly integrated dual-band dual-polarized SAR RF module was presented. The proposed radar tile integrates all the RF components, i.e., antennas and downconversion stages, required to compose the RF front end of a DBF SAR instrument. The architectural approach is fully modular, and it allows the scalability of the design as dictated by the mission specifications.

Although conceived for experimental purposes, the proposed demonstrator is conceived for a standard production process as it employs a standard high density interconnect (HDI) technology. Custom solutions have been devised and tested to adapt the HDI process to the complex stack-up necessary to implement the proposed tile. The main challenge was to design a low-cost SAR tile at the highest limit of complexity for the proposed technology. The experimental results demonstrate the validity of the overall approach and the good performance of the whole RF downconversion chain, from the antennas toward the IF output channels. Indeed, the results of the integrated tile are well matched with the behavior of the single blocks individually tested in [6]. A conversion gain of about 35 and 30 dB was demonstrated in the X-band and Ka-band, respectively. Thanks to its compactness, the proposed RF-board tile can be considered an example of a key building block enabling a new range of EO applications based on small satellite platforms.

ACKNOWLEDGMENT

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