TECHNOLOGY-DRIVEN DESIGN OF A SCALABLE SMALL SATELLITE PLATFORM

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ABSTRACT

This paper presents a new approach in satellite platform design. While traditionally the design of technology demonstration- or scientific missions is driven by the requirements of the payload, the focus of our approach lies on using avionics technologies developed by the German Aerospace Center (DLR) as the core components of the satellite bus. These components will then drive the design of the *Small Satellite Technology Platform*, in short S2TEP.

This methodology change towards a technology-driven approach results from the long-term goals identified for future in-house space missions, as there are a cost effective platform design, a shorter development time, short-term design adaptions and the ability to carry out own research and development activities which lead to a deeper design understanding. The accomplishment of these goals also requires a change within the satellite's model philosophy, a new development process and a flexible and highly autonomous ground segment.

The first instantiation of the S2TEP platform will be a satellite in the micro-satellite class. During this project the needed avionics technologies will be further developed up to a Technology Readiness Level (TRL) mature enough to be integrated in the flight model for the first mission. By separating mission- and bus-development it is ensured that the payload does not influence the bus design too much. Though, a reference mission will be designed to set an interface to and an envelope for possible payloads.

The DLR avionics technologies to be used for the S2TEP core avionics consist of the Onboard Computer (OBC), the Power Condition and Distribution Unit (PCDU) and the Transceiver-unit. All of these components are designed taking scalability into account - concentrating not only on performance parameters but also on quality aspects, like the migration path for all used electronic parts towards space qualification. Taking the OBC as an example, the scalability up to the next higher class of satellites will be presented within this paper.

1 INTRODUCTION

The German Aerospace Center (DLR) pursues the objective to develop a cost-effective satellite platform for technology in-orbit demonstration and for serving small scientific payloads. It is called *Small Satellite Technology Platform* – in short S2TEP – and is located within the class of micro satellites as shown in Table 1.

Category	**Launch mass [kg]**
Picosatellite	<1
Nanosatellite	1 – 10
Microsatellite	**10 – 100**
Small satellites	100 – 500
Medium satellites	500 – 1000
Large satellites	1000 – 5000
Extra-large sat.	>5000

Table 1: General Satellite Classification

The satellite design mainly focuses on the usage of DLR's own technologies, which is the reason why we call this approach *technology driven*. Emphasizing on in-house developed technologies shall accomplish the following long-term goals:

- shorten the development time for each S2TEP-based satellite
- allow short-term design adaptions
- allow own research and development activities
- allow design understanding

The micro satellite platform S2TEP has a close connection to DLR’s already existing small satellite program *CompactSat* and its first mission Eu:CROPIS which is scheduled to be launched by the middle of 2017 (see e.g. [Hauslage2014] for further details). This connection is mainly driven by the fact, that the CompactSat platform will make use of the maturation of system components onboard S2TEP: the in-house developed core avionics are scalable in both performance and component quality to satisfy the requirements from the cost-effective microsatellite S2TEP up to the high reliable small satellite CompactSat. New developed components are firstly utilized on S2TEP to gather in-orbit experiences, before a scaled-up version of the component is used for CompactSat.

Taking the compact onboard computer (COBC) (see [Treudler2014]) as an example, after demonstrating its suitability in space onboard the Eu:CROPIS mission as one of the secondary payloads, the COBC will be adapted and used as the onboard computer of the first S2TEP mission. Having heritage from these two DLR missions, the COBC is hereafter a mature system component and is most likely to be used as the onboard computer for the next CompactSat mission as well as for future S2TEP missions (see Figure 1).

In addition, also the S2TEP-platform as a whole has some kind of heritage, as its design benefits from the experiences gathered during the development of the AISat mission (based on the microsatellite bus CLAVIS; see [Sproewitz2010]) , as well as the development of the MASCOT asteroid lander (see [Grundmann2015]).

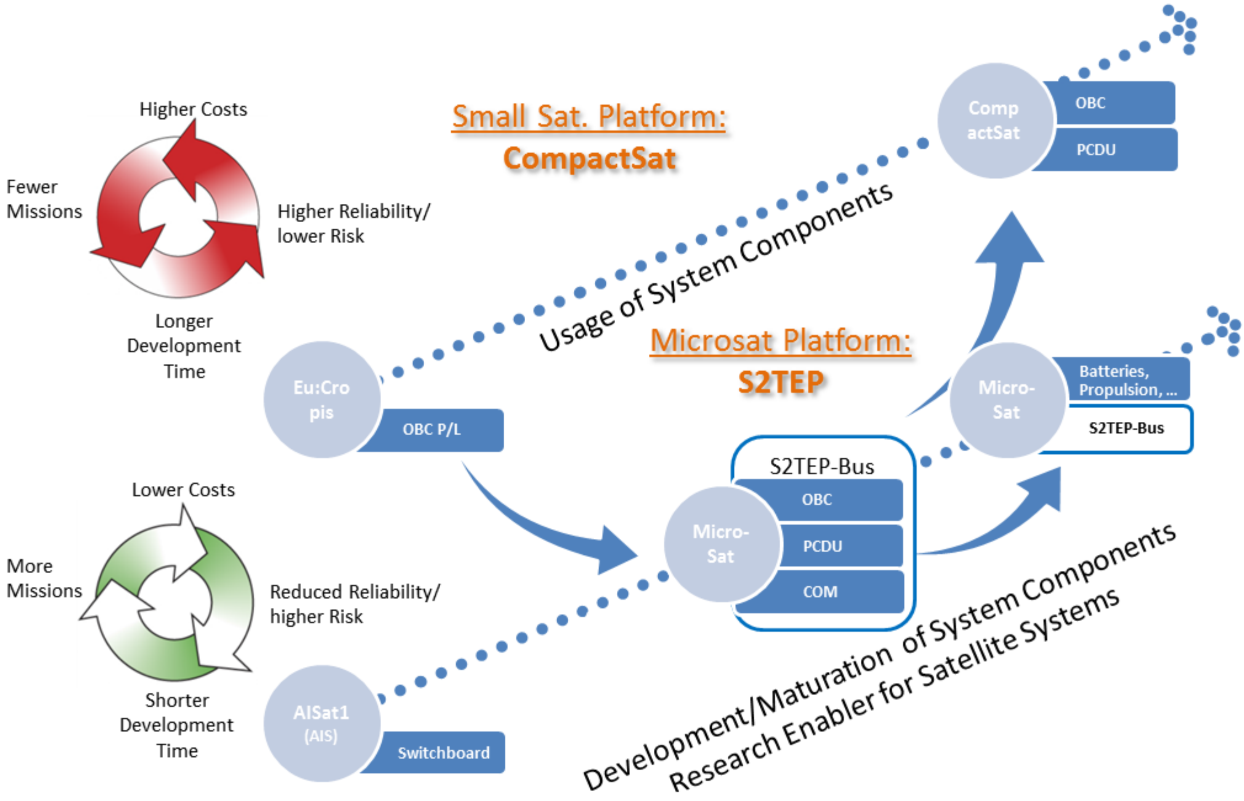

Figure 1: S2TEP Roadmap and Technology Transfer

2 DEVELOPMENT PHASES

The development of the S2TEP platform is based on the classical aerospace project approach, tailored from the ECSS recommendations. It mainly defers in the mission and system definition phases, due to the fact that bus design is not derived from a single mission. It is rather driven by the capabilities of the DLR in-house developed subsystems together with a mission envelope, formed by 10 potential payloads. The subsystem capability analysis and the mission envelope, together with the financial and programmatic constraints provide a reference mission which drives the design. Figure 2 summarizes the design driver for the S2TEP platform.

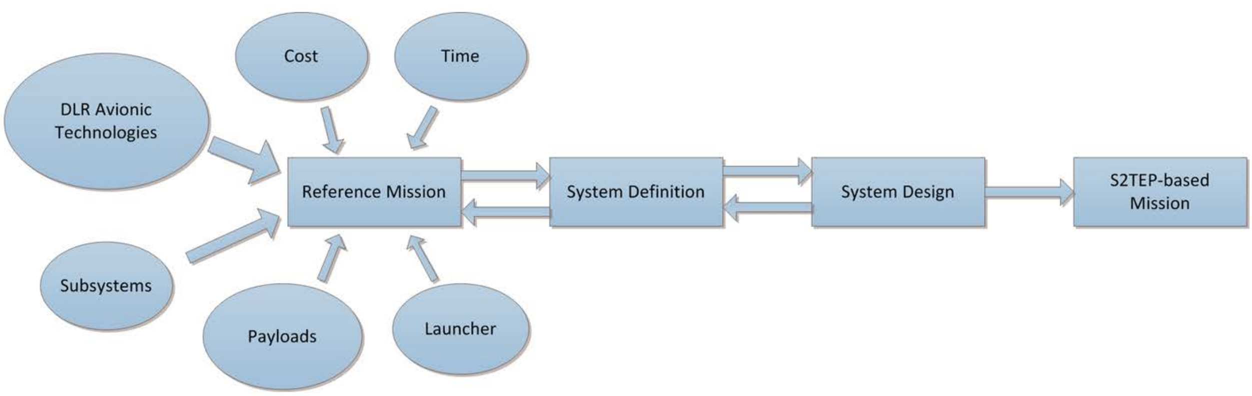

Figure 2: S2TEP Design driver

This approach shall satisfy the intended multi-mission compatibility where the focus is not on the optimal design for a specific mission but for the optimum of a series of satellites with different missions.

The platform development has been started with the Reference Mission Definition phase, where the mission envelope, programmatic constraints and the in-house technology development have been surveyed. The findings resulted in a set of development goals, constraints, general requirements and recommendations as basis for the requirements engineering and concept development during the subsequent Requirements and Concept Study.

During the feasibility study the findings from the reference mission definitions are iterated, the system requirements are derived and basic system concepts are developed. After the feasibility of the reference mission will be proven, the payloads for the first mission will be selected from a pool of candidates. In distinction from the general satellite development strategy the selected payloads have to be adapted by the payload supplier to satisfy the capabilities of the S2TEP payload interface standard. This is the expense on payload side for fast bus development and overall design cost reduction.

After this phase the development follows in general the classical design approach. During the Preliminary Design phase the concepts will be elaborated, so that with the start of the Final Design phase the assembly integration and verification of the structural and engineering model can be started. During that phase the design is reviewed a last time. The FM Integration, Qualification and Delivery phase finally focuses on the manufacturing and qualification of the flight model. The list of documents to be generated was reduced as well as the number of reviews in order to optimize development time. Each S2TEP project phase is completed by a review which is prepared in a dedicated workshop.
Figure 3 summarizes the development process for the first mission.

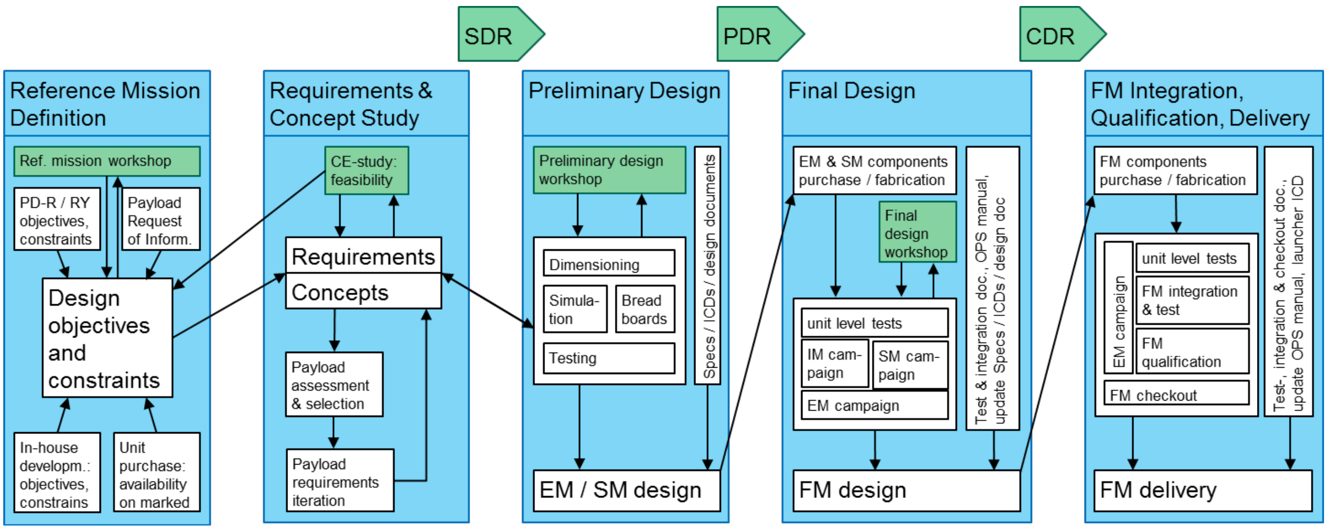

Figure 3 S2TEP development phases

For future missions the development deviates in the long term from the process pointed out above. The Reference Mission Definition will be replaced by a payload application and assessment phase. After payloads candidates are identified the bus configuration and required payload adaptions are determined in a concurrent engineering study, and elaborated in a shortened Preliminary Design Phase. The reviews are reduced to a delta PDR and a delta CDR.

The development will be supported and partly automated by model based systems engineering tools, which are developed during the first mission.

3 INTEGRATED TECHNOLOGY ROADMAP

The current status and further planning of DLR's own avionics technologies to be integrated in the S2TEP satellite bus is reflected within the S2TEP *Integrated Technology Roadmap* (ITR).

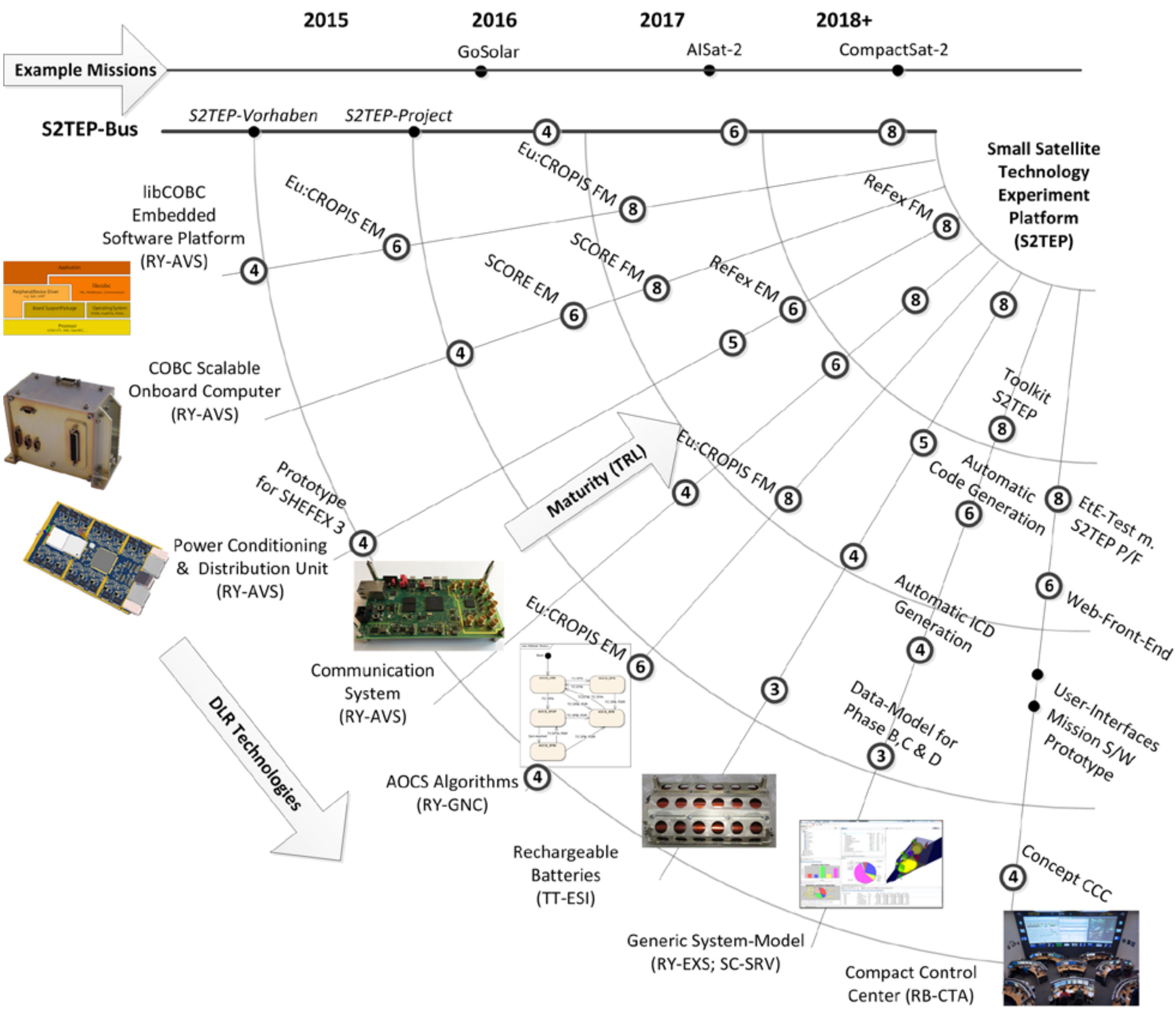

Figure 4: S2TEP Integrated Technology Roadmap

Using this kind of roadmap in order to define the technology development logic and combine it with the corresponding TRL maturation as well as the use cases within missions is a technique used in space industry as well (cf. to [Wolf2014]). Within the S2TEP ITR, DLR’s avionic technologies are mapped to their TRL and to their related projects in which these technologies will be further developed: as for some of them the main development activities will take place during S2TEP platform development, others have strong dependencies upon other DLR space projects. For the latter technologies, only adaptions to the S2TEP platform are foreseen. In detail, the core avionic technologies to be integrated over time are:

- the compact onboard computer (COBC)
- the corresponding software platform libCOBC (see [Dannemann2014])
- the power distribution and conditioning unit (PCDU)
- the communication system based on software defined radio (SDR)
- the algorithms for the attitude determination and control system (AOCS)
- rechargeable batteries

In addition, a generic system model and the remotely-usable und highly autonomous ground station Compact Control Center (CCC) will support the design process as well as the operational scenario. The key point of all these technologies lies within the fact that all of them are scalable and adaptable on component level, thus enabling the scalability and adaptability of the whole S2TEP platform.

4 SYSTEM DEVELOPMENT APPROACH

Taking the high frequency of S2TEP-based satellites to be build (see Section 1), the development phases (see Section 2) and the platform design drivers into account (see Section 3), also the overall system development process for the current and future S2TEP missions is longing for a new approach. It is displayed in Figure 5 and strongly oriented on the development approach created for the InnoSat platform (cf. to [Larsson2014]), as well the top-down product-driven design process as presented in [Alizon2007].

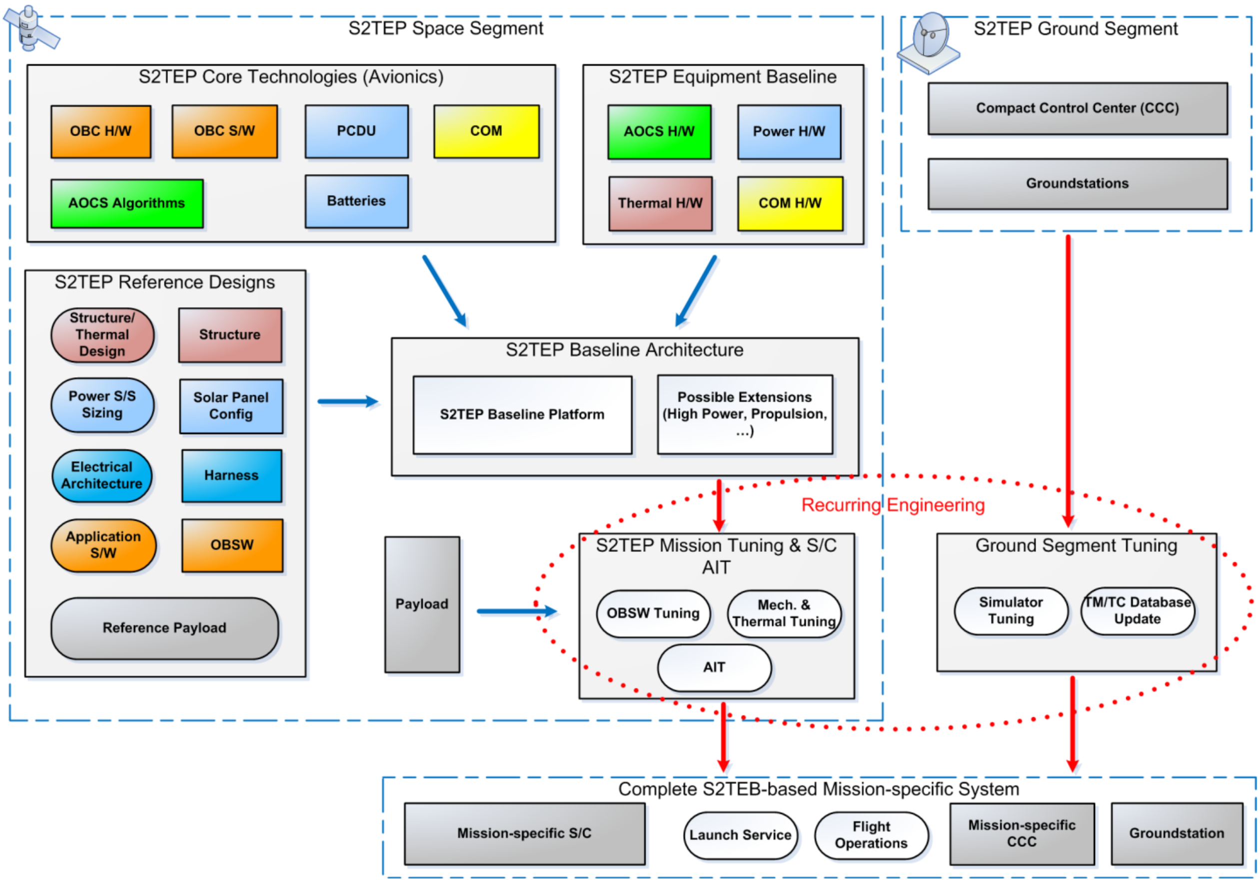

Figure 5: S2TEP System Development Approach

In its center, there is the S2TEP baseline architecture which is driven by the core technologies to be used, the additional baseline equipment and a set of reference designs. As explained in Section 3, the most important design drivers are the core technologies and the reference payload. The core technologies are managed within the S2TEP ITR also explained in Section 3. Starting from this baseline architecture, the mission tuning can then take place using a concrete payload. Together with the corresponding ground segment tuning we are hereafter able to develop a complete S2TEP-based mission scenario.

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