Design of a highly integrated and reliable SDR platform for multiple RF applications on spacecrafts

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***Abstract*— The utilization of Software-Defined Radios (SDR) has already become state-of-the-art for terrestrial Radio Frequency (RF) and wireless applications. The almost conservative space industry also identified the benefits of reconfigurable radio systems and uses SDRs on satellites and space vehicles. The traditional definition of a software-defined radio thereby is the digital implementation of applications in Field Programmable Gate Arrays (FPGA) or Digital Signal Processors (DSP). The analog parts (e.g. RF components) of the radio are generally tailored to the application specification and are not, or only partly, configurable. With the release of programmable and reconfigurable Radio Frequency Integrated Circuits (RFIC), a new era of SDRs was declared, which allows more flexibility and higher performance into smaller dimension. Thus, making these benefits available for applications on spacecraft has been identified as a big challenge, since those technologies are not designed for the harsh environmental conditions in space. This paper presents an approach for a highly integrated and reliable Generic Software Defined-Radio (GSDR) platform design and the results of a pre-evaluation test under radiation conditions on a prototype, to investigate certain mitigation techniques and a preconceived selection of system components. Focus of this platform is the integration into a satellite system, in order to operate multiple RF and wireless communication applications, where typically specific units for each application are used.**

Keywords—Satellite communication, Software-Defined Radio (SDR), fault-tolerant design, radiation-tolerant approach

I. INTRODUCTION

Software-Defined Radios (SDRs) are becoming an important factor in Radio Frequency (RF) and wireless communication technologies, in order to increase flexibility, data throughput and scientific output. Many satellite communication systems, providing high throughput data links in Geostationary Earth Orbit (GEO) or scientifically satellites in low earth orbit, use flexible radio systems, in which baseband algorithms are implemented in Field Programmable Gate Arrays (FPGA) or Digital Signal Processors (DSP). The main advantage of this kind of radio is the potential to update the baseband processing algorithms (or applications) and to improve the performances while the satellite or spacecraft is already in space. Another major benefit of SDRs is the reduction of cost and size, since most data processing can be handled in a single chip. Even if these kinds of SDRs have a modular architecture, those systems are commonly designed for one particular service. This is caused by the specific requirements of each application, which are mainly related to the RF properties (down-/up conversion, RF bandwidth and signal strength) and the analog-digital conversion and vice versa. To fulfil those requirements, plenty components are needed to be selected for each application and for this reason, a multiple application platform for a wide frequency range is hard to design, with respect to small dimensions. The Institute of Space Systems of the German Aerospace Center (DLR) is working on this topic and has developed a first prototype for a Generic SDR (GSDR) platform with multi-band operation purposes on spacecraft. Goal of this SDR approach is to provide a reconfigurable and small platform, suitable also for low- and mid-class spacecraft missions.

An important driver for SDR-based applications on satellite- and spacecraft missions is the reliability aspect, which strongly depends on the type of operated service. For example, a telecommunication broadcast service or a rescue application has a high priority in accessibility and reliability (high-class), while a failure or malfunction of an experimental and scientifically payload is often arguable (low/mid-class). Thus, the design of a SDR payload may vary extremely in cost, size, power budgets and performance. Most of the systems with a high claim of accessibility and reliability are based on expensive Radiation Hardened (RadHard) components and redundancies, whereby experimental payloads are often designed on a full Commercial Off-The-Shelf (COTS) approach and a non-redundant architecture. With respect to achieve smaller dimensions, lower costs, short lead-times and high performances, a COTS-based design seems more promising for a highly integrated GSDR platform. Moreover, important system relevant components for this platform approach are currently not available space qualified. To fulfil also higher demands on reliability purposes, specific solutions have to be found, e.g. by evaluating radiation hardening strategies in hardware design and software. In this paper, we propose the design and architecture for a highly integrated and reliable multi-band SDR platform on a spacecraft. A detailed

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design description is presented and a novel hybrid architecture is described, combining selected, well-known, COTS components, RadHard solutions and implemented mitigation techniques to detect and handle Single Event Effects (SEE) and being immune to Total Ionizing Dose (TID). Part of this process is a pre-evaluation test on a first prototype of the GSDR system and selected COTS candidates for further re-designs.

A motivation of the GSDR platform development is given in section II. Section III presents the GSDR prototype pre-evaluation results, including the analysis of the signal constraints and radiation impacts. A radiation hardening architecture approach (hardware and software) is briefly presented in section IV and V. The conclusion of this paper will be summarized in section VI.

II. Background and Motivation

As already introduced in chapter I, the main intention of this R&D activities is to provide a highly integrated platform, which can perform different communication-related applications on a spacecraft, without a complete re-design by each mission and service. Applications, for example, are the telecommand- and telemetry unit of a spacecraft, which are usually defined as dedicated communication subsystem, or any kind of communication payload, e.g. the processing of transmitted signals by Aircrafts or Vessels [1]. With the release of highly integrated RF transceivers, the traditional definition of a SDR has been changed and multi-band operation on single platforms becomes practical. Thus, by multiplexing and scheduling, applications in different frequency bands can be operated in a single device, where usually multiple units were required. Making such advantages available for space would have a massive impact in payload- and subsystem design, with respect to configuration, flexibility, mechanical dimensions and mass properties. Major challenge for this transaction is to protect the system and their sensitive components against the harsh environmental conditions in space, since targeted and required technologies are mostly designed and available for the terrestrial ambience.

A. *Baseline design*

To allow fast integration and adaption, the GSDR system is configured as a mother- and daughterboard design. The RF daughterboard contains application specific RF circuits and components (e.g. filters, mixer and amplifiers) to maximize the performance, while the architecture of the GSDR motherboard is unchanged. Thus, the re-design and tailoring to other applications and services is limited to the RF daughterboard and results into low design costs and low complexity levels. The GSDR motherboard architecture is based on a System-on-Chip (SoC) signal processing module and a highly integrated RF transceiver unit, which allows the operation in a frequency range between 70MHz and 6GHz, without using additional RF equipment (e.g. up-converter). Volatile and non-volatile memories are used to provide computing resources to the SoC and data storage capacities for system- and payload data. Different interfaces (analog, digital and RF) are implemented in the design. A supervisor circuit observes the functionality of the system and monitors sensitive units to prevent data corruption and destructive damages of the appropriated device. The interconnection between the GSDR motherboard and the RF daughterboard is performed on differential data-lines and are transformed to single-ended on the RF daughterboard to minimize the interferences to the data. External data interfaces implemented on the GSDR system, which are commonly used for space applications, are Space-Wire (SpW) for high-speed data transfer and a Universal Asynchronous Receiver Transmitter (UART) serial interface, for command and control. Additional debug interfaces, which are not common for space application (e.g. Ethernet, USB etc.) are provided as well and can be enabled by user.

B. *Baseband Processing System*

The Baseband Processing System (BPS) is based on a Xilinx-7000 SoC device. The SoC is separated into a Processing System (PS), including an application processing unit, interconnects and memory interfaces, as well as a Programmable Logic (PL) based on a 28nm process, comparable to a Xilinx Aritx-7 FPGA fabric. The PS comes with a dual-core ARM A9 cortex, operating at a frequency of up to 866MHz. Advantage of such SoC technologies is that very fast, multiple and complex signal processing can be performed in the high-efficient FPGA fabric, while the data post-processing and interfacing to other system parts can be handled by the PS. Connected to the SoC is an assorted memory architecture with volatile- and non-volatile memory options. Due to the 64-bit AXI-Interface, it is possible to push and capture data between the DDR Memory (DDRM), connected to the PS, and the RF transceiver unit, which is interfaced to the PL.

C. *RF Transceiver Unit*

The RF transceiver unit combines the RF signal processing, converting, and digitization (and vice-versa) in one single device. The selected AD9361 agile transceiver (Analog Devices) uses two independent transmitter and receiver chains, whereby each receiver chain has three RF inputs and the transmitter chains contain two separated outputs. An overview of the AD9361 agile transceiver system is shown in Fig. 1.

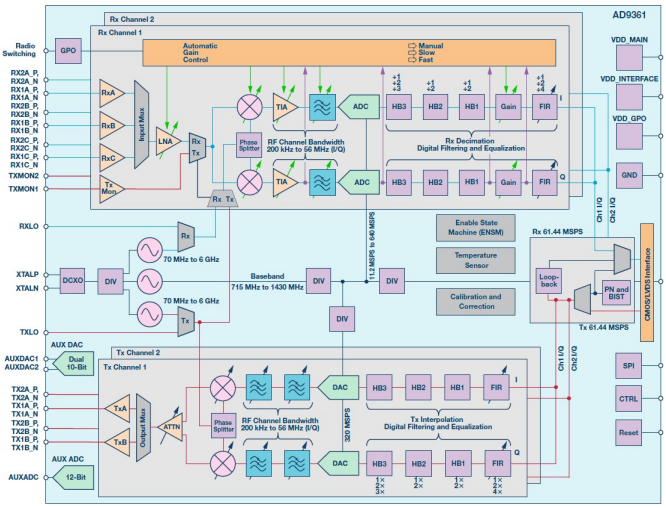

Fig. 1. AD9361 overview in block design

Those in- and outputs are multiplexed and can be used to attach different, application specific, RF circuit for performance-enhancement. Due to the 2x2 transceiver chain constellation, Multiple Input Multiple Output (MIMO) services are also applicable.

The AD9361 RFIC is based on a 65nm CMOS process, which makes the device sensitive to SEE, in particular to Single Event Upsets (SEU). These conditions have been identified as one of the most critical issues in the system design, since all configurations of the RFIC are register-based.

III. Pre-evaluation on a GSDR Prototype

To identify critical issues on non-negligible system components and to analyze signal constraints on the analog, digital and RF side, a first (all-COTS) prototype has been developed. A picture of this prototype at a Total Ionizing Dose (TID) test is given in Fig. 2 and selected results, in particular the AD9361 performance under ionizing dose effects, are presented in the following section.

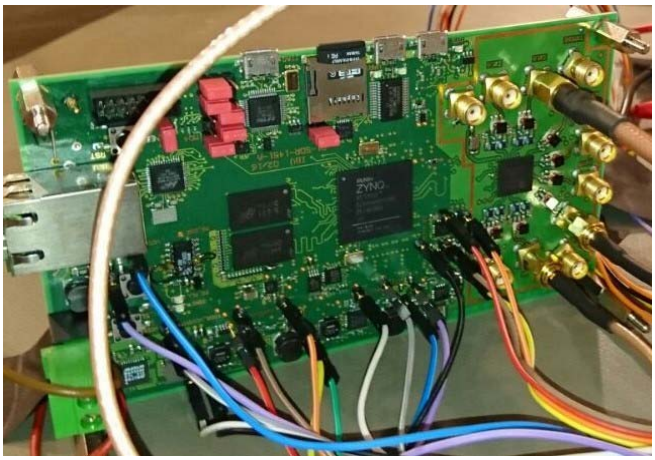

Fig. 2. GSDR Prototype board at TID test

The results of these pre-evaluation tests will have a massive influence on further development steps in order to radiation hardening and fault-tolerant enhancement of the GSDR system.

A. *Analyzed signal constraint*

To give an example about the importance of pre-analysis of the signal constraints, Fig. 3 shows the current on the Double Data Rate Synchronous Dynamic Random Access Memory (DDR RAM) at 1.5V DC for an AIS receiver application [2].

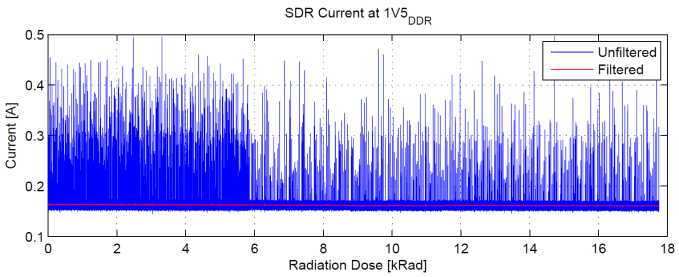

Fig. 3. Dynamic signal constraints for current at DDR3 1.5V DC

The current levels are highly dynamic and it was observed that these conditions strictly depend on the conducted application. These signal constraints are important to design latch-up protections and determine correct current-limit thresholds. Dynamic current conditions are also observed on the SD-Card and the non-volatile memory attached to the BPS due to read- and write operations. Static current values (e.g. RFIC, BPS) also depend on the conducted application.

B. *Impact of TID effects*

TID degradation effects of devices are caused by charged particles and gamma rays that create critical ionization. To evaluate the system behavior under ionizing conditions, selected parameters, like voltage regulator outputs, applied current levels and RF-Transceiver performances were monitored. Fig. 4 shows the output voltage and applied current of the 5V DC main input voltage regulator.

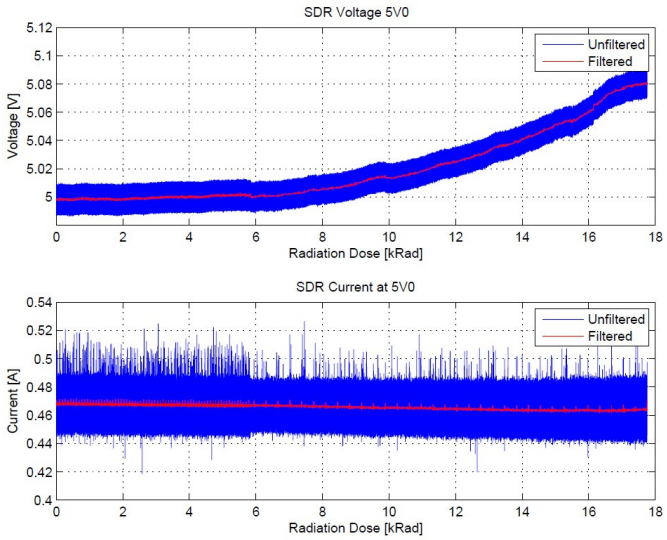

Fig. 4. Characteristic of the GSDR prototype 5V DC voltage regulator during TID test

After a dose of 8kRad, the regulator output voltage starts to increase continuously until the voltage level reaches the maximum allowed input voltage the following powered devices. At this point, and a dose of 17.5kRad, the test was aborted to protect the system of permanent damages. This radiation behavior was observed at different other regulators in the system and has been categorized as medium-critical for the further development. In addition, selected devices (e.g. multi-channel voltage regulator) for the further GSDR system design have been tested, that shows robustness to TID effects up to a dose of 45kRad. Deviations of other system components (e.g. Oscillators) specifications and functionalities during the TID test were not overserved. In particular the RFIC has shown strength robustness against the irradiated ionizing dose. On a second test-board, the RFIC parameters were evaluated against TID at room temperature (21°C). Therefore, only the RFIC has been irradiated and other system components have been shielded. For the receiver's evaluation, a 1MHz sine-wave of 0dBm was transmitted at a carrier frequency of 900MHz, 2.4GHz and 5.5GHz to test the complete supported frequency

range of the RFIC. The receiver's adjustable gain control over TID is shown in Fig. 5.

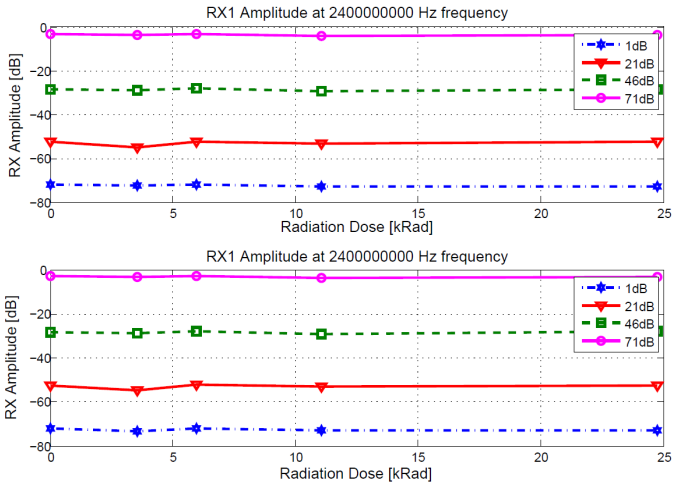

Fig. 5. RFIC adjustable gain control for 1dB, 21dB, 46dB and 71dB gain at a carrier frequency of 2.4GHz of Rx1 and Rx2

No significant gain-deviation on both receiver chains (RX1, RX2) was observed until a final dose of 25kRad was achieved. Other receiver-related specifications like noise figure, Automatic Gain Control (AGC) performance or scattering parameter were also evaluated without any remarkable degradation effects. A test with modulated signals, to analyze the demodulation accuracy or receiver sensitivity was not performed during this test. For a carrier frequency of 800MHz and 5.5GHz no appreciable results are given, since no significant deviations were noted.

For the transmitter's evaluation, similar test conditions were determined, which include the test of maximum output power stability at a 1MHz tone with a carrier frequency of 800MHz, 2.4GHz and 5GHz, the power control (adjustable attenuation) functionality and the transmitter's intermodulation distortions. In Fig. 6, the maximum output power of both transmitters including cable-losses of ~10dB is presented. The output power varies between -2.5dBm and -3.1dBm, which is not assumed to be an effect of irradiation since a variation, caused by TID, will follows a uniform direction.

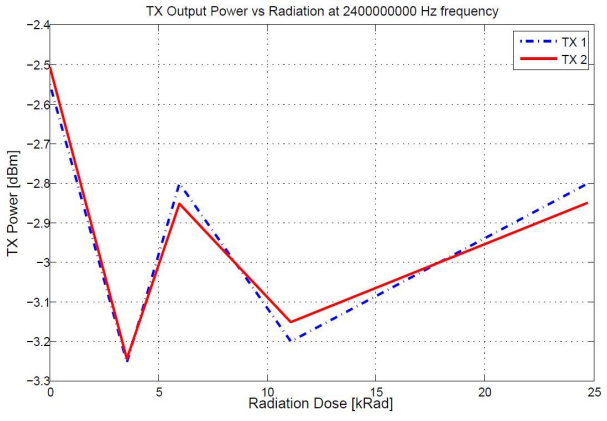

Fig. 6. RFIC maximum output power vs. TID of a 1MHz sine-wave at 2.4 GHz carrier frequency.

In Fig. 7 the results of a TX intermodulation test for different attenuation vs. TID is presented. The plots show the TX amplitude of the fundamental tones (1MHz and 2MHz), as well as magnitudes of the 3rd and 5th order for three different attenuation levels (-1dB, -11dB and -21dB).

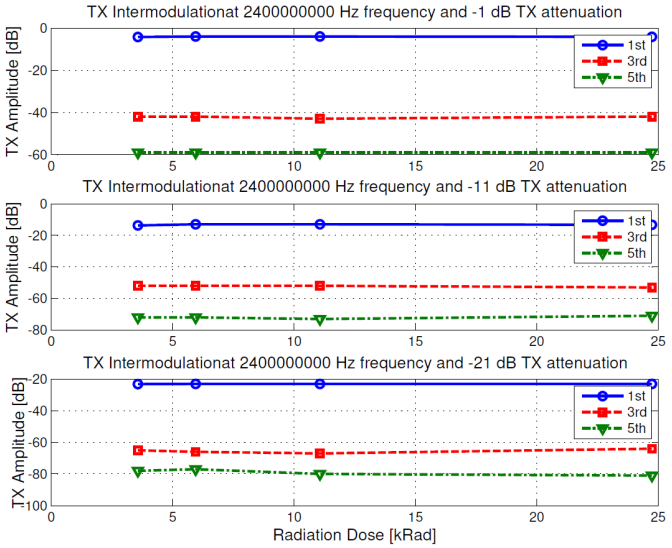

Fig. 7. RFIC TX intermodulation vs. TID for a 1MHz and 2MHz fundamental tone at 1dB, 11dB and 21dB attenuation and a carrier frequncy of 2.4 GHz.

The results show that the intermodulation distortion does not change with increasing TID levels, which proves that the TX amplifier linearity does not change during irradiation. In addition, attenuation levels are also not affected by TID.

Interfaces- and general functionality (configurations) tests of the AD9361 were also performed without any restriction.

IV. Radiation Hardening Hardware Architecture

Based on the pre-evaluation of the GSDR prototype, different changes in the design- and component selections are required, in order to ensure a reliable and full-functional system in space. Talking about reliability for space application is often associated with high costs, long lead times and large components-sizes, resulting from the utilization of RadHard devices. Moreover, due to the fact that the selected highly integrated RFIC is not available space qualified, a detailed investigation on system hardening strategies for radiation effects is mandatory. Therefore, it is essential to understand which part of the system may be sensitive to radiation environments and needs to be protected. The selection of COTS- or RadHard devices strictly depends on the availability and the reliability priority in each individual functional block of the system. The power distribution block, for example, is classified with a high priority, since radiation effects can determine that the output voltage runs out of specification and results into destructive damages of the following devices. Plenty researches have demonstrated that a number of COTS devices are capable to withstand at least high TID [3]. Main problem with COTS devices is that manufactures have different parts screening- and qualification approaches and there is usually a non-visible process-documentation, which

disables the chance to identify parts of certain lots. Thus, selecting COTS parts for the system design requires at least a good visibility of the manufacturing process and, in best case, flight heritage or access to radiation test reports. If none of these requirements can be satisfied, a space qualified solutions should be considered. In addition, there are different failure mitigation techniques that increase the system reliability, without the utilization of space qualified components. In the following sections, radiation hardening strategies by hardware design are presented for functional system blocks.

A. Memory Ressources

The BPS contains a hardened PS memory interface unit. This memory interface unit includes a dynamic memory controller and static memory interface modules. The GSDR uses two DDR3 memory devices, totaling to a density of 512MB with Error Correction Code (ECC) enabled. Thus, failures in the data transmission between the PS and the dynamic RAM can be corrected during operation. A 8Gb NAND-Flash supports non-volatile memory for boot images, initialization procedures and sensitive data storage. The selected NAND flash is a radiation tested COTS device and the manufacturing traceability is sufficient [4]. Moreover, different vendors offer radiation-tolerant NAND-Flashes, which are based on the same die. Magnetoresistive RAM (MRAM) devices, which are known to be tolerant to SEU, are used for backup storage of sensitive system and payload data.

B. Power Regulation

To support the complex architecture with unit- and device specific power, an aggregate regulation and distribution system is required, that provides up to seven different voltage levels. Since there is no multi-channel voltage regulator available at space qualification level, a solution has to be found to achieve both, a highly integrated and small design and a high claim of reliability under radiation conditions. Integrated, multi-channel, solutions have already been tested against TID effects and shows good robustness up to 45kRad, as shown in Fig. 8.

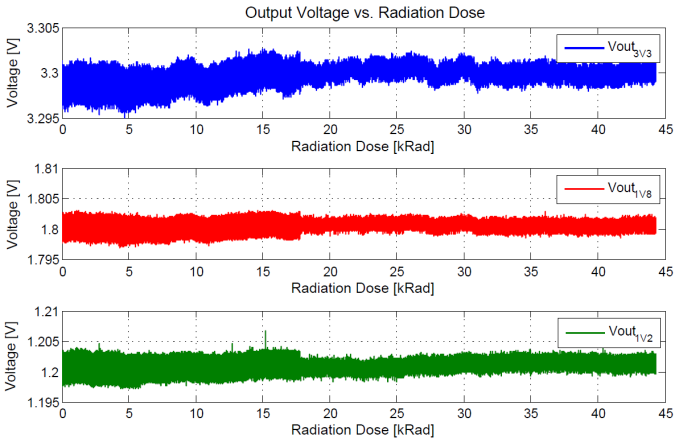

Fig. 8. Output voltages of a selected multi-channel voltage regulator vs. radiation dose up to 45kRad.

Unfortunately, there are no characteristics of SEE, in particular of Single Event Transients (SET). SET occurs in different strength and length and can lead into a destructive damage of the powered devices. Thus, at least an Overvoltage Protection (OVP) circuit is required on every power-line that protects voltage inputs of devices against fast and heavy transients. SEE characterization of the chosen multi-channel power regulator is scheduled and might have influence of the final system design. In worst case, a full space qualified power regulation solutions is feasible, but leads into a very large, inefficient and expensive design.

C. Health monitoring and supervising circuits

Since most of the GSDR system components are preferable based on COTS, it is assumed that radiation effects will decrease the system reliability, even if they claimed space heritage or radiation test data are available. To avoid such impairment, several health monitoring tasks and supervising circuits are implemented into the design. Those mechanisms for example, are based on current sensing and voltage monitoring nodes, to protect the system against SEL and SET.

The SEL detection is partly realized via the Xilinx Analog-Digital Converter (XADC) of the BPS and a current-sense monitoring network within the power regulation unit. The XADC includes a dual 12-bit ADC with a sampling rate of 1MSPS. The XADC is able to monitor up to 17 external differential signals. Moreover, the XADC monitors internal voltages and core temperatures of the SoC. A routine is reading the external voltages continuously with a maximum sampling rate of 1/17MSPS (inputs are multiplexed) and interacts with the power regulation unit to shut down the system, if a non-conformance is detected. The current-sensing monitoring network is realized by shunt-resistors and high accuracy current-sense amplifiers. These amplifiers are required since the monitored voltage-drop over the shunt resistor is too low for the XADC. Selected current-sense amplifiers have also been tested against TID effects as shown in Fig. 9

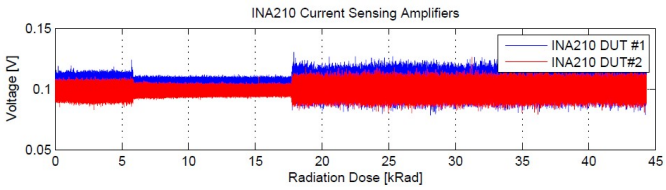

Fig. 9. Output voltages of a selected current-sense monitor vs. radiation dose up to 45kRad.

The results show no gain-deviation and a stable output voltage. The different noise levels (min to max swings) depend on the sampling rates, which have been changed after breaks during the test (7.5kRad, 17.5Krad and final dose).

D. RF Transceiver

As already been mentioned, the AD9361 is categorized as one of the most sensitive and critical devices in the system with respect to SEEs. To ensure that the RF transceiver configuration won't be corrupted by a SEU or permanently damaged by a SEL, the RF transceiver unit is implemented dual redundant. Thus, different fault-tolerant mechanisms are

convertible to improve the reliability against SEUs and destructive failures.

1) Cold Redundancy

A cold redundancy is useful if one of the RFICs will be permanently damaged by a SEE, or the harsh environmental surrounding. This mechanism does not require additional algorithms, but does not prevent corruptions by SEU.

2) Signal Comparison

Signal comparison is comparable to warm/hot redundancy, where the signals simultaneously and independently from each device are processed by the BPS. A signal deviation can be detected afterwards, which may suggest to a SEU in one of the RFIC configuration.

3) Toggle-mode

In this mode only one RFIC (A) is in nominal operation while the other RFIC (B) will be re-configured. After the re-initialization, the previous active RFIC (A) will be re-configured and the pre-initialized RFIC (B) will run in nominal mode. The re-configuration and initialing time is about 10ms, which allows a quick toggle-interval. Thus, it shall minimize the influence by SEUs and allows a reliable operation of the RF transceiver unit.

However, it depends on the operable application, which of the described fault-tolerant mechanisms is more promising and suitable.

V. Radiation Hardening Software Architecture

The software architecture of the GSDR platform approach is important to provide a framework for rapid and easy implementation of different applications and to improve the reliability of the system in addition to radiation hardening strategies by hardware design. This chapter briefly introduces the operational concept and framework for the integration of SDR applications and describes several mechanisms for software reliability assurances.

A. Operational concept

Applications are basically realized in Hardware Description Language (HDL) and are integrated into the reference GSDR system design on the PL. On PS, the GSDR platform runs a tailored, lightweight Linux-based Operation System (OS). The application processed data of the HDL design are captured by a multi-buffer routine, which is implemented into the RF transceiver driver. Those data are processed through the OS by saving-operations or additional signal processing algorithms. Application independent routines are running in background, performing system health checks, data storage and fault-indication and handling. Due to multi-boot mechanisms, the system can be reconfigured between different applications and provide fall-back operation, if an image is invalid (corrupted).

B. Software Reliability Assurance

The GSDR system supports a boot-up sequence to verify the correctness of the loaded boot image from the NAND flash memory via RSA authentication. In case of a corrupted image, the boot sequence features a fall-back option to the next valid image. Once the image is loaded correctly (bitstream has been flashed into the FPGA and the OS is running), several mechanisms ensure error detection and correction, e.g. by ECC in the DDR3 memory. ECC is also available for non-volatile memories to mitigate corruption of payload-data or bootable images. During the nominal operation mode, three internal watchdogs (1x ARM L1 Core, 1x ARM L2 Core and 1x monitoring external device) are enabled and trigger an interrupt in case of a system crash or a program-execution problem. The flashed bitstream into the FPGA is supported by a Soft Error Mitigation (SEM) IP-Core, which detects and restores bit-flips in the FPGA configuration. Additional configuration- and register scrubbing mechanisms are utilized to support SEU mitigation in the FPGA, Memory and RFIC configuration [5].

VI. Conclusion

In this paper the system design and architecture of a fault-tolerant, highly integrated and generic SDR platform for RF applications on spacecraft was presented. Particular focus was made in the design of using selected COTS devices and implementing certain mitigation techniques, to enhance the system reliability under the hash environmental conditions in space. Pre-evaluation test results on a GSDR prototype and promising future system parts (e.g. multi-channel power regulator) were presented. These results have an important influence on further development steps, the selection of sensitive system components and the design of hardening mechanism for radiation effects, to increase the system reliability. Those reliability assurances were separated into hardware and software aspects, whereby the software reliability assurance was only briefly introduced.

In future works, the actual prototype will be re-designed by the presented approaches. The result of this development is going to be analyzed and verified for a small satellite mission of the DLR, which includes mechanical-, electrical-, and environmental test conditions. In particular, thermal-vacuum- and radiation tests (TID and SEE) are scheduled to evaluate the fault-tolerant approaches and to decide if further re-designs are required.

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